# Inductance-Independent Discontinuous Current Mode Control with Minimized Inductor for Power Converters

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Hoai Nam Le

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# Chapter 1

# Introduction

## 1.1 Background

Global warming which is also referred to as climate change, is the rise in the average temperature of the Earth's climate system. The Earth's average temperature has always fluctuated and climate change is not unusual. It is the pace of global warming today that is unprecedented.

Fig. 1.1 depicts the temperature anomaly from 1880 to 2017, recorded by National Aeronautics and Space Administration (NASA) [1-1]. The Earth's temperature had already warmed by 1$^{o}$C compared to pre-industrial levels. This temperature rise might appear small, but just a small rise in temperature would lead to large changes for the world's climate. According to National Geographic, the extra energy coming from just 1$^{o}$C warmer could cause numerous global changes such as; e.g. the Artic is ice-free for half the

year, sea level rises submerge coastal areas, hurricanes occur more frequently around the globe, severe droughts and emergence of new deserts cause shortage in global food supply, and within 85 years one third of the fresh water would be eliminated [1-2].

Fig. 1.2 depicts the atmospheric carbon dioxide concentrations in parts per million (ppm) for the past 800,000 years, recorded by National Oceanic and Atmospheric Administration (NOAA) [1-3]. It is clear that humans have caused most of the past century's warming by releasing heat-trapping gases, i.e. greenhouse gases, as we power our modern lives. Carbon dioxide is the most important of Earth’s long-lived greenhouse gases. It absorbs less heat per molecule than the other greenhouse gases such as methane or nitrous oxide, but it is more abundant and it stays in the atmosphere much longer. Until the pre-industrial levels, the atmospheric carbon dioxide was never higher than 300 ppm. Over the past decade, the global growth rate of atmospheric carbon dioxide has been closer to 2.3 ppm per year, which was only 0.6 ± 0.1 ppm per year in the 1960s. The annual rate of increase in atmospheric carbon dioxide over the past 60 years is about 100 times faster than previous natural increases.

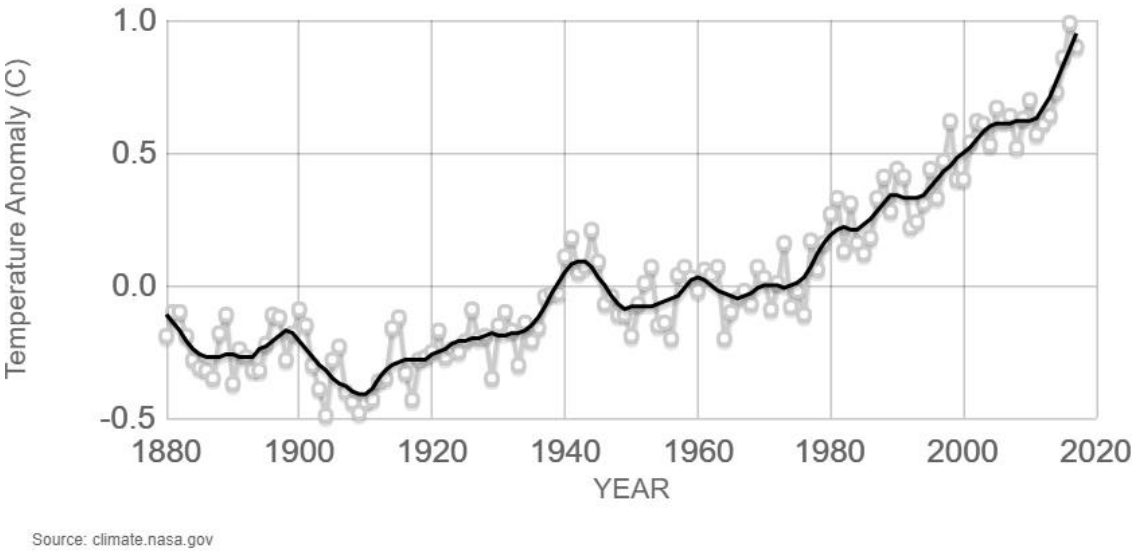



Fig. 1.1. Temperature anomaly from 1880 to 2017, recorded by National Aeronautics and Space Administration (NASA). The Earth's temperature had already warmed by 1ºC compared to pre-industrial levels.

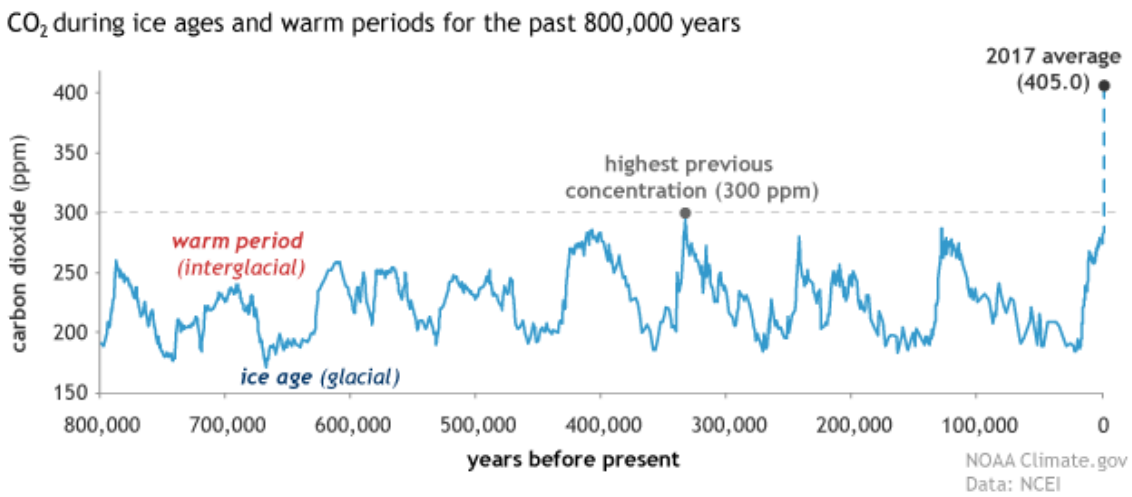



Fig. 1.2. Atmospheric carbon dioxide concentrations in parts per million (ppm) for the past 800,000 years, recorded by National Oceanic and Atmospheric Administration (NOAA). It is clear that humans have caused most of the past century's warming by releasing carbon dioxide as we power our modern lives. The annual rate of increase in atmospheric carbon dioxide over the past 60 years is about 100 times faster than previous natural increases.

Fig. 1.3 depicts the U.S. greenhouse gas emissions and sinks by economic sector from 1990 to 2014, recorded by the U.S. Environmental Protection Agency (U.S. EPA) [1-4], whereas Fig. 1.4 depicts the world energy consumption by source from 1990 to 2040, recorded by the U.S. Energy Information Administration (U.S. EIA) [1-5]. Among the various sectors of the U.S. economy, electricity generation (power plants) accounts for the largest share of emissions-31 percent of total greenhouse gas emissions since 1990. Transportation is the second-largest sector, accounting for 26 percent of emissions since 1990. According to the U.S. EIA, world energy consumption will grow by 48% between 2012 and 2040. Renewables energy sources are the world's fastest-growing energy sources over the projection period, which increases by an average 2.6% per year through 2040. Even though non-fossil fuels are expected to grow faster than fossil fuels (petroleum and other liquid fuels, natural gas, and coal), fossil fuels still account for more than three-quarters of world energy consumption through 2040. In order to accelerate the employment of renewable energy sources, research on renewable energy sources should be further conducted actively and intensely.

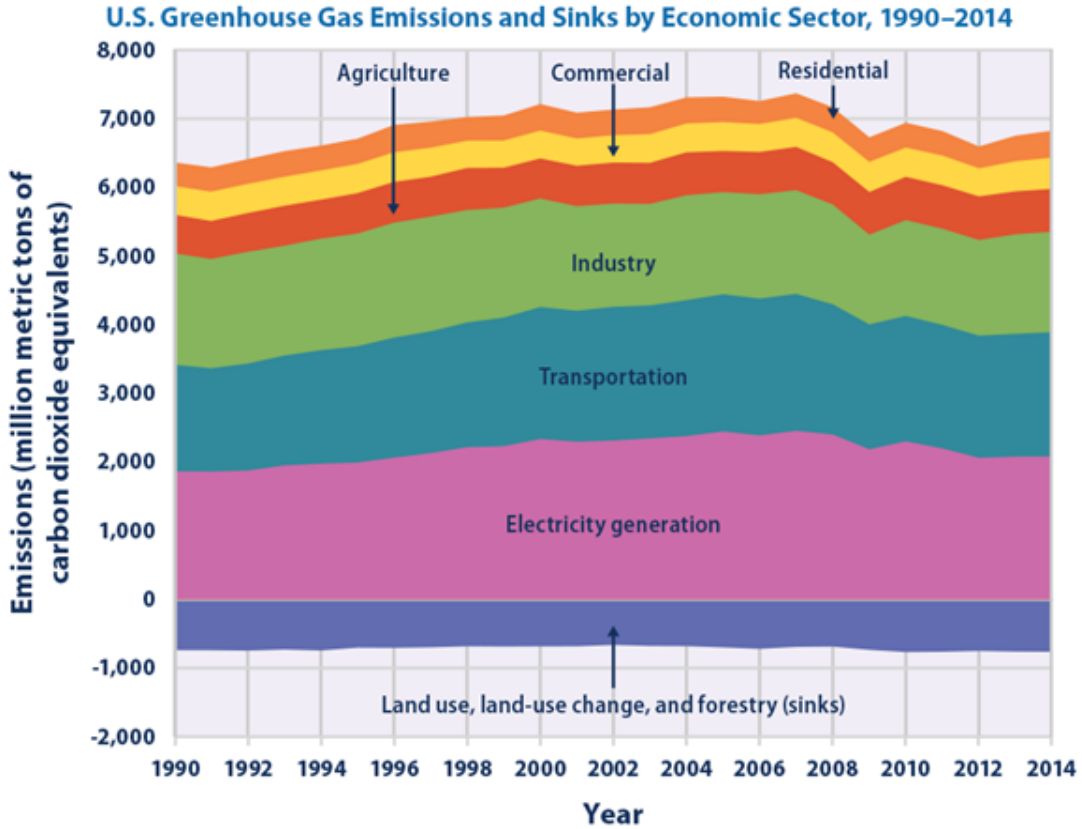



Fig. 1.3. U.S. greenhouse gas emissions and sinks by economic sector from 1990 to 2014, recorded by the U.S. Environmental Protection Agency (U.S. EPA).

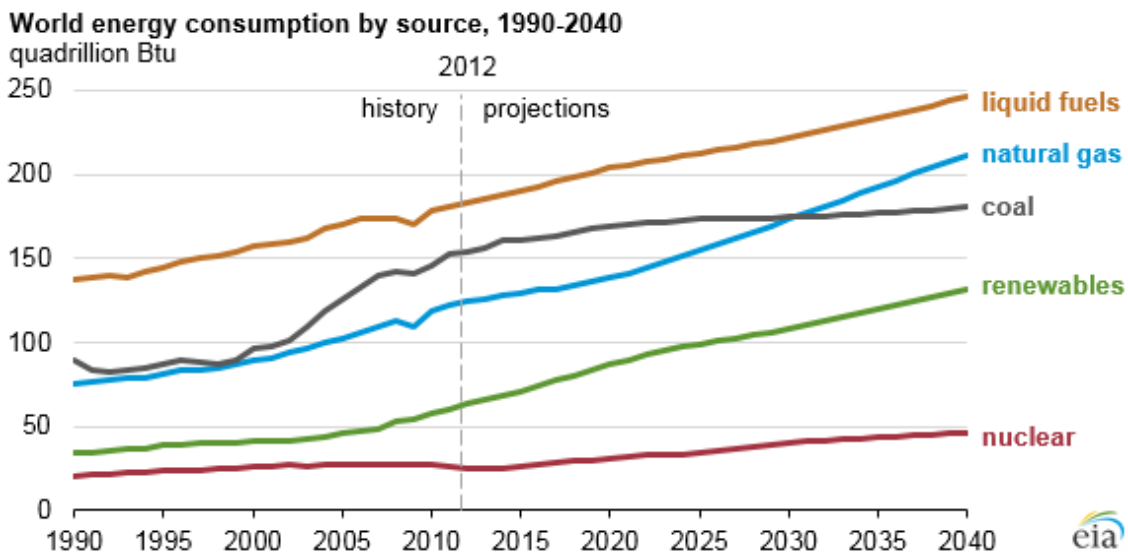



Fig. 1.4. World energy consumption by source from 1990 to 2040, recorded by the U.S. Energy Information Administration (U.S. EIA).

Fig. 1.5 depicts the electricity generation system employing renewable energy sources. The notable characteristic of such electricity generation system is that numerous power converters are utilized to convey the electricity power from the renewable energy sources to the electrical grid. These power converters, which can be divided into four categories as, AC/DC, DC/AC, DC/DC, and AC/AC power converters, play a vital role in renewable energy systems. Therefore, many studies focusing on these power converters are actively conducted in terms of stability, efficiency, size and cost.

Fig. 1.6 depicts the breakdown of the solar power systems. This thesis focuses on the research of the DC/DC and DC/AC power converters in the solar power system. In particular, DC/DC converters, single-phase grid-tied inverters and three-phase grid-tied inverters are considered as the research objectives. In solar power systems, DC/DC converters achieve the maximum power point tracking in each solar cells, whereas single-phase or three-phase grid-tied inverters converts the DC power into the AC power to transmit to the electrical grid. Therefore, these converters' performance greatly contributes to the solar power system expansion.

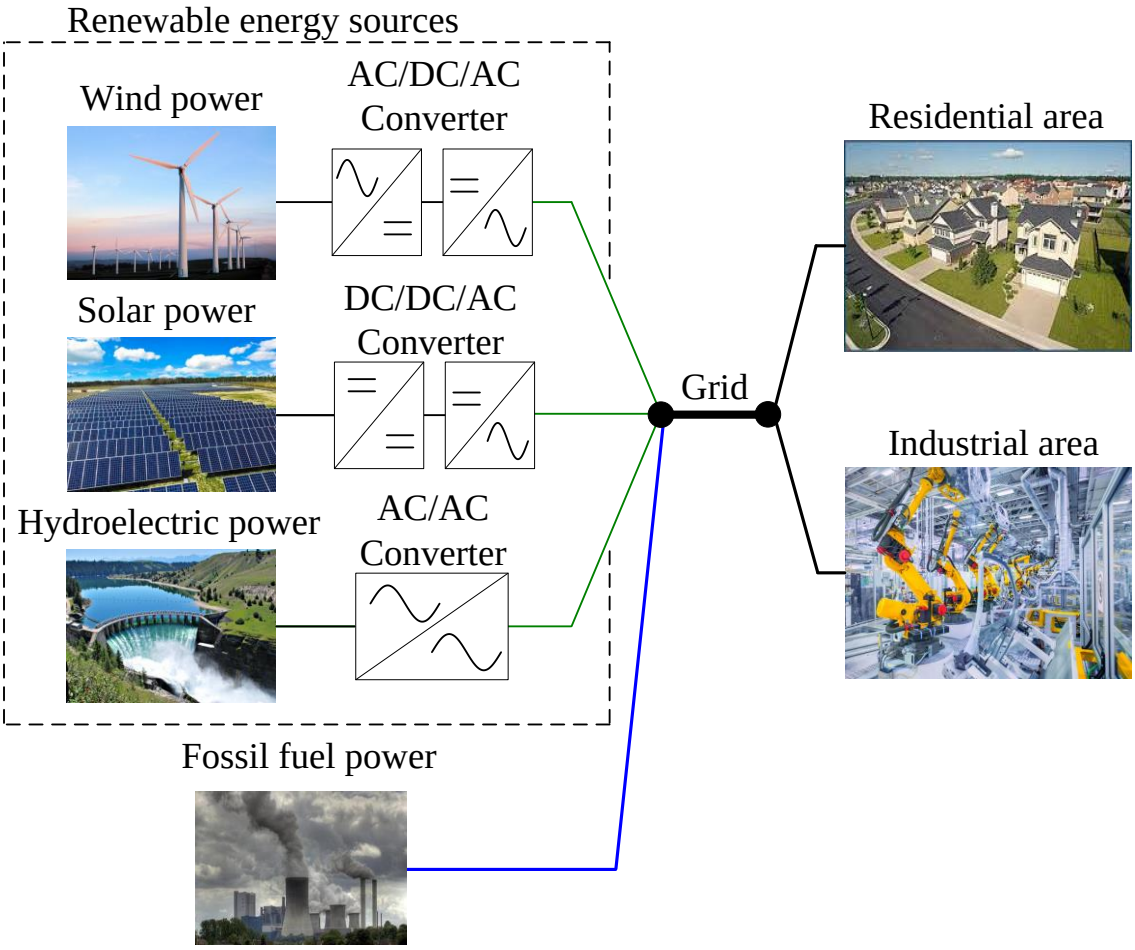
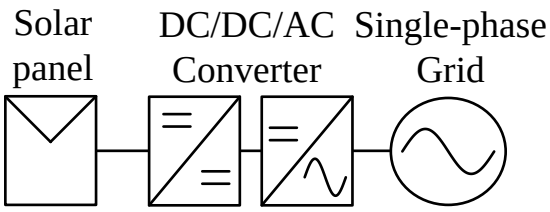
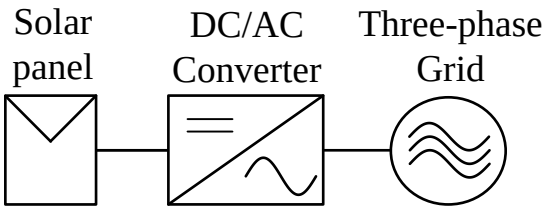



Fig. 1.5. Electricity generation system employing renewable energy sources.




(1.6.a) Single-phase grid-tied solar power systems




(1.6.b) Three-phase grid-tied solar power systems

Fig. 1.6. Breakdown of the solar power systems.

## 1.2 Research Objectives

Over last decades, the employment of solar power systems has accelerated due to a continuously decrease in solar panel price. In the solar power systems, typical boost DC-DC converters and grid-tied inverters are required in order to transmit solar DC power into AC single-phase grid. High efficiency and compact size with low cost are requirements for these converters and inverters in order to further assist the penetration of the solar power systems.

Fig. 1.7 depicts the component volume distribution in the typical boost converter with power rating of 1 kW [1-6]. The problem in the typical boost converters is the use of bulky passive components, i.e. an output capacitor and a boost inductor. One of the challenges to minimize the output capacitor is the dynamic voltage regulation during the fast load transient. In the applications for power conditioning system, the output voltage within a tight tolerance range must be maintained during the faults of the grid, i.e. a load current step occurs. The load transient requirement can be met even with small capacitance by a wide bandwidth voltage control [1-7]-[1-8]. Meanwhile, many minimization methods for the inductor have been

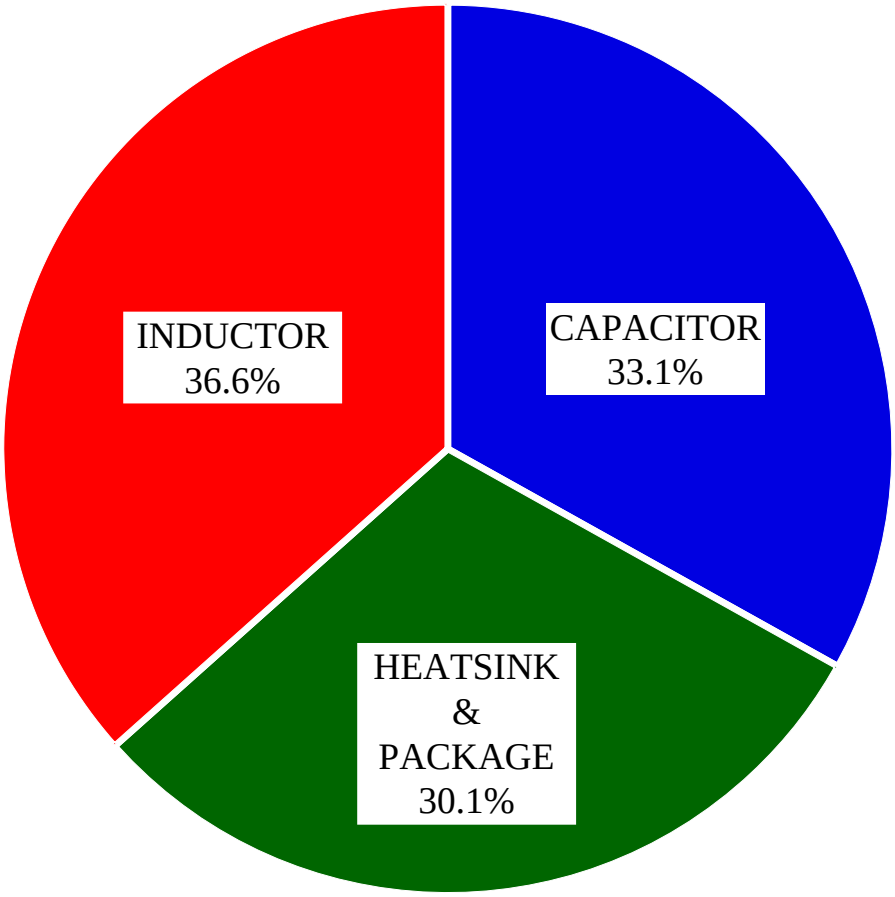



Fig. 1.7. Component volume distribution in the typical boost converter with power rating of 1 kW [1-6].

proposed such as high frequency switching, coupled-inductor or flying-capacitor topologies [1-9]-[1-12]. However, higher switching frequency leads to the increase in both the switching loss and the emission noise [1-13], whereas the addition components results in the complexity of the design in the main circuit and the control method.

There are other approaches to minimize the boost inductor in terms of the operation mode. By increasing the current ripple at a given switching

frequency, the typical boost converters can be operated in two main current modes; continuous current mode (CCM) and discontinuous current mode (DCM) [1-14]-[1-15]. The advantages of CCM are: simple controller design due to the linear duty-ratio-to-inductor-current transfer function, and the simple average current sampling. On the other hand, the boost converter with the DCM operation achieves the high efficiency over a wide load range because the current ripple in DCM decreases at light load. Nonetheless, the nonlinear duty-ratio-to-current transfer occurs in DCM, which worsens the current control performance when the same controller as in CCM is used. In particular, the effects of the DCM nonlinearity on the duty-ratio-to-current transfer function changes according to the current load [1-16]. This results in the overcurrent when the current is regulated by a wide bandwidth controller [1-17]. In past few years, many researches focusing on the control of DCM have been reported to solve this problem [1-18]-[1-23]. However, in those control methods, the DCM nonlinearity compensation method becomes circuit-parameter-dependent. Due to this problem, a wide bandwidth current control is still difficult to be applied into DCM. Consequently, the bandwidth of the voltage control cannot be increased in

order to minimize the output capacitor [1-24], which restricts the circuit minimization.

On the other hand, in the grid-tied inverters, *LCL* filters are generally employed between the output of the inverter and the AC single-phase grid in order to suppress current harmonics and meet grid current harmonic constraints as defined by standards such as IEEE-1547 [1-25]. Inductors in the *LCL* filters account for major volume and cost of the inverter, which can be decreased by a low-inductance *LCL* filter design [1-26]-[1-30]. However, the reduction of the inductance implies a design of a high current ripple due to a high dc-link-voltage-to-inductance ratio. This high current ripple results in a current distortion phenomenon entitled zero-current clamping, in which the current distortion increases notably as the current ripple increases [1-31]-[1-36].

When the zero-current clamping occurs, the inverter operation changes from continuous current mode (CCM) to discontinuous current mode (DCM), which is well-known for its strong nonlinear behavior. In particular, the DCM operation exhibits a nonlinear duty-ratio-to-current transfer function, which significantly changes the converter dynamic; consequently, the

current distortion increases when the same CCM controller is used to control the DCM current [1-16], [1-21], [1-37]. Similarly to the DCM operation in the boost converters, many researches focusing on compensation methods for the DCM nonlinearity have been reported to solve this problem [1-21], [1-23], [1-38]-[1-42]. However, the critical penalty of those methods is that the nonlinearity compensation for DCM is dependent on the inductance. In the solar power systems, the inductors with high tolerance are generally employed in the inverter; furthermore, the grid-tied inverter is required to deal with severe changes of the ambience, i.e. the inductance varies frequently. When actual inductances are different from nominal values, the stability of such inductance-dependent control methods can no longer be guaranteed. In general, the inductance-dependent control bandwidth is designed to be low to ensure the stability, restricting the application of the DCM operation. On the other hand, the inductance-independent control for the DCM operation can compensate the DCM nonlinearities while still achieving a wide control bandwidth because the inductance toleration no longer has a significant effect on the control stability. Consequently, the inductance-independent DCM control is essential for expanding the

employment of the DCM operation.

The objective of this research is to minimize the inductors in the solar power systems. The inductance reduction is accomplished by the low-frequency high-current-ripple design, leading to the operation of DCM. Consequently, the solar power systems benefit in term of size and efficiency because the high-switching-frequency design is unnecessary to minimize the inductance.

First of all, the inductance-independent control of DCM is studied. As previously discussed, the DCM operation enables the inductor minimization even at the low switching frequency because this operation mode features a low-frequency high-current-ripple design. Furthermore, the DCM operation also provides an efficiency improvement at light load due to the load-dependent decrease in current ripple. However, the application of the DCM operation still remains inactive. One of the reason is the occurrence of the nonlinearity in the DCM operation; this makes the converter control become inductance-dependent. Consequently, the control bandwidth of the DCM operation is generally low to ensure the converter stability. This research focuses on the inductance-independent nonlinearity compensation for the

DCM operation. If the nonlinearity in the DCM operation is completely compensated independently from the inductance, the same controller designed in the CCM operation can be applied and the same control bandwidth as in CCM can be achieved.

Then, the mode transition between the CCM and DCM operation is studied. Similarly, the inductance-independently current mode detection between CCM and DCM is necessary when the inverter is designed to operate in both CCM and DCM. When both the current mode detection and the DCM nonlinearity compensation becomes independently from the inductance, the employment of the proposed control method is no longer restricted. Consequently, the inductor can be actively minimized due to the application of the DCM operation.

Finally, the hybrid current mode between DCM and triangular current mode (TCM) is studied. The hard switching on turn-on still occurs in CCM and DCM; this restricted the design of the high switching frequency to further minimize the inductors. The hybrid current mode between DCM and TCM achieves both zero-voltage-switching (ZVS) and current reduction at light load. Therefore, the high efficiency is achieved over wide load range.

## 1.3 Thesis Outline

Fig. 1.8 shows the outline of this thesis divided into 7 chapters. Chapter 1 introduces the importance of the renewable energy sources being the key to fight against global warming issue. Next, the power converter role in such renewable energy sources is discussed. In particular, the power conversion in the solar power systems is focused in this research. Then, the objectives to minimize the inductors in the solar power systems are demonstrated.

Chapter 2 reviews the state of arts of current control for CCM and DCM, and propose the novel method. First, the DCM control challenges in DC-DC converters, and single-phase and three-phase DC-AC converters are discussed and then following by the conventional inductance-dependent control for CCM and DCM. Then, the inductance-independent control for CCM and DCM are proposed with the hybrid DCM. The original idea in this thesis is that the DCM nonlinearity compensation is constructed by utilizing a duty ratio at a previous calculation period instead of using the inductance. Furthermore, the current mode is also determined without using the inductance by the comparison of the output duty ratios. After that, the beneficial position of the proposed method compared with the conventional

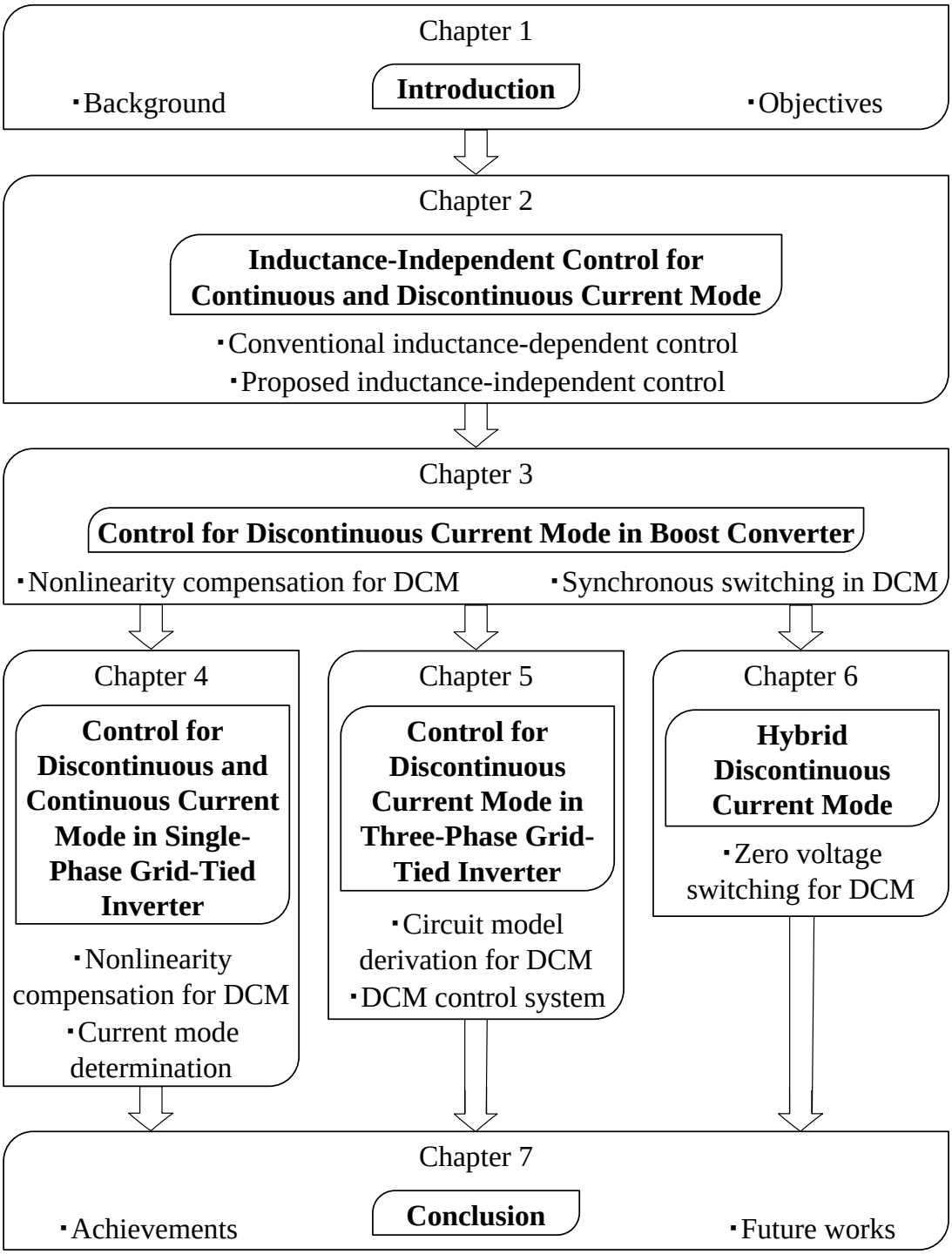



Fig. 1.8. Outline of the thesis.

method is discussed. Finally, the conclusion of the chapter is provided.

Chapter 3 discusses the proposed DCM control for boost converter as an

example for DC-DC converters. First, the design of the conventional PI controller is explained because the proposed DCM control is based on the CCM control with a PI controller, next the inductance-independent DCM nonlinearity compensation method is proposed as the main part of this chapter. Then, the validity of the proposed DCM nonlinearity compensation method is verified. In addition, in order to achieve higher efficiency in the boost converter, the simple DCM synchronous switching method is realized based on the proposed DCM current control. After that, the comparisons of the efficiencies and the current-control computation time are demonstrated in order to confirm the effectiveness of the proposed DCM current control. Finally, the conclusion for the chapter is provided.

Chapter 4 discusses the proposed CCM/DCM control for single-phase grid-tied inverter. First, the zero-current clamping phenomenon is explained together with the problems of the conventional DCM nonlinearity compensation methods, then the CCM/DCM current control based on the inductance-independent DCM nonlinearity compensation is proposed as the main part of this chapter. Next, the mechanism of the current mode detection without using the inductance is explained. After that, the effectiveness of the

proposed CCM/DCM current control is confirmed. Finally, the conclusion for the chapter is provided.

Chapter 5 discusses the proposed DCM control for three-phase grid-tied inverter. First, the circuit model for DCM is derived, and following by the proposed DCM control system. Next, the effectiveness of the proposed DCM control is confirmed by simulation. After that, the operation of the proposed DCM control is experimentally verified together with the efficiency comparison. Finally, the conclusion for the chapter is provided.

Chapter 6 discusses the hybrid DCM. First, the drawbacks of the conventional current mode are provided, and following by the hybrid current mode between DCM and TCM. Next, the generation and control of the hybrid DCM is demonstrated. After that, the operation of the hybrid DCM is experimentally verified together with the comparisons of root-mean-square current and efficiency. Finally, the conclusion for the chapter is provided.

Chapter 7 provides the conclusion for the thesis. In this chapter, the advantages and drawbacks of the proposed converter are classified clearly. The present works are summarized and future works which are expected to be carried out will be discussed.

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# Chapter 2

# Inductance-Independent Control for Continuous and Discontinuous Current Mode

## 2.1 Introduction

The previous chapter described the vital role of power converters in the solar power systems. The minimization of passive components in power converters not only solves many space issue for hardware designer, but also gives many advantages such as, e.g. cost reduction. In this thesis, the inductance-independent CCM&DCM control method is proposed to reduce the inductor volume at certain switching frequency.

In this chapter, first, the inductor minimization by the CCM&DCM control method is explained in detail. Then, the state-of-the-art CCM&DCM control methods are reviewed and discussed. The control loop gain

characteristics of the CCM and DCM operations are completely different from each other, leading to the requirement of the separation for the CCM and DCM duty generations in the CCM&DCM control methods. Therefore, the CCM&DCM control methods are basically combined three parts;

(i) CCM control,

(ii) DCM control,

(iii) Current mode detection of CCM and DCM.

The DCM control methods and the current mode detection of CCM and DCM in each parts are discussed and the advantages/disadvantages in term of control performance and compatibility are elaborately demonstrated. A comparison chart is provided to discuss about the most applicable CCM&DCM control method for the solar power system.

Then, the proposed inductance-independent CCM&DCM control method is described in detail. The beneficial position of the proposed control method along with other conventional control methods is presented. The superiority position of proposed converter is discussed to show the contribution of this research.

## 2.2 Inductor Minimization with CCM&DCM Control Method

In this chapter, the typical boost converter in the single-phase PV system is considered as an example.

Fig. 2.1 depicts the typical boost converter in the single-phase PV system. As shown in Fig. 1.6 and Fig. 2.1, there are three factors which contribute to the volume; the heatsink of the semiconductor devices $Vol_H$, the boost inductor $Vol_L$ and the capacitor $Vol_C$. The capacitor volume is determined by the capacitance, the allowable current ripple and the capacitor type. In the single-phase PV system, the factor dominating the design of the capacitor volume is the capacitance, which is designed to absorb the power ripple from the single-phase grid, i.e. the passive power decoupling [2-1]. Active power decoupling methods can reduce the required capacitance, leading to the capacitor volume reduction. However, the topic on the active power decoupling methods is out of scope of this thesis. Hence, the volume-reducible components in the typical boost converter is the inductor and the heatsink.

The volume of the heatsink changes according to the loss from the

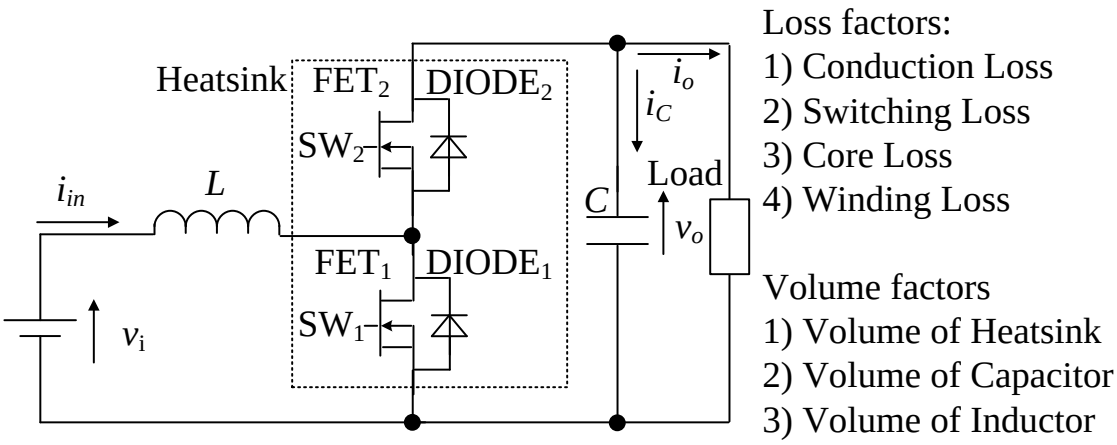



Fig. 2.1. Typical boost converter. The losses and volume is calculated in order to design the power density and the power conversion efficiency.

semiconductor devices. The estimation of the heatsink volume $Vol_H$ is conducted based on the Cooling System Performance Index (CSPI) [2-2], which is defined as the inverse factor of the thermal resistance per unit volume; hence, the higher CSPI becomes, the more effective the heat is dissipated through the heatsink,

$$Vol_H = \frac{1}{R_{th(s-a)}CSPI} = \frac{1}{CSPI} * \frac{1}{\frac{T_j - T_a}{P_{cond} + P_{sw}} - R_{th(j-s)}} \quad \text{.....(2.1)}$$

where $R_{th(s\text{-}a)}$ is the required thermal resistance between the heatsink and the ambience, $T_j$ is the junction temperature of the MOSFET, $T_a$ is the ambient temperature, $R_{th(j\text{-}s)}$ is the thermal resistance between the junction and the heatsink, $P_{cond}$ and $P_{sw}$ are the conduction loss and switching loss of the

semiconductor devices.

Meanwhile, the inductor volume $Vol_L$ is calculated by the Area Product [2-3]-[2-4],

$$Vol_L = K_V \left( \frac{LI_{\max}^2}{K_u B_{\max} J} \right)^{\frac{3}{4}} = K_V \left[ \frac{V_i (V_o - V_i) I_{avg}}{2K_u B_{\max} J V_o} \frac{1}{f_{sw}} \left( \sqrt{\Delta I} + \frac{1}{\sqrt{\Delta I}} \right) \right]^{\frac{3}{4}} \quad (2.2)$$

where $K_V$ is the coefficient which depends on the shape of the core [2-3], $K_u$ is the window utilization factor, $B_{max}$ is the maximum flux density of the core, $J$ is the current density, $\Delta I$ is the boost inductor current ripple, $f_{sw}$ is the switching frequency. It is clearly understood from (2.2) that, the inductor volume depends on both the switching frequency $f_{sw}$ and the current ripple $\Delta I$. In the typical inductor minimization method, the inductor current ripple is designed to be smaller than 10%, whereas the switching frequency $f_{sw}$ is increased. Nevertheless, the high switching frequency $f_{sw}$ leads to the increase in the switching loss, requiring the larger heatsink as aforementioned. There are several methods to avoid the increase in the switching loss even with the high switching frequency, e.g. the multi-level topology [2-5]-[2-6] or the soft switching technique [2-7]-[2-10]. The multi-level topology enables the low switching frequency of the low voltage rating switching devices in each modular to result in the high current-ripple

equivalent-frequency. In the other words, the multi-level topology can minimize the inductor without increasing the heatsink volume. However, the voltage unbalance issue is one of the main problems restricting the application of the multi-level topology. On the other hand, soft switching techniques can greatly reduce the switching loss, in which resonance between an inductor and a capacitor is utilized in order to achieve zero-voltage switching (ZVS). However, in order to satisfy conditions for ZVS, these methods suffer many drawbacks such as, e.g. a requirement of additional components, a restriction of controllable duty ratio or a sharp decrease in the efficiency at light load.

Fig. 2.2 shows the relationship among the current ripple, the inductor volume and the heatsink volume [2-4]. This thesis focuses on the minimization limitation of the inductor volume at certain switching frequency by varying the current ripple. Focusing on the characteristic of the inductor volume, the minimization of the inductor volume by the high current ripple design shows a high effectiveness in the current ripple range from 10% to around 40%, showing by the sharp decrease slope of the inductor volume. However, the high current ripple design becomes less

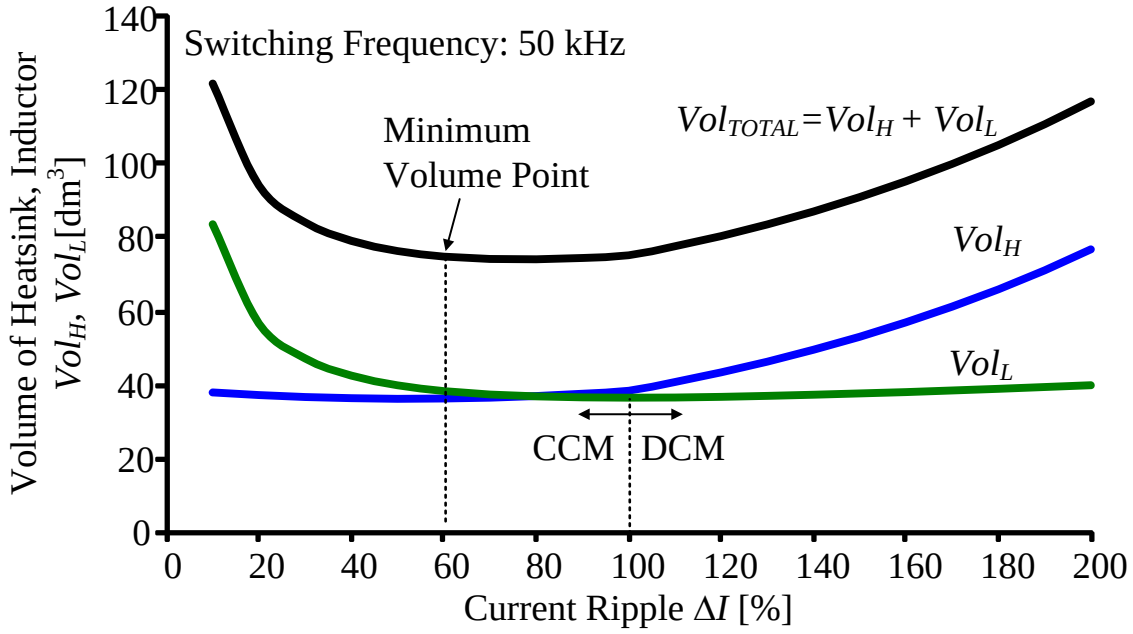



Fig. 2.2. Relationship among current ripple, inductor volume and heatsink volume. By varying the current ripple, the smallest total volume of the inductor and the heatsink is achieved at the current ripple of 60%.

effective on the inductor volume minimization when the current ripple keeps increasing from 40%. Especially, the high current ripple has no effectiveness on the inductor volume minimization when the current ripple is higher than 100%, where is the boundary between the CCM and DCM operations. It implies that the design which makes the circuit deeply operate in DCM provides no benefit on the inductor minimization.

Meanwhile, the high current ripple design increases the root-mean-square current value even with the same current average value, i.e. same output power, leading to the increase in the conduction loss of the

semiconductor devices. As aforementioned, the high conduction loss of the switching devices requires the larger heatsink. Therefore, it is clearly observed from Fig. 2.2 that the heatsink volume increases with the high current ripple design. It implies that there is the minimum total volume of the inductor and the heatsink as the current ripple is varied. The design of the typical boost converter in [2-4] confirms the minimum total voltage of the inductor and the heatsink is achieved with the current ripple of 60%, leading to the CCM operating at rated load and the DCM operation at light load, i.e. the mixed conduction mode between CCM and DCM. Therefore, this thesis focuses on the CCM&DCM control methods to achieve the inductor minimization.

## 2.3 Overview of Continuous and Discontinuous Current Mode Control

Fig. 2.3 depicts the classification of the CCM&DCM control methods. In the unidirectional converter such as, e.g. one-switch boost converters or bridgeless power factor converters (PFC), the DCM operation inevitably occurs at light load [2-11]-[2-28]. On the other hand, in the bidirectional converters such as, e.g. two-switch boost converters or grid-tied inverter, the occurrence of DCM is difficult to analyze because the DCM operation occurs only during the dead time interval near the current zero crossing points [2-29]-[2-37]. In order to deal with the nonlinearity in DCM, the separation for the CCM and DCM duty generations is required in the CCM&DCM control methods. Hence, the CCM&DCM control methods intrinsically need the current mode detection of CCM and DCM. Consequently, the CCM&DCM control methods are basically combined three parts; CCM control, DCM control, the current mode detection of CCM and DCM. The CCM control methods are divided into two groups: CCM feedforward control and CCM feedback control, which are not the main focus on this thesis. Therefore, the explanation of the CCM control methods are omitted.

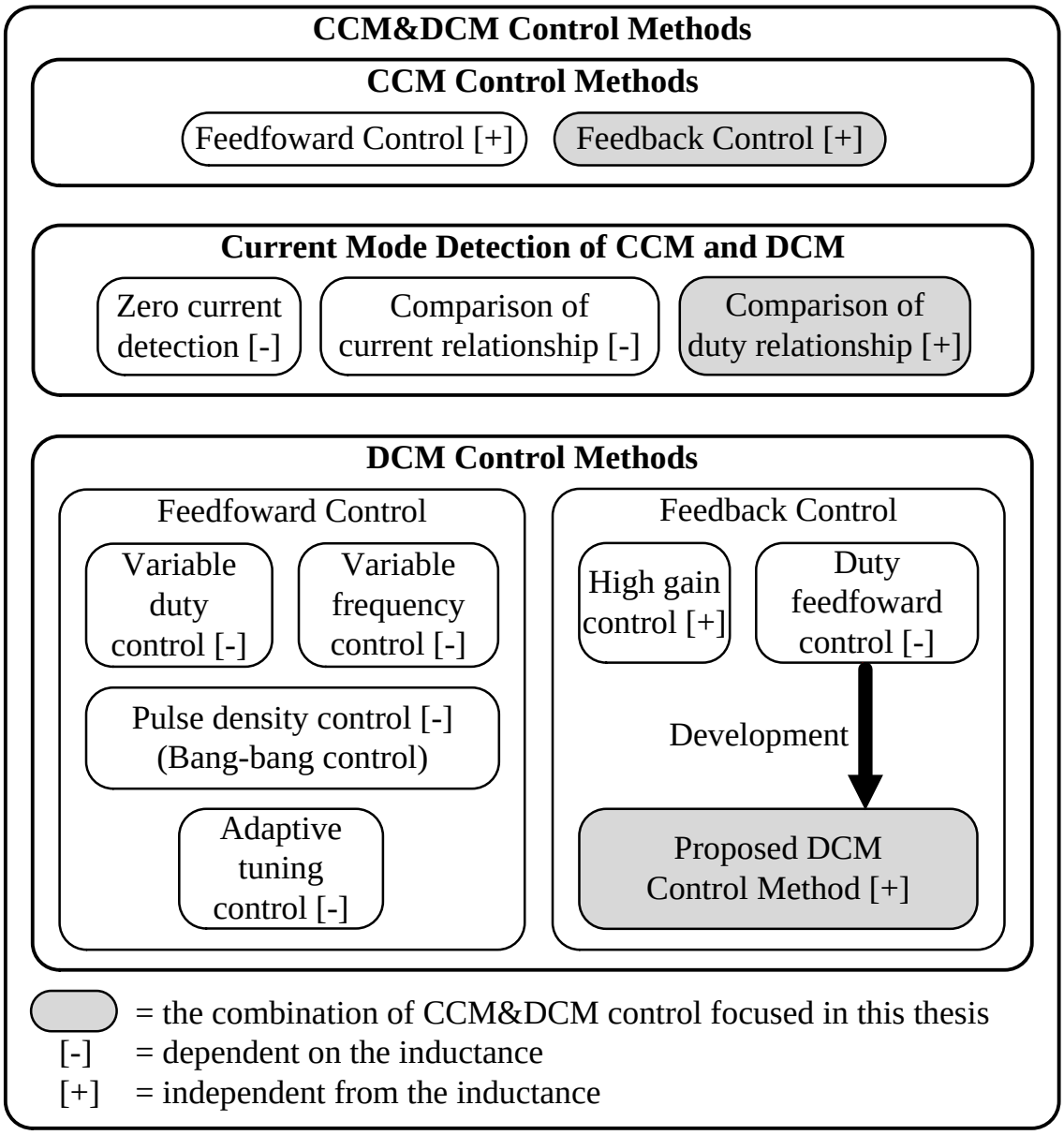



Fig. 2.3. Classification of CCM&DCM control methods.

On the other hand, the conventional DCM control methods can be divided into two groups: DCM feedforward control and DCM feedback control. The DCM feedforward control is divided into three subgroups: variable duty control [2-11]-[2-18], variable frequency control [2-19]-[2-20], pulse density

control (or bang-bang control) [2-21]-[2-23] and adaptive tuning control [2-24]. Meanwhile, the DCM feedback control are classified into four subgroups: high gain control [2-25]-[2-26], and duty feedforward control [2-27]-[2-31]. The current mode detection of CCM and DCM can be divided into three groups: zero current detection [2-23]-[2-24], [2-26], comparison of current relationship [2-14] and comparison of duty relationship [2-27]-[2-28], [2-31]. The combination of the CCM control, the DCM control and the current mode detection in Fig. 2.3 results in the CCM&DCM control. For instance, the CCM&DCM control in [2-23] is combined of the CCM feedforward control, the DCM feed forward control (i.e. the pulse density control), and the current mode detection of CCM and DCM (i.e. the zero current detection).

# 2.4 Conventional Discontinuous Current Mode Control

## 2.4.1 DCM Feedforward Control

The feedforward current control is generally applied to control the DCM current, because there is nonlinearities in DCM, which restricts the application of the feedback control [2-38]. The feedforward current control benefits from the simple controller design, and the elimination of the current sensor. Nevertheless, the feedforward current control alone cannot provide the accurate current control in the practical application due to several reasons such as, e.g. the tolerance of the devices, or the temperature-dependent value variation. Therefore, the feedforward current control for CCM and DCM are generally employed with an outer loop voltage feedback control, resulting in a cascade control [2-39]. The error between the current reference and the actual current is compensated by the outer loop voltage feedback control. This cascade control for CCM and DCM is basically divided into three subgroups: variable duty control [2-11]-[2-18], variable frequency control [2-19]-[2-20], pulse density control (or bang-bang control) [2-21]-[2-23] and adaptive tuning control [2-24].

**(1) Variable duty control**

The duty in the DCM operation directly depends on the current due to the nonlinearity [2-38]. Consequently, the variable duty control achieves the current regulation by varying the duty under the constant switching frequency, i.e. pulse width modulation (PWM). The relationship between the duty and the current in DCM is based on the reduced-order model or the full-order model. This variable duty control for DCM is employed in numerous applications such as, e.g. bidirectional DC/DC converters, single-phase grid-tied inverters, three-phase single-switch inverters, or the VIENNA rectifiers [2-11]-[2-18].

Fig. 2.4 depicts the variable duty control system for DCM in DC/DC converter [2-13]. The DC/DC converter is designed to operate under only DCM at rate load of 45 kW. The duty controlling the switching devices is calculated directed from the inductance, the switching frequency, the inductor current and the input/output voltage (cf., equation (1) of [2-3]). This control method for DCM can be simply implemented in the existing controller. However, unlike DCM, the CCM operation does not exhibit the nonlinearity between the current and the duty. In other words, the current in

CCM does not depend on the duty, but only depends on the change of the duty. Due to this difference between the controls of two current modes, it is difficult to design a fixed high bandwidth control for the converter operating in both CCM and DCM. Hence, the variable current control for DCM is usually employed into the converters operating under only DCM. Another drawback of the variable duty feedforward control is the dependence of the inductance, which is shown in Fig. 2.4.

The example of the control method for the boost converter operating in

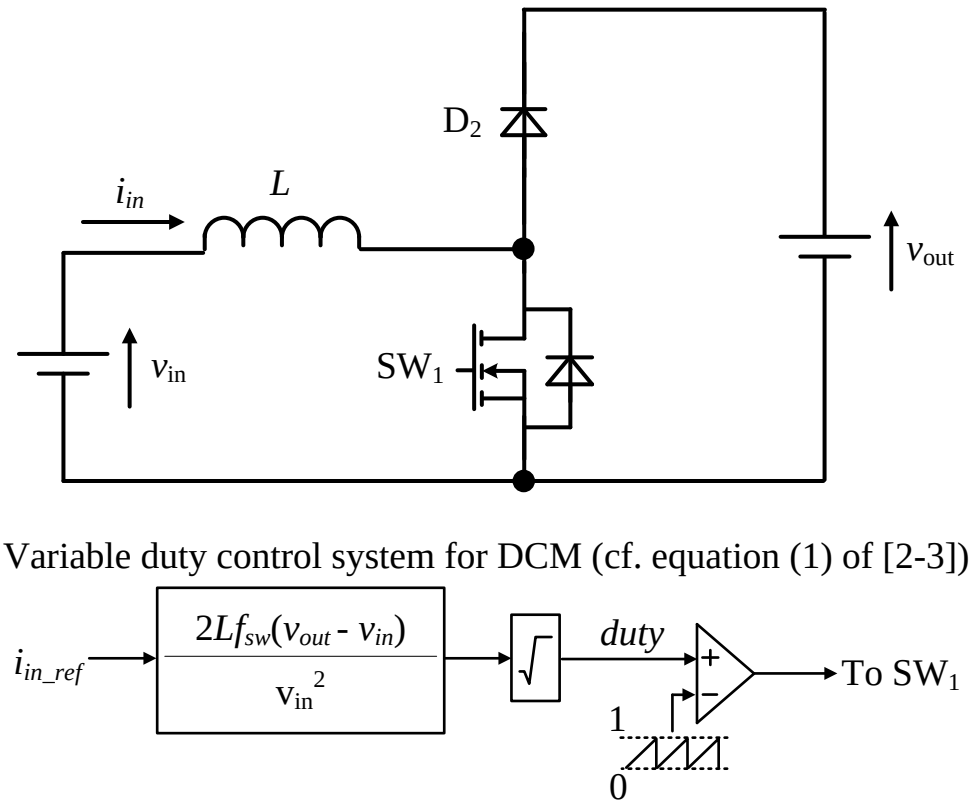



Fig. 2.4. Variable duty control system for DCM in DC/DC converter.

both CCM and DCM can be found in [2-14]. In particular, the CCM current feedback control is employed with the variable duty feedforward control for DCM. As mentioned above, due to the difference of the characteristic between the CCM current feedback control and the DCM variable duty feedforward control, the bandwidth of the mixed control loop is necessary to be low to ensure the control stability, e.g. 100 Hz to 1 kHz despite the sampling frequency of 10 kHz [2-14].

**(2) Variable frequency control**

Fig. 2.5 depicts the variable frequency control system for DCM in DC/AC converter. The principle of this DCM variable frequency control method is similar to that of the DCM variable duty control method; due to the DCM nonlinearity, the DCM current depends directly to the duty, and the switching frequency. Therefore, in the variable frequency control, the switching frequency is varied whereas the off-time (or on-time) is kept constant to achieve the current regulation, resulting in pulse frequency modulation (PFM) [2-19]-[2-20]. Compared to the variable duty control (PWM), the variable frequency control (PFM) spreads the switching-frequency harmonic components over a wide range of frequency, which

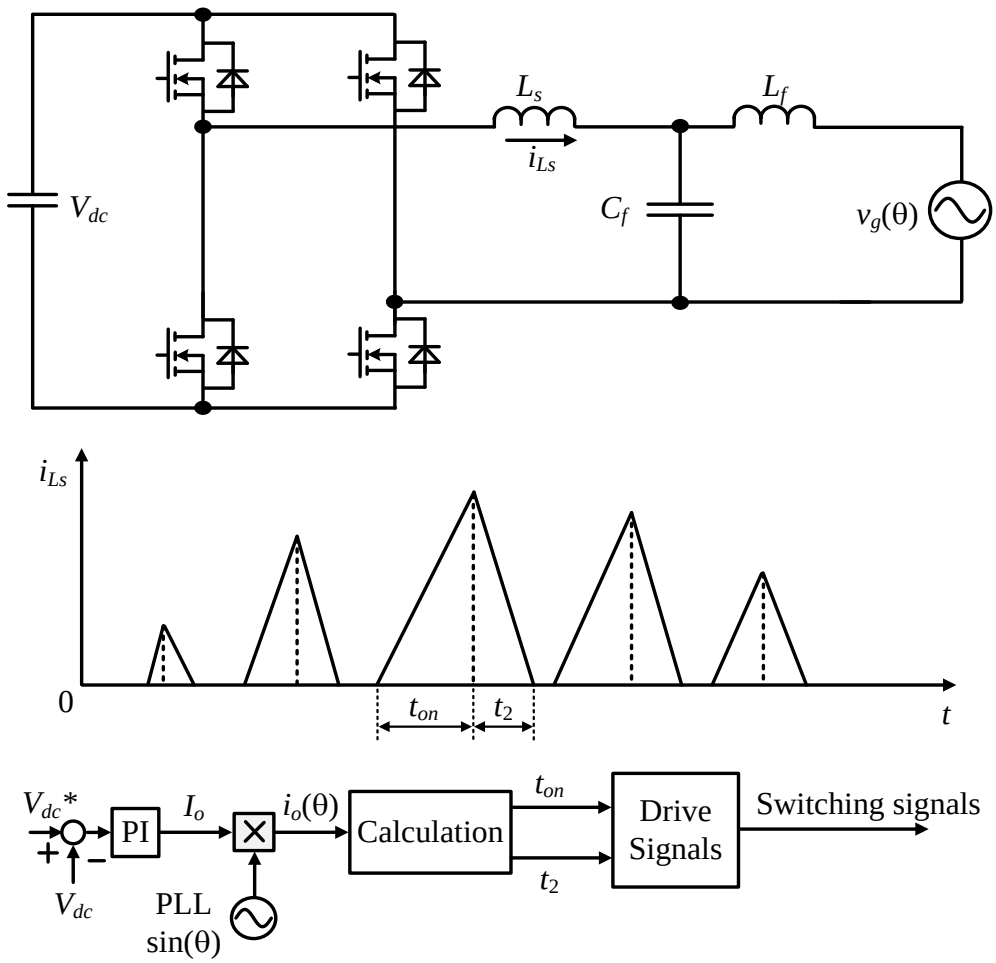



Fig. 2.5. Variable frequency control system for DCM in DC/AC converter.

enables the minimization of the filter. Nevertheless, the DCM variable frequency control still suffers the similar drawbacks of the DCM variable duty control, which are the difficulty in control both CCM and DCM, and the inductance dependence. Hence, the variable frequency control for DCM is usually employed into the converters operating under only DCM with low current control bandwidth.

**(3) Pulse density control**

Fig. 2.6 depicts the pulse density control system for DCM in DC/DC converter. In the pulse density control, each DCM interval is treated as one pulse; the density of the pulses is modulated in order to achieve the current regulation, resulting in pulse density modulation (PDM) [2-21]-[2-23]. The

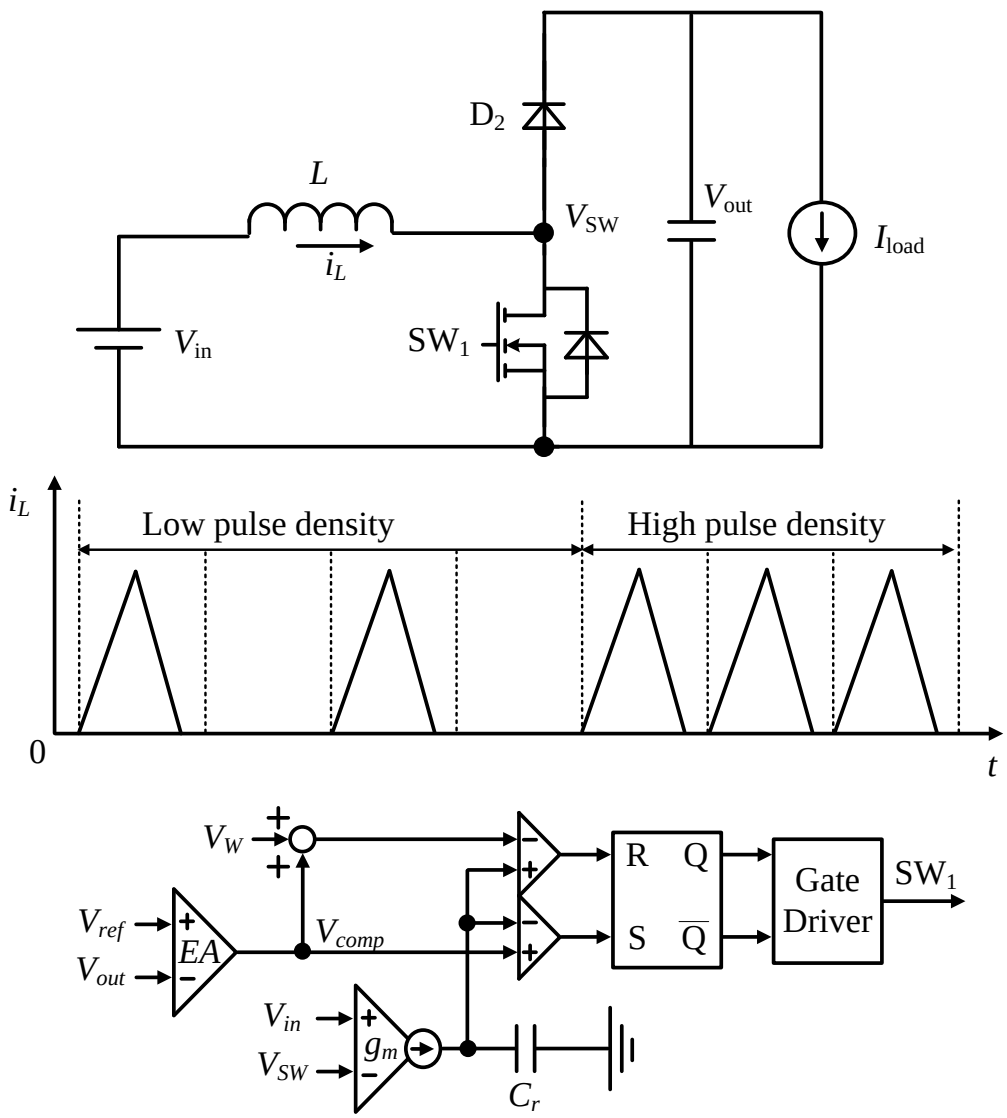



Fig. 2.6. Pulse density control system for DCM in DC/DC converter.

literature in [2-21]-[2-23] proposed the pulse density control for buck converters. The output voltage is compared with the voltage reference to determine the pulse density. Apart from the similar drawbacks of the DCM variable duty control, the pulse density control has some critical drawbacks; the control stability is difficult to be evaluated. Therefore, the pulse density control is normally applied into low power application.

**(4) Adaptive tuning control**

Fig. 2.7 depicts the adaptive tuning control system for DCM in DC/DC converter. As another approach to control both CCM and DCM, a method of continuous adaptive tuning of voltage-mode digital controllers has been proposed in [2-24]. The adaptive controller is designed based on the small-signal model of CCM and DCM. When the DCM operation is detected, the tuning system operates by updating the DCM control gain, and the DCM control coefficients in order to zero the error between the desired and measured stability margins. Simultaneously, the inputs to the CCM control part are held at zero such that the CCM compensator parameters remain unchanged. In reverse, when the CCM operation is detected, the CCM compensator are tuned and loaded into the controller, whiles the most recent

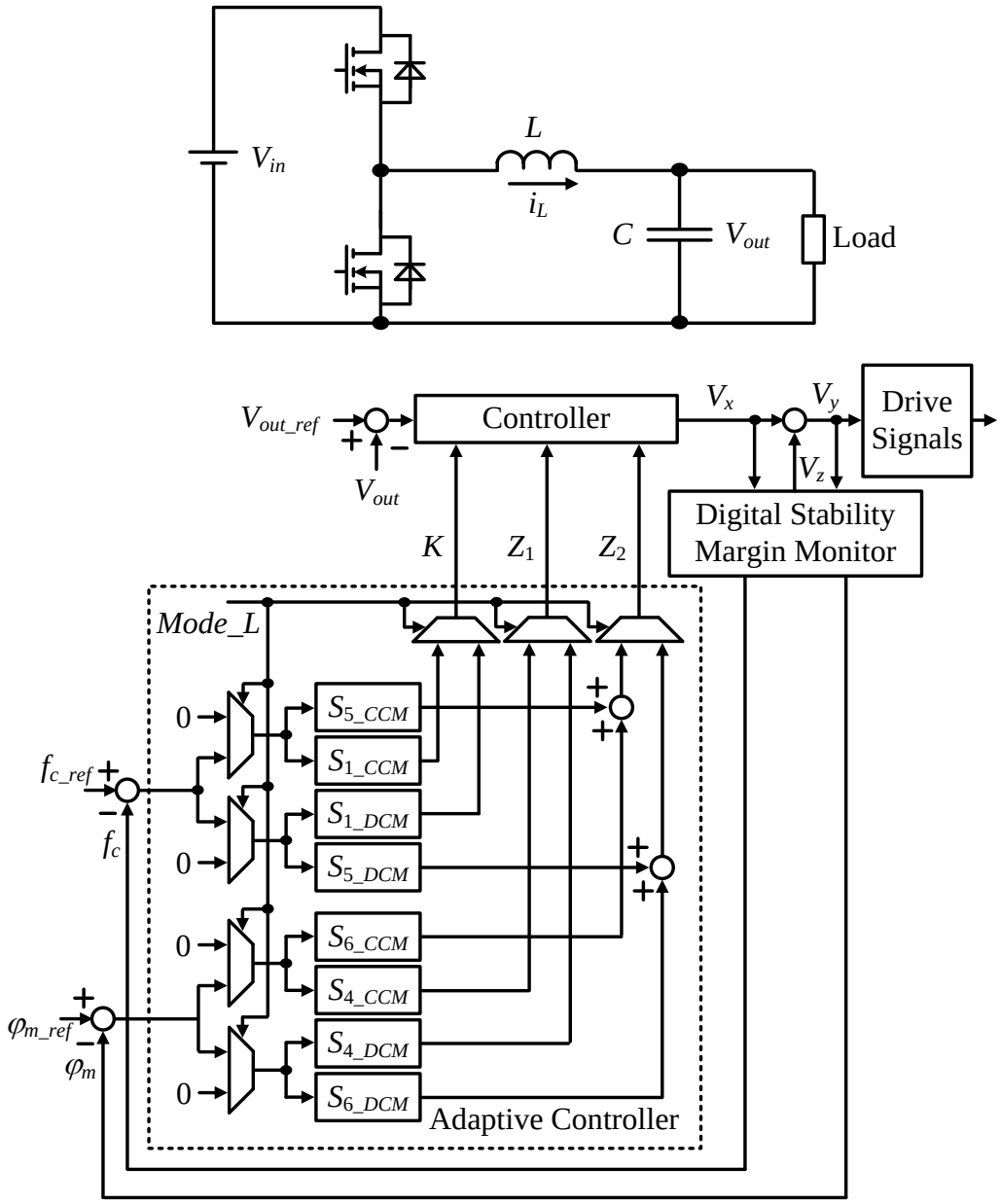



Fig. 2.7. Adaptive tuning control system for DCM in DC/DC converter.

DCM compensator parameters are stored. Note that the current mode determination is carried out by comparing the switched-mode voltage to zero (ground). This detection method assumes that during the zero current interval

in DCM, the switched-mode voltage is clamped at the output voltage; however, in practical application, the switched-mode voltage oscillates during the zero current interval due to the energy oscillation between the inductor and the parasitic capacitance of the switches, which becomes more severe with a low inductance and a high switching frequency. Consequently, the current mode determination in [2-24] has to be tuned for each individual prototype to obtain the desired operation.

### 2.4.2 DCM Feedback Control

In the DCM operation, the duty-to-current loop gain becomes significantly low at light load compared to that in the CCM operation. Therefore, many control methods have been proposed to deal with this load-dependent loop-gain decrease. The outer loop voltage feedback control becomes optional with the employment of the current feedback control. In particular, the feedback current control for CCM&DCM is basically divided into four subgroups: high gain control [2-25]-[2-26], and duty feedforward control [2-27]-[2-31].

**(1) High gain control**

The principle of the high gain control for the DCM operation is to use a high-gain controller to deal with the load-dependent loop gain decrease at light load in DCM. In [2-25], a controller with the cutoff frequency of 20 kHz is employed to control the current with the frequency of just 50 Hz. The obvious drawback of the high gain control is the requirement of the high sampling frequency to implement the high gain controller. In addition, when the converters are designed to operate in both CCM and DCM, two different controllers are required because there is no load-dependent loop gain

decrease in CCM [2-26]. Furthermore, the current mode determination is also necessary to choose the controller for corresponding current mode. In [2-26], the current mode determination is accomplished by the detection of the zero current in DCM. However, the zero current detection faces many challenges in practical applications, one of which is the current oscillation during the zero-current interval. In particular, this current oscillation is caused by the energy oscillation between the inductor and the parasitic capacitance of the switches, which becomes more severe with a low inductance and a high switching frequency. Consequently, the current mode determination in [2-26] has to be tuned for each individual prototype to obtain the desired operation.

**(2) Duty feedforward control**

Fig. 2.8 depicts the duty feedforward control for the boost converter operation in both CCM and DCM [2-27]. The duty feedforward control might appear differently for a variety of application such as, e.g. boost converters [2-27]-[2-28], Vienna rectifiers [2-29], [2-31], or three-phase buck-type rectifier [2-30]. Nevertheless, the same principle to control both CCM and DCM is applied in these duty feedforward control methods. In the

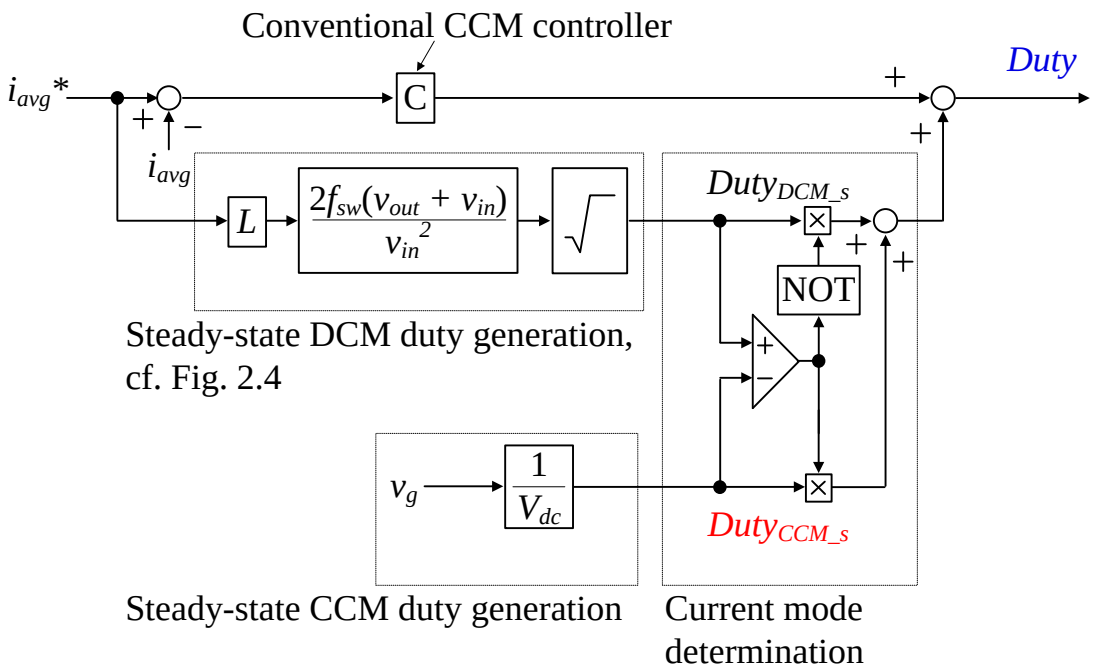



Fig. 2.8. Duty feedforward control for boost converter operation in both CCM and DCM.

only-CCM control, the steady-state CCM duty is fed forward to the output of the controller; consequently, the controller handles only the small difference of the duty between two consecutive sampling periods. This implies that the controllers with low gain is sufficient. The same control mechanism can be applied in order to control the DCM current with low-gain controllers. As shown in Fig. 2.5, in the only-DCM control, the steady-state DCM duty is fed forward to the output of the controller. Furthermore, in order to avoid the current mode determination by the zero current

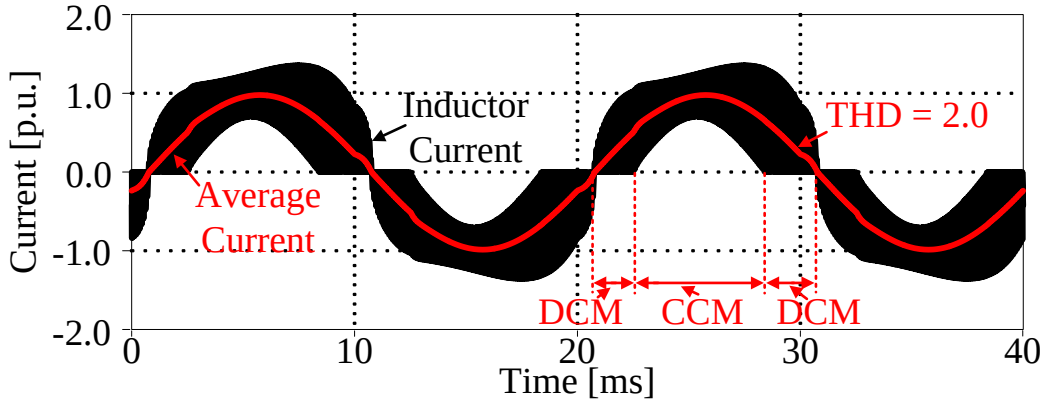
detection, the current mode is determined by the comparison of the steady-state duty between CCM and DCM. Nevertheless, the duty feedforward control still suffers the drawback as the inductance dependence in the steady-state DCM duty generation, which makes the control stability sensitive to the circuit parameter.

### 2.4.3 Problems of Inductance-Dependent Control Systems

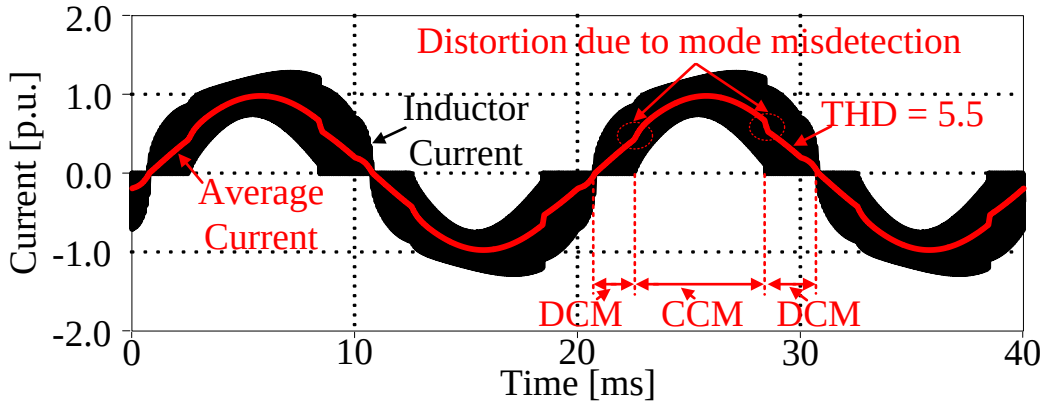
The common drawback in the conventional CCM&DCM control method is the inductance dependence. In particular, the inductance is required in either in the DCM duty generation or the current mode detection of CCM and DCM. With the inductance-dependent DCM duty generation, the bandwidth of the DCM current control varies according to the inductance difference between the nominal value and the actual value of the inductance, referring as the inductance error. This problem can still be overcome by the high bandwidth design of the current control. In other words, the DCM current control can still maintain a stable operation even with the inductance error if the designed bandwidth is designed much higher than the maximum required response of the current. However, the main issue occurs with the mode misdetection of CCM & DCM when the inductance error occurs. As aforementioned, the current dynamics of the CCM operation is completely different from that of the DCM operation. Therefore, if the controller designed under the CCM operation is applied in the DCM operation due to mode misdetection, or vice versa, the current control can no longer maintain a stable operation. This problem becomes more severe in the application

requiring a quick and frequent alternation between the CCM and DCM operation, e.g. the inverter.

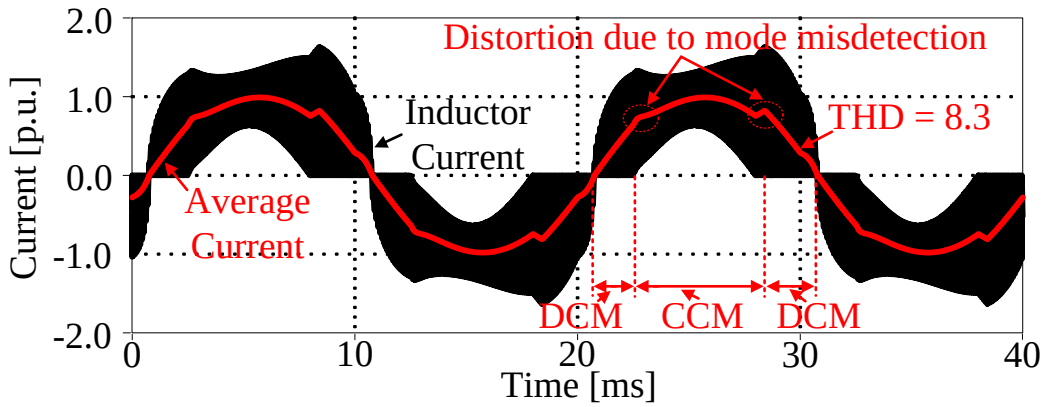
Fig. 2.9 depicts the single-phase inverter current waveform operating under the CCM and DCM with the duty feedforward control (cf. Chapter 2.4.2 of (2)) and several different cases of the inductance error. Fig. 2.9 (a) shows the waveforms with no inductance error, Fig. 2.9 (b) shows the waveforms with the inductance error of +20%, and Fig. 2.9 (c) shows the waveforms with the inductance error of -20%. It is clearly observed from Fig. 2.9 that the current distorts due to the mode misdetection. The inductance error prevents the widespread application of such inductance-dependent CCM&DCM current control, limiting the inductor minimization by the CCM&DCM control.




(a) Actual inductance equals to nominal inductance




(b) Actual inductance equals to 120% of nominal inductance




(c) Actual inductance equals to 80% of nominal inductance

Fig. 2.9. Single-phase inverter current waveform operating under CCM and DCM with the duty feedforward control (cf. Chapter 2.4.2 of (2)) and several different cases of the inductance error.

### 2.4.4 Comparison of Conventional Control Methods

Table 2.1 depicts the comparison of the conventional control methods for CCM&DCM. In the term of response, the variable duty control, the variable frequency control and the pulse density control have the worst response due to the difference in the CCM and DCM plants, whereas the high gain control and the duty feed forward control obtain a good response because the control bandwidth is simply designed to be around 1/10 of the sampling frequency. Meanwhile, the adaptive tuning control has to change the control bandwidth according to the load condition.

Regarding the stability analysis, it is the most difficult to design the stability for the variable frequency control and the pulse density control due to the nonlinear characteristic in the hysteresis control. Meanwhile, the high gain control and the duty feed forward control are simple to analyze the stability because these controller design of these methods is based on the conventional CCM-only control. The missing of the inner current control loop brings some difficulties for the stability analysis of the variable duty control and the adaptive tuning control.

TABLE 2.1.
COMPARISON OF CONVENTIONAL CONTROL METHODS FOR CCM&DCM.

| Control Methods / Comparison Aspects | Feed forward control | | | | Feedback control | |
|---|---|---|---|---|---|---|
| | Variable duty control | Variable frequency control | Pulse density control | Adaptive tuning control | High gain control | Duty feed forward control |
| Response | X | X | X | Δ | O | O |
| Stability Analysis | Δ | X | X | Δ | O | O |
| Implementation Simplicity | Δ | X | X | Δ | O | Δ |
| Hardware Demand | O | Δ | Δ | Δ | X | O |
| Modulation | PWM | PFM | PFM | PFM | PWM | PWM |
| Noise Filter Design | O | Δ | Δ | Δ | O | O |
| Robustness against Inductance | Δ | X | X | X | X | Δ |

Symbols: O = Good / Simple, Δ = Average, X = Poor / Difficult
PWM = Pulse width modulation, PFM = Pulse frequency modulation

Concerning the implementation simplicity, the high gain control is the simplest method to employ because this method is basically the conventional CCM-only control with high control bandwidth. On the other hand, due to the difficulty in the stability analysis, it is not simple to implement the variable frequency control and the pulse density control, especially in the digital control where the constant sampling frequency is preferred.

Meanwhile, the variable duty control, the adaptive tuning control and the duty feed forward control requires the addition compensation for the DCM operation.

In regard to the hardware demand, the high gain control requires both the high sampling frequency and the zero current detection, resulting the undesirable highest hardware demand. In contrast, the variable duty control and the duty feed forward control can be simply implemented in the same hardware as the conventional CCM-only control. Besides, the variable frequency control, the pulse density control and the adaptive control still require additional circuit to detect the zero current.

In terms of the modulation and the noise filter design, it is simple to design the noise filter for the variable duty control, the high gain control and the duty feed forward control because these methods operates under PWM. On the other hand, PFM are resulted in the variable frequency control, the pulse density control and the adaptive tuning control, complicating the noise filter design.

Finally, regarding the robustness against the inductance, the variable frequency control, the pulse density control, the adaptive tuning control and

the high gain control achieve the current mode determination by the zero current detection, whose operation depends on the inductance; consequently, these control methods have a low robustness against the inductance. On the other hand, then variable duty control use the mode tracker and the relationship between duties, respectively, to determine the current mode, advoiding the use of the inductance in the current mode determination. Nevertheless, these control methods still require the inductance to calculate the steady-state DCM duty.

## 2.5 Proposed Inductance-Independent Control for Continuous and Discontinuous Current Mode

### 2.5.1 Inductance-Independent Control for Continuous and Discontinuous Current Mode with Duty at Previous Calculation Period

Fig. 2.10 depicts the proposed inductance-independent control for the inverter operating in CCM&DCM. The control system is mainly divided into the duty generation and the current mode determination. In the duty generation, both the DCM duty $Duty_{DCM}$ and the CCM duty $Duty_{CCM}$ are generated. The conventional CCM controller compensates for the difference of the duties between the calculation periods. The CCM duty generation is basically as same as that in the conventional CCM-only control, whose function is to compensate for the grid voltage. The DCM duty generation includes the nonlinearity compensation which provides the control system inductance-independence and the same CCM current response when the inverter operates in DCM.

In the current mode determination, the generated CCM and DCM duties are compared to determine the current mode. In particular, if $Duty_{CCM}$ is

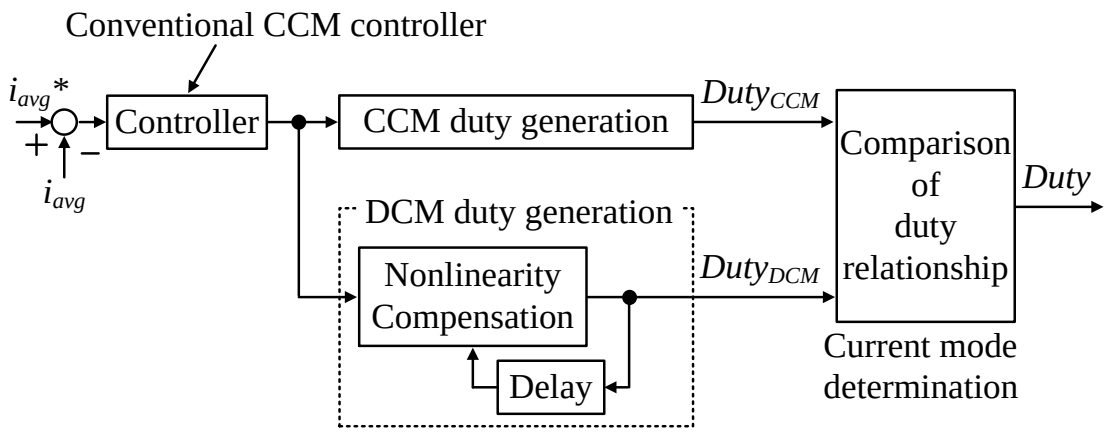



Fig. 2.10. Proposed inductance-independent control for inverter operating in CCM&DCM.

larger than $Duty_{DCM}$, DCM becomes the operation mode and vice versa. In general, $Duty_{CCM}$ is the output value of the controller, which implies the calculation for $Duty_{CCM}$ is independent from the inductance. The calculation for $Duty_{DCM}$ also becomes inductance-independent because the proposed DCM nonlinearity compensation is employed. Consequently, when the relationship between $Duty_{CCM}$ and $Duty_{DCM}$ is used to determine the current mode, the inductance-independent current mode determination is achieved.

The original idea of the inverter control for the operation in both DCM and CCM is that as first step, the duty ratio at the previous calculation period is used to compensate the DCM nonlinearity regardless of the inductance, then two outputs of the inductance-independently generated duty ratios are compared to each other in order to determine the current mode. Consequently,

the CCM&DCM current control system can perform the current control independently from the inductance.

### 2.5.2 Beneficial Position of Proposed Method

Fig. 2.11 depicts the comparison between the proposed control method and the conventional control methods. The y-axis indicates the control bandwidth, whereas the x-axis represents the comparability, which is evaluated by the below factors: stability analysis, implementation simplicity, hardware demand and robustness against inductance. The wide control bandwidth implies the possibility to design the high cutoff frequencies for the current control loop, and vice versa. Meanwhile, the high compatibility

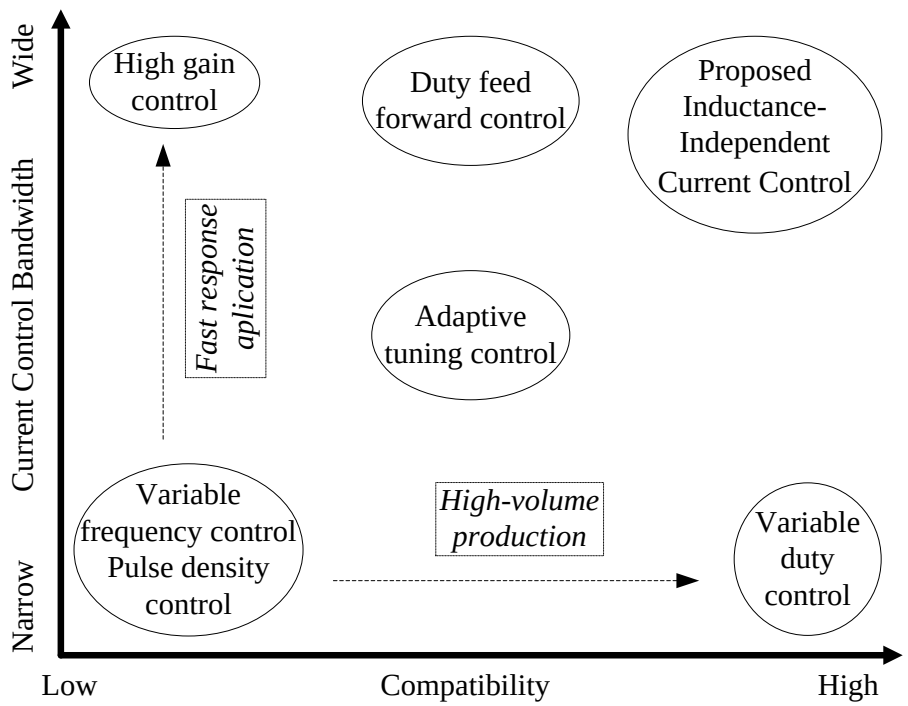



Fig. 2.11. Beneficial position of proposed method compared to conventional methods.

indicates the simpler approach to analyze stability, implementation, the low hardware demand and the stronger robustness against the inductance, and vice versa.

As explained in section 2.3.3, the variable duty control exhibits a simple controller design and implementation; however, the response is slow to ensure the stability even when the mismatch of the plant occurs. Hence, variable duty control is suitable for only slow response application. On the other hand, the high gain control provides wide control bandwidth which is required for applications requiring fast response; nevertheless, high-speed controllers are necessary due to the high sampling frequency. Furthermore, the additional circuit for the zero current detection is also required for the current mode determination. Consequently, the high gain control is unsuitable for the high-volume production.

The proposed inductance-independent control shows superior characteristics which are suitable for both applications requiring fast response and high-volume production simultaneously. The proposed control utilizes the mechanism of the current mode determination in the duty feed forward control, where the relationship between CCM and DCM is used to

determine the current mode without using the inductance; furthermore, the proposed control completely eliminates the inductance dependency of the duty feed forward control in the DCM duty generation by using the duty at the previous calculation period. Consequently, the proposed inductance-independent CCM&DCM control can achieve the same response with the same hardware as the conventional CCM-only control.

## 2.6 Conclusion

In this chapter, numerous control methods for the CCM&DCM operation have been reviewed. The drawbacks of the conventional control are as follows: the requirement of the zero current detection, or the low response to ensure the stability. Many studies have been conducted to improve the response when the converter operates in DCM by increase the control bandwidth or feed forward the steady-state duty. Nevertheless, the control system either becomes independent on the inductance, which worsens the robustness against the inductance, or requires the high-speed controller hardware. The duty feed forward control avoids the zero current detection by using the relationship between CCM and DCM duty to determine the current mode; nevertheless, the inductance is still required in the DCM duty generation.

The proposed control utilizes the mechanism of the current mode determination in the duty feed forward control, and completely eliminates the inductance dependency of the duty feed forward control in the DCM duty generation by using the duty at the previous calculation period, resulting in the achievement of the same response with the same hardware as the

conventional CCM-only control. This makes the proposed control suitable for both applications requiring fast response and high-volume production. The next chapter will explain the mechanism of the proposed inductance-independent CCM&DCM control and demonstrate its superior characteristics.

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# Chapter 3

# Control of Discontinuous Current Mode in Boost Converter

## 3.1 Introduction

This chapter presents a DCM nonlinearity compensation method which is independent from the boost inductance and the load condition. The original idea in this research is that the DCM nonlinearity compensation is constructed by utilizing the duty ratio at the previous calculation period instead of using the circuit parameter. The advantages of the proposed method are as follows: circuit-parameter-independence and short computation time.

This chapter is organized as follows; in section 3.2, the problems of the conventional DCM control are introduced in detail with past works, then in section 3.3 the design of the conventional PI controller is explained

because the proposed DCM control is based on the CCM control with a PI controller, next in section 3.4, the DCM nonlinearity compensation method is proposed as the main part. In addition, in section 3.5, in order to achieve higher efficiency in the boost converter, the simple DCM synchronous switching method is realized based on the proposed DCM current control and is presented. After that in section 3.6, the validity of the proposed DCM nonlinearity compensation method is verified, and the comparisons of the efficiencies and the current-control computation time are demonstrated in order to confirm the effectiveness of the proposed DCM current control. Finally, in section 3.7, the conclusion of this chapter will be presented.

## 3.2 Problems of Conventional Discontinuous Current Mode Control Methods

Typical boost DC-DC converters are widely applied in many power conversion systems, e.g. power conditioning system in photo-voltaic systems. The problem in the typical boost converters is the use of bulky passive components, i.e. an output capacitor and a boost inductor. One of the challenges to minimize the output capacitor is the dynamic voltage regulation during the fast load transient. In the applications for power conditioning system, the output voltage within a tight tolerance range must be maintained during the faults of the grid, i.e. a load current step occurs. The load transient requirement can be met even with small capacitance by a wide bandwidth voltage control [3-1]-[3-2]. On the other hand, many minimization methods for the inductor have been proposed such as high frequency switching, coupled-inductor or flying-capacitor topologies [3-3]-[3-6]. However, higher switching frequency leads to the increase in both the switching loss and the emission noise [3-7], whereas the addition components results in the complexity of the design in the main circuit and the control method.

There are other approaches to minimize the boost inductor in terms of the operation mode. By increasing the current ripple at a given switching frequency, the typical boost converters can be operated in two main current modes; continuous current mode (CCM) and discontinuous current mode (DCM) [3-8]-[3-9]. The advantages of CCM are: simple controller design due to the linear duty-ratio-to-inductor-current transfer function, and the simple average current sampling. On the other hand, the boost converter with the DCM operation achieves the high efficiency over a wide load range because the current ripple in DCM decreases at light load. Nonetheless, the nonlinear duty-ratio-to-current transfer occurs in DCM, which worsens the current control performance when the same controller as in CCM is used. In particular, the effects of the DCM nonlinearity on the duty-ratio-to-current transfer function changes according to the current load [3-10]. This results in the overcurrent when the current is regulated by a wide bandwidth controller [3-11]. In past few years, many researches focusing on the control of DCM have been reported to solve this problem [3-12]-[3-17]. However, in those control methods, the DCM nonlinearity compensation method becomes circuit-parameter-dependent. Due to this

problem, a wide bandwidth current control is still difficult to be applied into DCM. Consequently, the bandwidth of the voltage control cannot be increased in order to minimize the output capacitor [3-18], which restricts the circuit minimization.

Fig. 3.1 shows the typical boost converter configuration. In order to minimize the boost converter at the given switching frequency, this paper proposed the concept where the boost inductor is minimized by the DCM operation and the output capacitor is minimized by the wide bandwidth voltage control in DCM. In other words, at the given switching frequency,

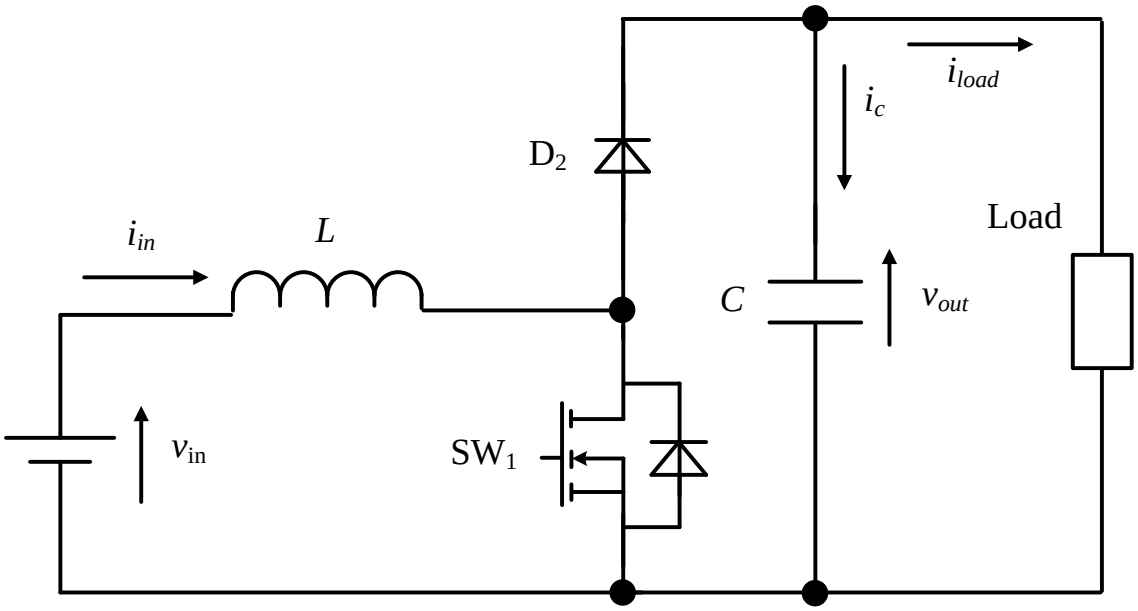
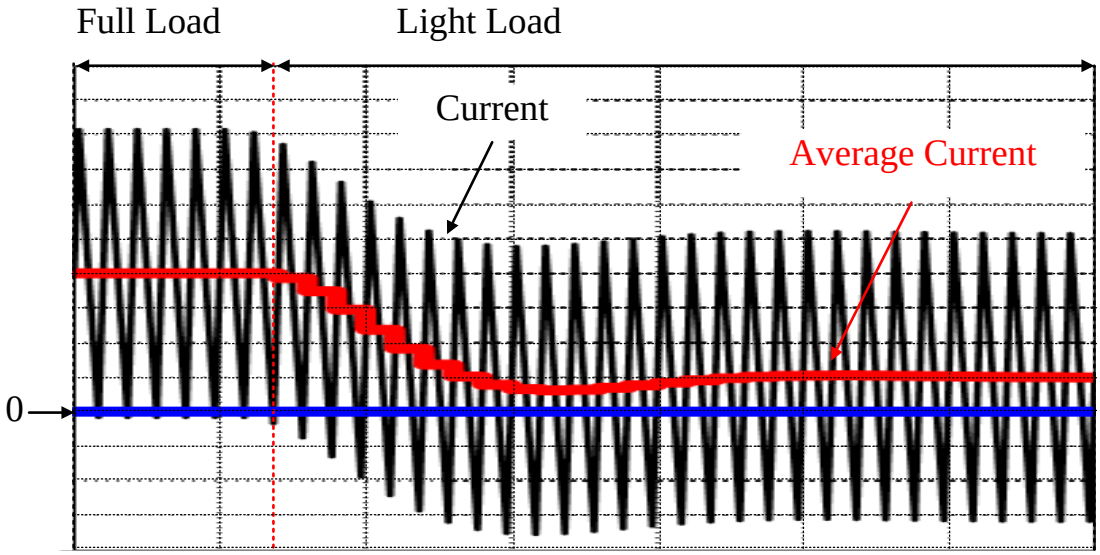


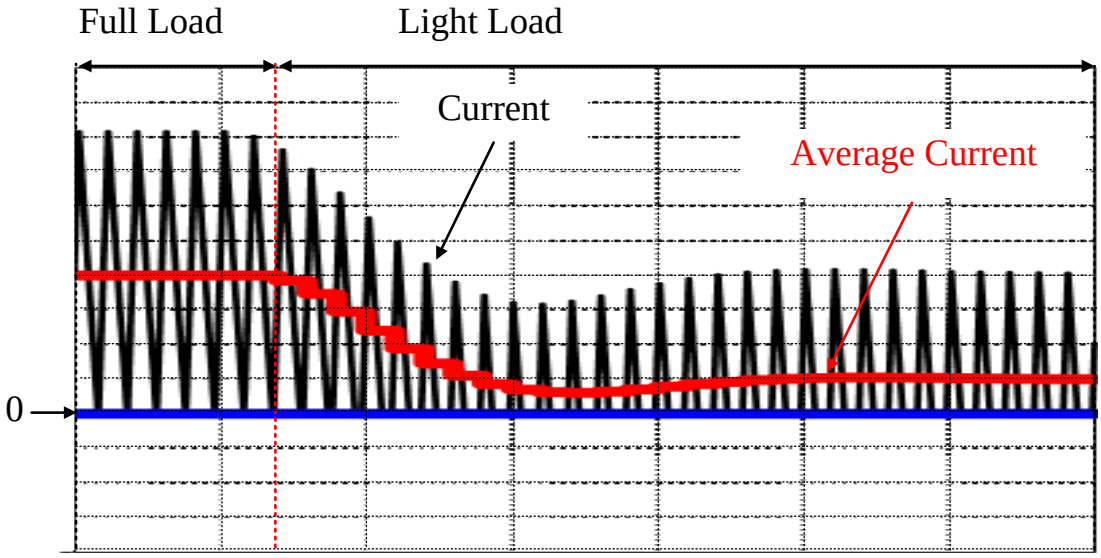

Fig. 3.1. Circuit diagram of typical boost converter. This research proposes the concept where the boost inductor is minimized by DCM and the output capacitor is minimized by the wide bandwidth voltage control in DCM.

the boost converter can achieve higher power density by the application of DCM. Note that the high current ripple in DCM can be overcome simply with the interleaved boost converter topologies as shown in [3-8]-[3-9].

Fig. 3.2 illustrates the current waveforms of CCM and DCM when the inductance is reduced at the given switching frequency. Note that the boost converter is designed to be operated at critical current mode (CRM) at full load and the constant switching frequency is applied over all load range, i.e. the requirement to apply the pulse-width modulation. At light load, the boost inductor current becomes discontinuous. Consequently, the transfer function becomes nonlinear and this leads to the instability of the current control [3-10]. In order to avoid the discontinuous current, the switch is used instead of the upper diode. The CCM synchronous switching by applying this switch improves the efficiency at full load and maintains the continuity of the current. However, the current ripple becomes much higher than the average current at light load. This results in the poor power conversion efficiency at light load. On the other hand, the current ripple in DCM decreases at light load as shown in Fig. 3.2(b). Hence, when the converter is operated in DCM, the high efficiency is expected to be




(3.2.a) Continuous current mode at light load




(3.2.b) Discontinuous current mode at light load

Fig. 3.2. Inductor current waveform of CCM and DCM when the inductance is minimized at given switching frequency. At light load, the constant current ripple of CCM increases the ratio between the average current and the current ripple, whereas the current ripple of DCM decreases. Therefore, the high efficiency at wide load range with DCM is achievable.

maintained over wide load range.

The current control for DCM is generally divided into two main

methods: feedforward control and feedback control. The principle of the DCM current feedforward control is to design the controller based on the reduced-order model or the full-order model [3-9], [3-12]. An advantage of the feedforward control is the unrequired current sensor. However, the mismatch between the nominal values and the actual values of the circuit parameters results in the instability of the control system when a wide bandwidth control is applied [3-11], [3-18]. On the other hand, the feedback control in DCM has to deal with the nonlinear duty-to-current transfer function [3-10]. In [3-13] and [3-17], the PI controller with constant coefficients is used in order to control DCM. The DCM nonlinearity, however, implies that the duty-ratio-to-inductor-current transfer function depends on the load. With a constant-coefficient PI controller, the cutoff frequency of current controller varies dependently on load, which results in the instability of the control system when the load varies. In order to deal with the DCM nonlinearity and also avoid the PI controller design with online-tuning coefficients, the hybrid control between the feedforward control and feedback control has been proposed in [3-15]-[3-16]. The principle of these control methods is to estimate the duty

ratio from the current command, then feed forward this estimated duty ratio to compensate for the DCM nonlinearity. In [3-15], the estimated duty ratio is calculated by a complex function based on the reduced-order model as same as [3-9], [3-12]. In [3-16], the calculation time is reduced by estimating the duty ratio through a reference table.

However, the penalties of these control methods are as follows; the control system becomes circuit-parameter-dependent and a long computation time is required. In case of the power conditioning system application, the boost converter is usually required to deal with the severe change of the ambient environment, where the circuit condition such as the operation temperature varies frequently. When the actual values of the circuit parameters such as, e.g. inductance and capacitance, are different from the nominal values due to the variation of the circuit condition, the stability of the circuit-parameter-dependent control system can no longer be guaranteed. As the motivation for the achievement of the wide bandwidth DCM current control, it is necessary to realize the DCM nonlinearity compensation with the features as circuit-parameter-independence and short computation time.

## 3.3 PI Controller Design for Continuous Current Mode

This section presents the design of the conventional PI controller for the boost converter because the proposed DCM control is based on the CCM control with a PI controller.

Fig. 3.3 depicts the inductor current waveform in DCM, where $D_1$, $D_2$ and $D_3$ denote the duty ratios of the first, the second and the zero-current interval. Average small signal modeling technique is used to model the boost converter for the inner current control loop design [3-10], [3-16]. The average inductor voltage during a switching period $T_{sw}$ is given by (3.1),

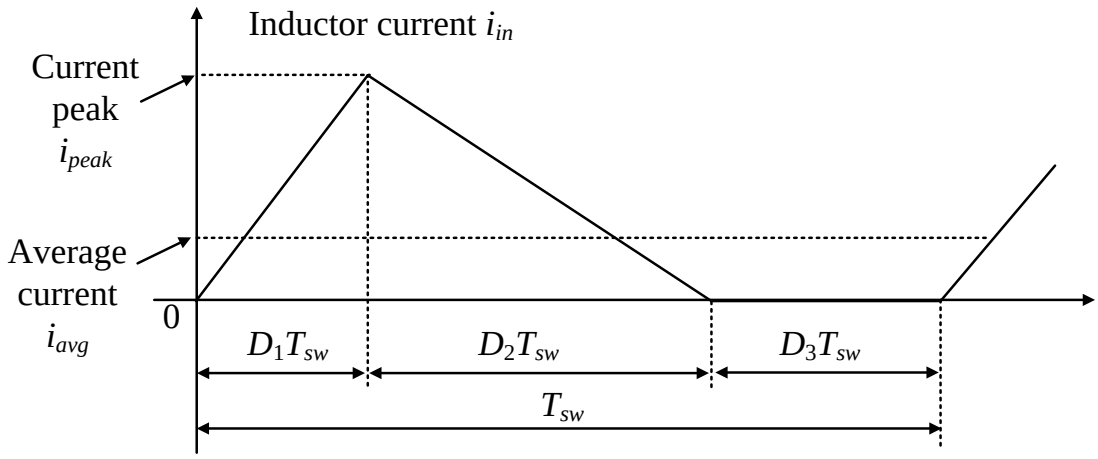



Fig. 3.3. Inductor current waveform in DCM. The zero current interval occurring in DCM introduces the nonlinearity into the duty-to-current transfer function [3-10].

$$L\frac{di_{avg}}{dt} = D_1 v_{in} + D_2\left(v_{in} - v_{out}\right) \quad (3.1)$$

where $v_{in}$ and $v_{out}$ are the instantaneous input voltage and the instantaneous output voltage, $i_{avg}$ is the average inductor current during a switching period $T_{sw}$, and $L$ is the inductance. In case of CCM, the relationship between $D_1$ and $D_2$ becomes,

$$D_1 + D_2 = 1 \quad (3.2)$$

By substituting (3.2) into (3.1) in order to represent (3.1) as a function of only the duty ratio $D_1$, (3.3) is obtained,

$$\frac{L}{v_{out}}\frac{di_{avg}}{dt} = \frac{v_{in} - v_{out}}{v_{out}} + D_1 \quad (3.3)$$

When the boost converter operates in steady state, the output voltage, the input voltage, the average input current and the duty ratio in each switching period $T_{sw}$ can be expressed as,

$$v_{out} = V_{out_s} + \Delta v_{out} \quad (3.4)$$

$$v_{in} = V_{in_s} + \Delta v_{in} \quad (3.5)$$

$$i_{avg} = I_{avg_s} + \Delta i_{avg} \quad (3.6)$$

$$D_1 = D_{1_s} + \Delta D_1 \quad (3.7)$$

where $V_{out_s}$, $V_{in_s}$, $I_{avg_s}$ and $D_{1_s}$ are the output voltage, the input voltage,

the average input current and the duty ratio at steady state, and $\Delta v_{out}$, $\Delta v_{in}$, $\Delta i_{avg}$ and $\Delta D_1$ are the small signals of the output voltage, the input voltage, the average input current and the duty ratio, respectively. In the current design step, the input and output voltages are considered to be at the steady state. Consequently, the small signals of the input voltage and the output voltage, i.e. the input and output voltage dynamics are considered to be negligible. By substituting (3.4)-(3.7) into (3.3), (3.8) is obtained,

$$\frac{L}{V_{out_s}}\frac{d\left(\Delta i_{avg}\right)}{dt}=\frac{V_{in_s}-V_{out_s}}{V_{out_s}}+D_{1_s}+\Delta D_1 \quad \text{.....(8)}$$

The values of the input voltage, the output voltage and the duty-ratio at steady state are determined by letting the left-hand side of differential equation (3.8) and the small signal of the duty ratio $\Delta D_1$ equal to zero,

$$D_{1_s}=\frac{V_{out_s}-V_{in_s}}{V_{out_s}} \quad \text{.....(9)}$$

Substituting (3.9) into (3.8) and applying the Laplace transform, then the duty-ratio-to-inductor-current transfer function in CCM is given by (3.10),

$$G_{CCM}(s)=\frac{\Delta i_{avg}(s)}{\Delta D_1(s)}=\frac{V_{out_s}}{sL} \quad \text{.....(3.10)}$$

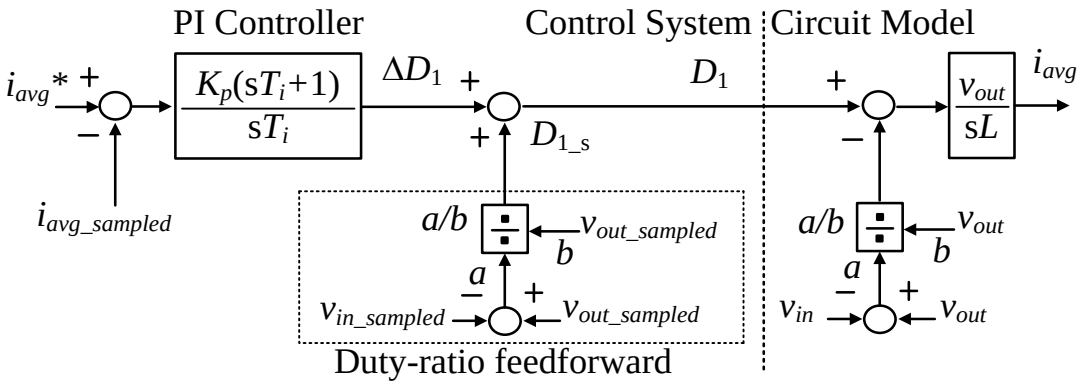



Fig. 3.4. Current control system for CCM. By applying the duty-ratio feedforward in CCM, the PI controller compensates only the small difference between the duty ratio at steady state and the instantaneous duty ratio [3-15].

Fig. 3.4 depicts the current control system in CCM designed based on (3.3) and (3.10). The integral period $T_i$ and the proportional gain $K_p$ of PI controller are designed based on the second-order standard form expressed by (3.11),

$$G_{2nd-order-delay}(s) = \frac{\omega_c^2}{s^2 + 2\zeta\omega_c s + \omega_c^2} \quad \text{.....} (3.11)$$

where $\omega_c$ is the cutoff angular frequency and $\zeta$ is the damping factor, which are designed in order to achieve the desired current response. The closed loop transfer function of the current control loop in Fig. 3.4 is derived by (3.12),

$$H_{CCM}(s) = \frac{i_{avg}(s)}{i_{avg}{}^*(s)} = \frac{\frac{K_p V_{out_s}}{LT_i}(1+sT_i)}{s^2 + \frac{K_p V_{out_s}}{L}s + \frac{K_p V_{out_s}}{LT_i}} \quad \text{.....} \quad (3.12)$$

In order to make the design of PI parameters simple, a low pass filter whose role is to filter the command current $i_{avg}{}^*$ is necessary for matching (3.11) and (3.12). However, a low pass filter is not essentially required. Matching (3.11) and (3.12), the PI parameters are obtained by (3.13) and (3.14),

$$K_p = \frac{2\zeta\omega_c L}{V_{out_s}} \quad \text{.....} (3.13)$$

$$T_i = \frac{2\zeta}{\omega_c} \quad \text{.....} (3.14)$$

The digital PI controller has the same coefficients as the analogous controller. To sum up, the design of the controller is performed in the frequency domain, whereas for the digital implementation, the obtained parameters are linked to the parameters of a digital PI controller [3-15].

## 3.4 Current Control for Discontinuous Current Mode

### 3.4.1 Circuit Model Derivation

In order to design the nonlinearity compensation part for DCM, the circuit model in DCM is required. First, the average current $i_{avg}$ and the current peak $i_{peak}$, which are shown in Fig. 3.3 can be expressed as,

$$i_{avg} = \frac{i_{peak}}{2}(D_1 + D_2) \quad (3.15)$$

$$i_{peak} = \frac{v_{in}}{L} D_1 T_{sw} \quad (3.16)$$

Substituting (3.16) into (3.15) and solving the equation for the duty ratio $D_2$, then the duty ratio $D_2$ is expressed by (3.17),

$$D_2 = \frac{2Li_{avg}}{D_1 T_{sw} v_{in}} - D_1 \quad (3.17)$$

Substituting (3.17) into (3.1) to remove $D_2$ and representing (3.1) as a function of only the duty ratio $D_1$, (3.18) is obtained [3-10].

$$L\frac{di_{avg}}{dt} = v_{in} - v_{out} + D_1 v_{out} + (v_{out} - v_{in})\left(1 - \frac{2Li_{avg}}{v_{in} D_1 T_{sw}}\right) \quad (3.18)$$

Then, the circuit model in DCM is established based on (3.18).

Fig. 3.5 illustrates the circuit model of the boost converter in the DCM operation which is based on (3.18). In CCM, the dash line part does not exist, because the average current $i_{avg}$ equals to the half current peak $i_{peak}/2$.

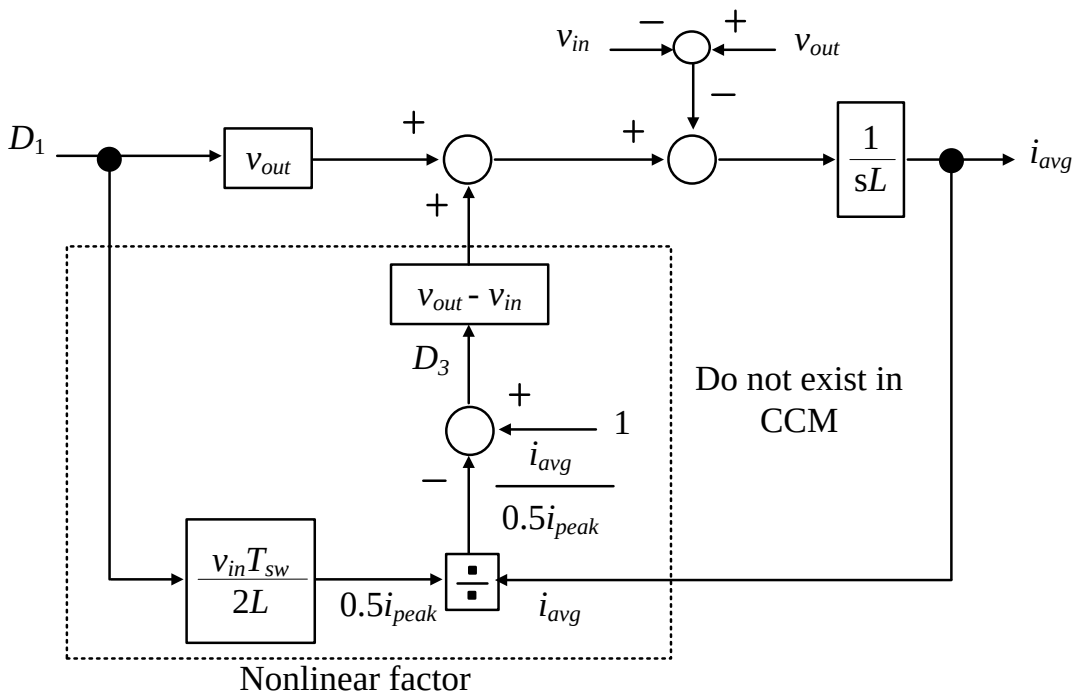



Fig. 3.5. Circuit model of boost converter operated in DCM. The zero-current interval $D_3T_{sw}$ introduces the nonlinearity into the DCM transfer function, which worsens the current control performance.

On the other words, this makes the zero-current interval $D_3T_{sw}$ in Fig. 3.3 become zero. However, in DCM, the zero-current interval introduces the nonlinearity into the DCM transfer function. This worsens the current response in DCM when same PI controller is applied for both CCM and DCM [3-10], [3-15]. Therefore, the output of the PI controller is necessary to be compensated when the circuit is operated in DCM. The design of the compensation part for the DCM nonlinearity is explained as follows. First, the circuit model in Fig. 3.5 is linearized at steady state.

### 3.4.2 Nonlinearity Compensation with Duty Ratio at Previous Calculation Period

Fig. 3.6 depicts the linearized circuit model. In order to simplify the coefficients in the linearized circuit model, the relationships between such coefficients at steady state are derived by substituting the differential of the inductor current d$i_{avg}$/d$t$ in (3.18) as zero and calculating the current peak,

$$I_{avg_s} = \frac{T_{sw}}{L}\frac{D_{1_s}^{2}}{2}\frac{V_{in}V_{out}}{V_{out}-V_{in}} \quad \text{.....(3.19)}$$

$$I_{peak_s} = \frac{V_{in}}{L}D_{1_s}T_{sw} \quad \text{.....(3.20)}$$

where $I_{avg_s}$, and $I_{peak_s}$ are the average current and the peak current at steady state, respectively. Then, (3.19) and (3.20) are substituted into Fig. 3.6 in order to express all coefficients as functions of $D_{1_s}$.

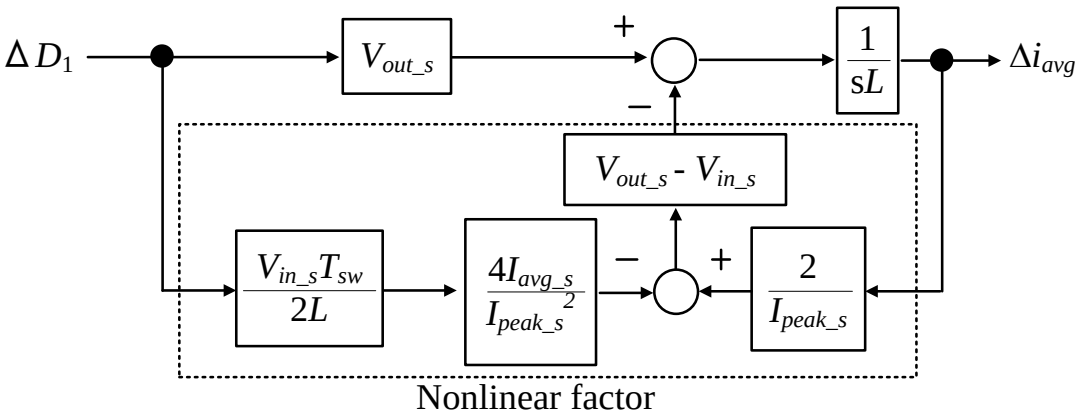



Fig. 3.6. Linearized circuit model. Controlling DCM by PI controller of CCM is achieved by compensating the DCM nonlinearity at the PI output.

Fig. 3.7 depicts the simplified circuit model. In order to eliminate the dash line part in Fig. 3.5, in the control system, the value of $D_{1_s}$ is approximated as the duty ratio of $SW_1$ at the previous calculation period $D_{1[n-1]}$. As a result, the circuit model is necessary to be analyzed in the discrete model.

Fig. 3.8 depicts the discretized circuit model. In order to compensate the DCM nonlinearity at the output of the PI controller designed in CCM, the dash line part in Fig. 3.8 is necessary to be set as 1 when the circuit is operated in DCM. Therefore, in the control system, the inverse part of the dash line part in Fig. 3.8 is multiplied at the output of the PI controller in order to compensate for the DCM nonlinearity.

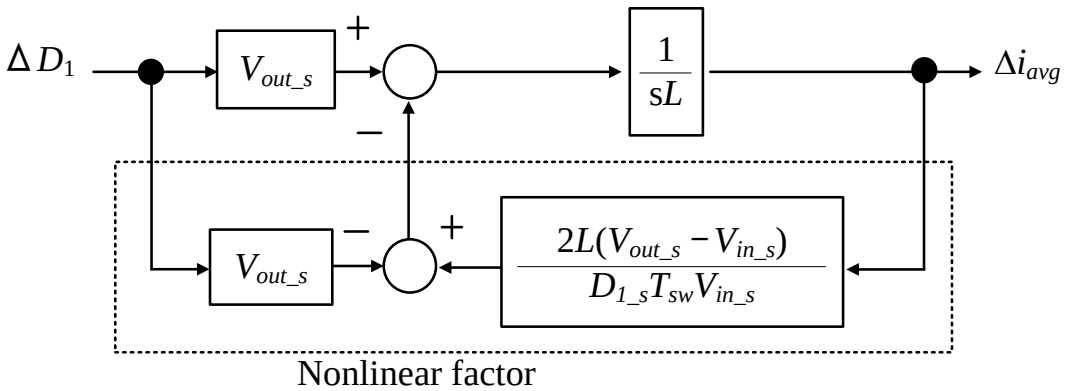



Fig. 3.7. Simplified and linearized circuit model. The duty ratio at steady state in the circuit model is approximated as the duty ratio at previous sampling period in order to eliminate the DCM nonlinearity.

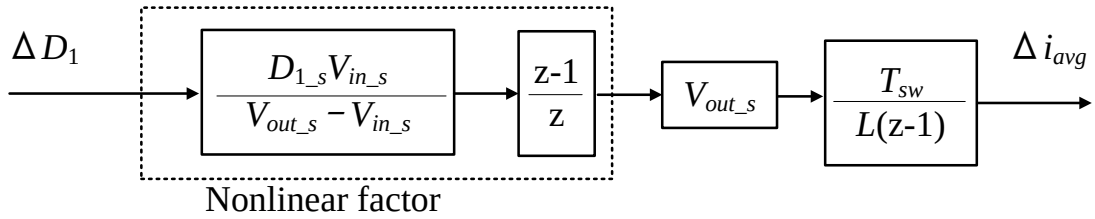
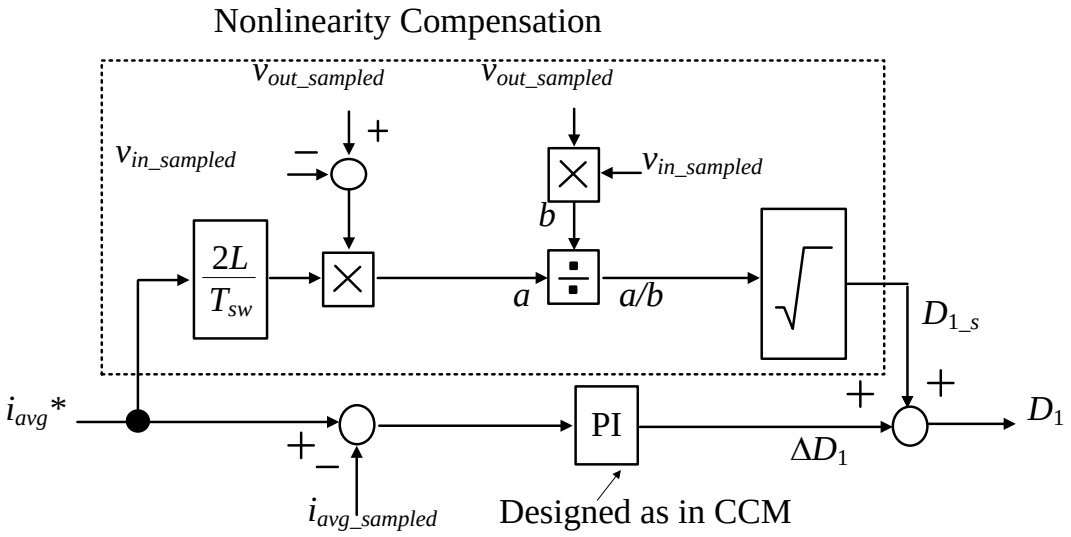
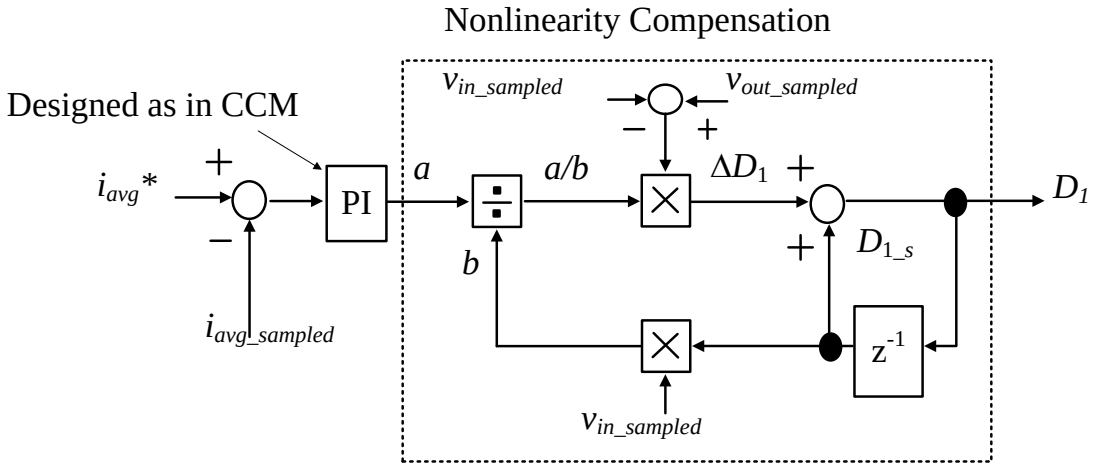



Fig. 3.8. Discretized circuit model. Utilizing the duty ratio at previous sampling period in order to eliminate the DCM nonlinearity makes the current control independent from inductance.

Fig. 3.9 illustrates the conventional DCM nonlinearity compensation in [3-15]-[3-16], and the proposed DCM nonlinearity compensation. Note that the PI controllers in both the conventional and proposed method are designed by (3.13)-(3.14). Besides, in the power conditioning system application, the sampled input voltage which is used for the maximum power point tracking can be also used for the DCM nonlinearity compensation. The principle of two methods is the estimation of the duty ratio at steady state in order to compensate for the DCM nonlinearity. In the conventional method, the duty ratio at steady state is estimated by using current command $i_{avg}^*$ and (3.19). This leads into many disadvantages: circuit-parameter-dependence, and long computation time. On the other hand, in the proposed method, the duty ratio at steady state is estimated by utilizing the duty ratio at the previous calculation period. This provides the




(3.9.a) Conventional DCM nonlinearity compensation in [3-15]-[3-16]




(3.9.b) Proposed DCM nonlinearity compensation

Fig. 3.9. Conventional and proposed DCM nonlinearity compensation. The main difference in the proposed method is that, the DCM nonlinearity compensation is constructed by utilizing the duty ratio at the previous calculation period. This makes the control system circuit-parameter-independent and achieves the fast computation of the current control.

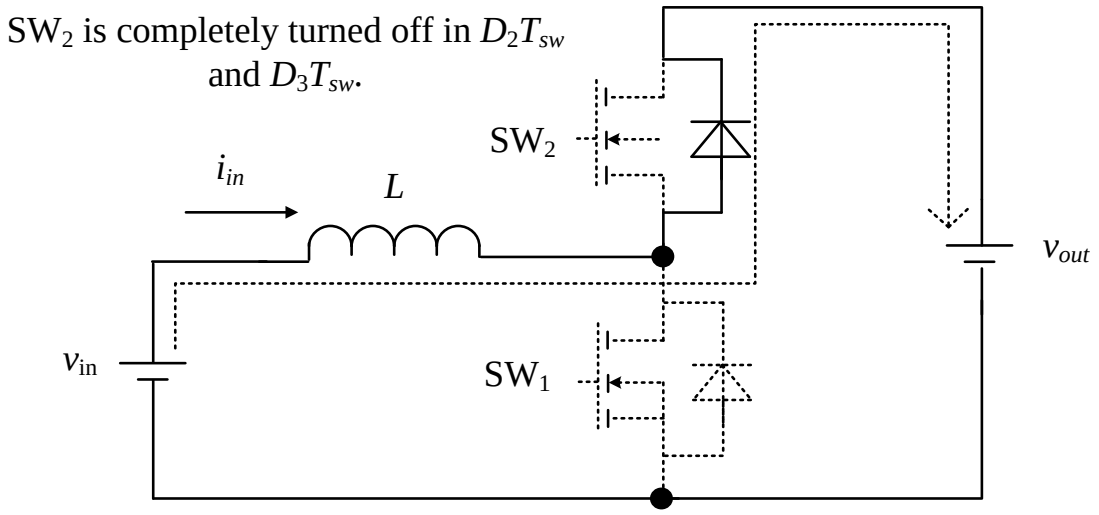
control system circuit-parameter-independence, and short computation time.

Moreover, because the dash-line part in Fig. 3.9(b) is always the inverse part of the nonlinear factor in Fig. 3.8 by utilizing the duty ratio at the previous calculation period, the DCM nonlinearity is eliminated over entire load range.

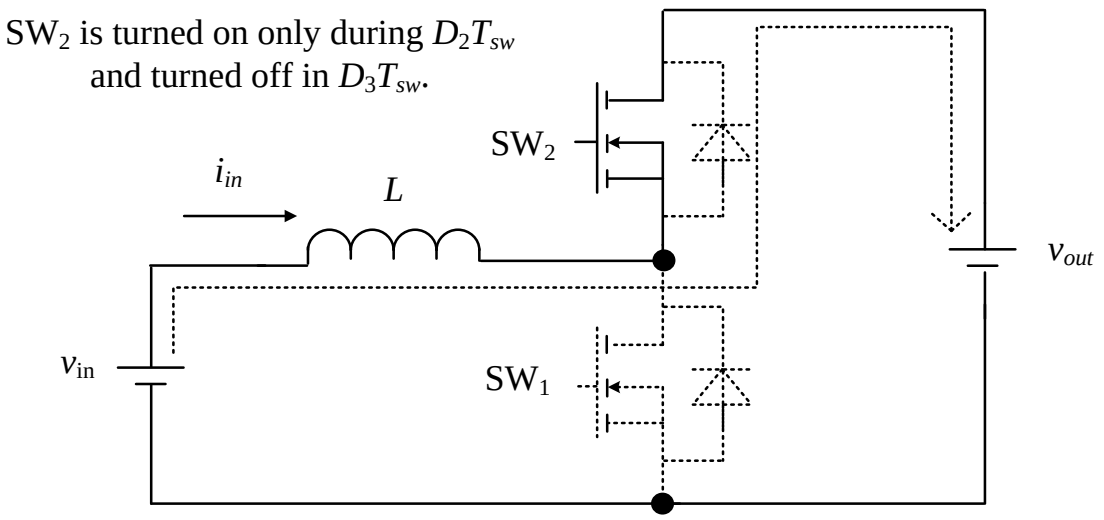
## 3.5 Synchronous Switching in Discontinuous Current Mode

Fig. 3.10 depicts two switching patterns which occur in DCM when the switch (MOSFET) is used instead of the upper diode. This converter can improve the efficiency because the conduction loss of MOSFET is smaller than that of diode. This converter can realize three operation modes at light load depending on the turn on and off of $SW_2$; i) Simple CCM synchronous switching in which $SW_2$ is switched alternately to $SW_1$, ii) DCM asynchronous switching in which $SW_2$ is turned off at light load and iii) DCM synchronous switching in which $SW_2$ is turned on only during the period $D_2T_{sw}$ as depicted in Fig. 3.3.

The boost inductor current of the simple CCM synchronous switching becomes continuous. Therefore, the boost inductor current ripple is constant. However, the boost inductor current increases at light load compared to that of the conventional circuit which is shown in Fig. 3.2. In order to improve the efficiency at light load, the DCM asynchronous switching is applied. Although the DCM asynchronous switching can reduce the boost inductor current in light load, the conduction loss of the




(3.10.a) Asynchronous switching




(3.10.b) Synchronous switching

Fig. 3.10. Asynchronous switching and synchronous switching in DCM. The loss reduction is achieved by applying synchronous switching to DCM.

body diode in the MOSFET is still high. In the DCM synchronous switching, in case that $SW_2$ is turned on exactly only in period $D_2T_{sw}$, the current flows through MOSFET. As a result, the conduction loss is reduced.

The main key of the DCM synchronous switching technique is to detect or estimate the moment when the current reaches zero in order to turn off $SW_2$. The zero-current period can be detected by comparing the detected current with a threshold value [3-17] or by the modified Gate Drive Unit (GDU) in [3-19]. However, both techniques suffers following penalties; the experimental tuning of the threshold value in the current detection or the complex GDU. In order to realize the DCM synchronous switching without any modifications of the main circuit, the duty ratio $D_2$ is calculated by (3.21) in the proposed DCM feedback control and (3.22) in the conventional DCM feedforward control [3-9], respectively,

$$D_{2_prop._fb} = D_1 \frac{v_{in}}{v_{out} - v_{in}} \quad \text{.....} \quad (3.21)$$

$$D_{2_conv._ff} = \sqrt{\frac{2Li^*_{avg}(v_{out} - v_{in})}{T_{sw} v_{in}^2}} \frac{v_{in}}{v_{out} - v_{in}} \quad \text{.....} (3.22)$$

Table 3.1 illustrates the duty generation of the DCM asynchronous switching and the DCM synchronous switching. Because of the mismatch between the nominal values and the actual values, the duty ratio calculated from the feed forward control method in (3.22) makes $SW_2$ turn off too early or too late when the inductor current reaches zero. This leads to the

TABLE 3.1.
DUTY GENERATION OF DCM ASYNCHRONOUS SWITCHING AND DCM SYNCHRONOUS SWITCHING.

| | Asynchronous Switching | Synchronous Switching |
|---|---|---|
| Duty-to-$SW_1$ | $D_1$ | $D_1$ |
| Duty-to-$SW_2$ | 0 | $\frac{D_1 v_{in}}{v_{out} - v_{in}}$ |

increase of the switching losses and the conduction losses. On the other hand, the duty ratio $D_1$ calculated from the feedback control method in (3.21) represents precisely for the value of the inductor current. This enables $SW_2$ to be turned off exactly at the moment when the inductor current reaches zero, which results in Zero Current Switching (ZCS).

## 3.6 Experimental Results

Table 3.2 shows the parameters of circuit and controllers in experiments. While the proposed DCM compensation is applicable for the boost converter at any power rate and any switching frequency, a boost converter is designed for a specific switching frequency at 20 kHz due to the

TABLE 3.2.
PARAMETERS OF CIRCUIT AND CONTROLLERS IN EXPERIMENTS.

| Symbol | Quantity | Value |
|---|---|---|
| $V_{in}$ | Input Voltage | 180 V |
| $V_{out}$ | Output Voltage | 280 V |
| $P$ | Rated Output Power | 360 W |
| $f_{sw}$ | Switching Frequency | 20 kHz |
| | Frequency Analysis Simulation & Current Step Response − Load Transient Response Experiment | |
| $\Delta i_{HCR}$ | Current Ripple at Rated Load | 100% (High) |
| $\Delta i_{LCR}$ | Current Ripple at Rated Load | 10% (Low) |
| $L_{HCR}$ | High Current Ripple Inductance | 655 μH |
| $L_{LCR}$ | Low Current Ripple Inductance | 6680 μH |
| $i_{ac}$ | Injected AC current (Magnitude) | 0.5 A (0.25 p.u.) |
| $f_{iac}$ | Injected AC current (Frequency) | 0.1-5 kHz |
| $v_{ac}$ | Injected AC voltage (Magnitude) | 0.1 p.u. |
| $f_{vac}$ | Injected AC voltage (Frequency) | 0.1-100 kHz |
| $i_{dc}$ | Offset of AC current command | 1.25 A |
| $f_c$ | Cutoff frequency (Current Con.) | 2 kHz |
| $\zeta_c$ | Damping factor (Current Con.) | 0.707 |
| $C$ | Output Capacitance | 33 μF |
| $f_v$ | Cutoff frequency (Voltage Con.) | 0.2 kHz |
| $\zeta_v$ | Damping factor (Voltage Con.) | 0.707 |
| | Efficiency Comparison | |
| | Switching device | TPH3006PS (Transphorm) |

computation time limitation of the low cost controller. Besides, the sampling method for the instantaneous average current in DCM which has been described thoroughly in [3-15]-[3-16] is also applied simply in the proposed DCM current control.

### 3.6.1 Frequency Analysis, Current Step Response and Load Transient Response

Fig. 3.11 illustrates the frequency characteristics of the conventional and proposed DCM current feedback control as shown in Fig. 3.9. From Table 3.2, it is noted that the magnitude of the injected AC current command is 0.25 p.u., which can be considered as a large signal. This makes the elimination of nonlinearity in DCM by the proposed control be confirmed not only in the small-signal model but also in the large-signal model. Besides, the designed gain in Fig. 3.11 is calculated from the discretized second-order standard form which is derived from (3.11). Note that the frequency analysis is conducted in the simulation in order to confirm the cutoff frequency between the conventional and proposed DCM current feedback control. As shown in Fig. 3.11, the frequency characteristic of the

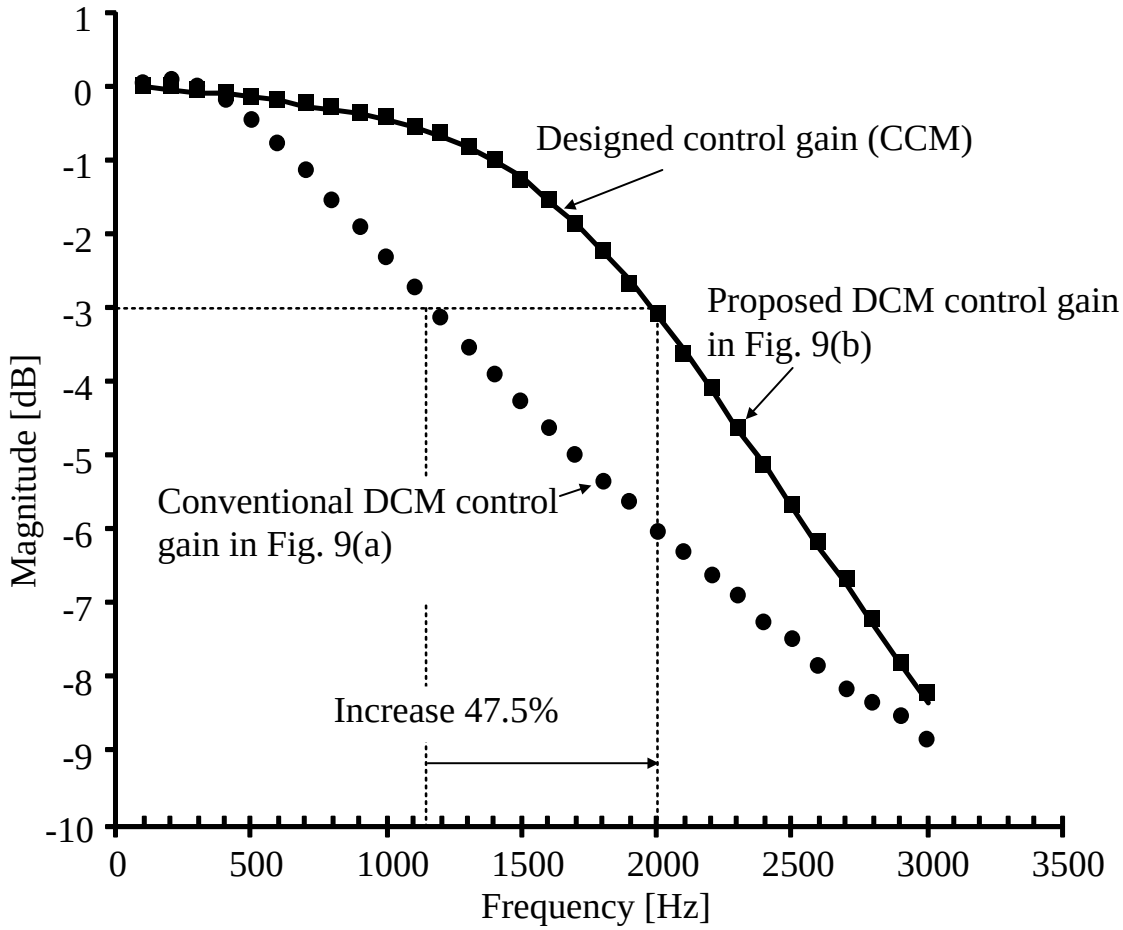



Fig. 3.11. Frequency characteristics of conventional and proposed DCM current feedback control. The agreement between the proposed DCM control gain and the designed gain confirms the complete elimination of the DCM nonlinearity, whereas the conventional DCM control gain results in high error of 47.5%.

proposed DCM control agrees exactly with the designed values (CCM), whereas the cutoff frequency of the conventional DCM control results in high error of 47.5%. Furthermore, the relationship between the cutoff frequency of the outer voltage control loop and the output capacitance is expressed as (3.23) [3-1],

$$C = \frac{\Delta I_{load}}{2\pi V_{overshoot} f_v} \quad \text{.....} (3.23)$$

where $C$ is the output capacitance, $\Delta I_{\text{load}}$ is the load current variation, $V_{overshoot}$ is the overshoot voltage during the load transient variation and $f_v$ is the cutoff frequency of the outer voltage control loop. It can be understood from (3.23) that, under the same condition of the load current variation $\Delta I_{\text{load}}$ and the overshoot voltage $V_{overshoot}$, the output capacitance can be minimized by a wide voltage control bandwidth. Besides, the cutoff frequency $f_v$ of the outer voltage control loop depends linearly on the cutoff frequency of the inner current control loop [3-18]. Hence, the bandwidth of the outer voltage control loop can be improved by 47.5% with the proposed DCM current control comparing to the voltage control bandwidth of the conventional DCM current control. As a result, the output capacitance $C$ can be minimized by 47.5% with the proposed DCM current control.

In this chapter, the implementation of the proposed DCM nonlinearity is carried out by the simplified model as shown in Fig. 3.6, in which the complete model in Fig. 3.5 is linearized and the small signal of the output voltage, i.e. the output voltage dynamic is neglected. This simplification can be considered to be reasonable in PFC applications where the output

capacitor is designed based on the line frequency. However, for DC-DC conversion applications, the output voltage dynamic has to be considered in the DCM nonlinearity compensation. Therefore, AC voltages at different frequency are injected into the output voltage in order to investigate the simplification of the output voltage dynamic in the proposed DCM nonlinearity compensation.

Fig. 3.12 depicts the frequency characteristics of the closed-loop transfer function between average inductor current and its reference, when the proposed DCM nonlinearity compensation is implemented, using the simplified model and the complete model that includes also the output voltage dynamic. It is understood from Fig. 3.12 that a resonance occurs due to the second-order nature of the transfer function between the duty-ratio and the inductor current [3-10]. Apart from that, the maximum gain difference between the simplified model and the complete model is below 0.5 dB. Consequently, in the proposed DCM nonlinearity compensation, the output capacitor is required to be designed so that the frequency of the output voltage dynamic is much higher than the cutoff frequency of the current control loop.

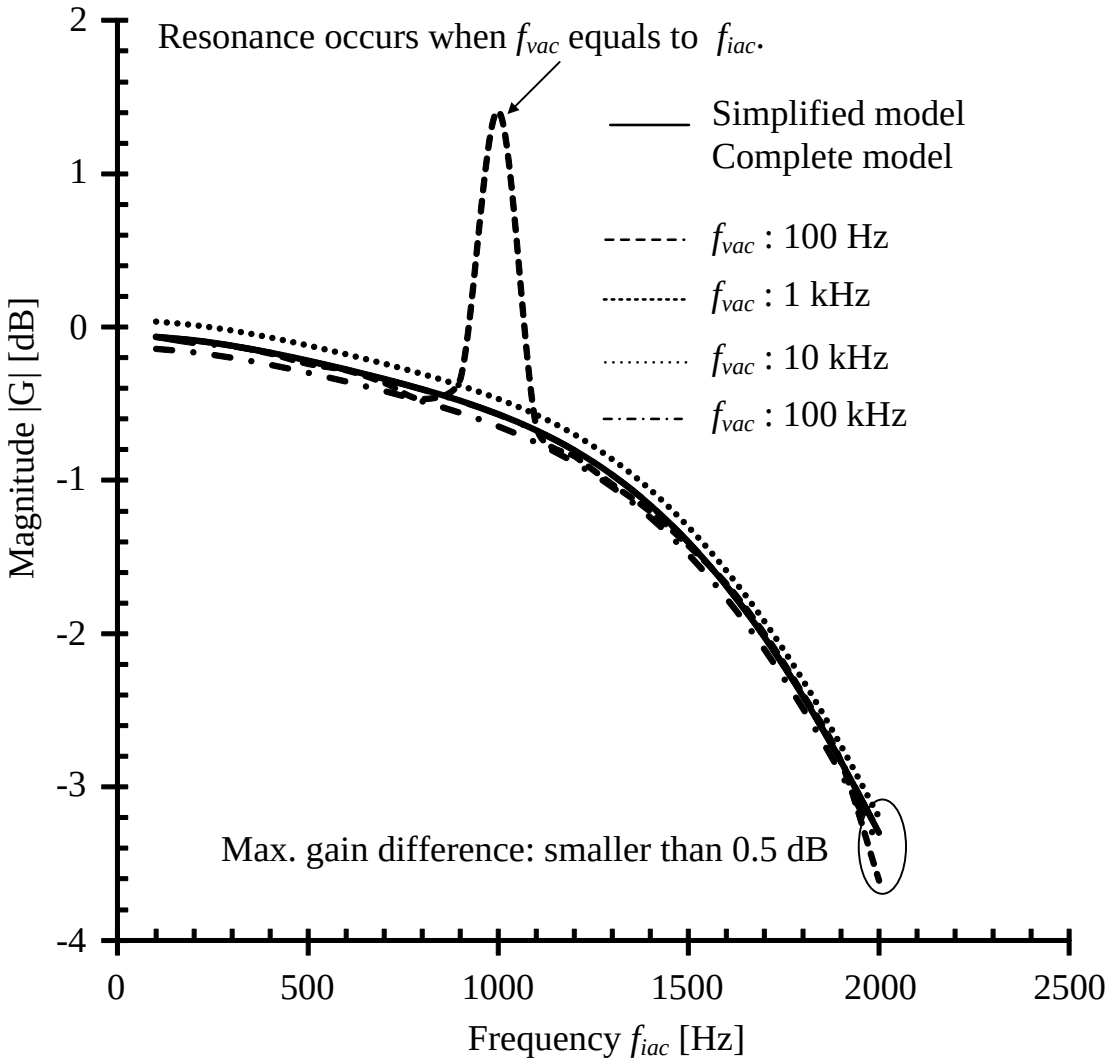
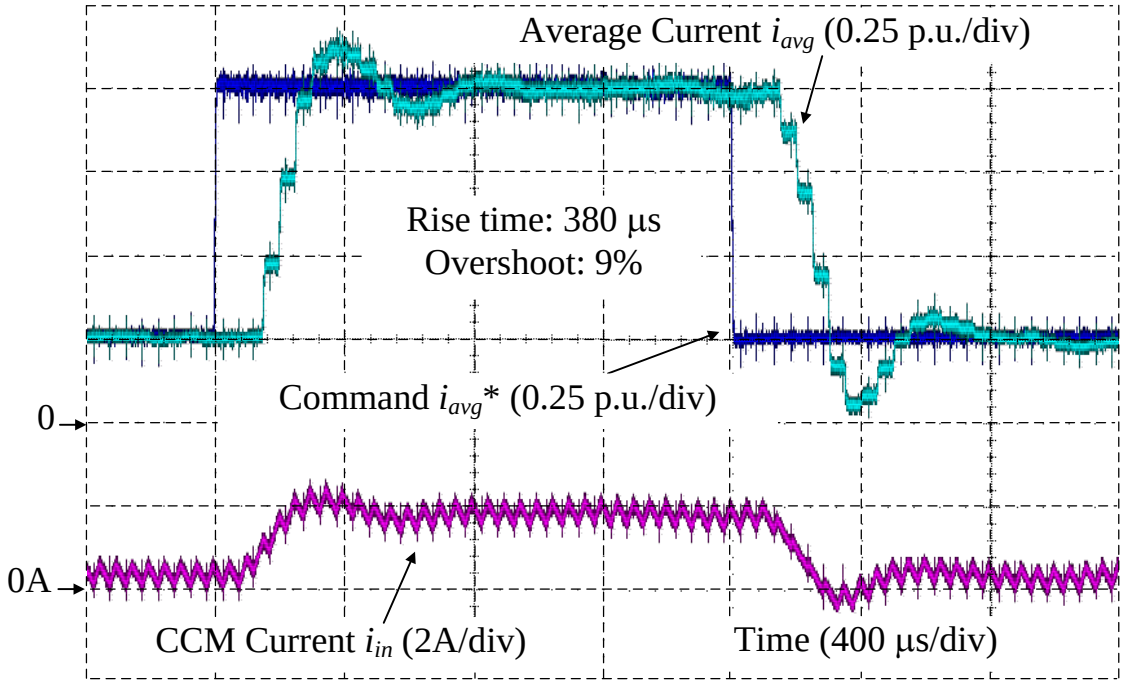
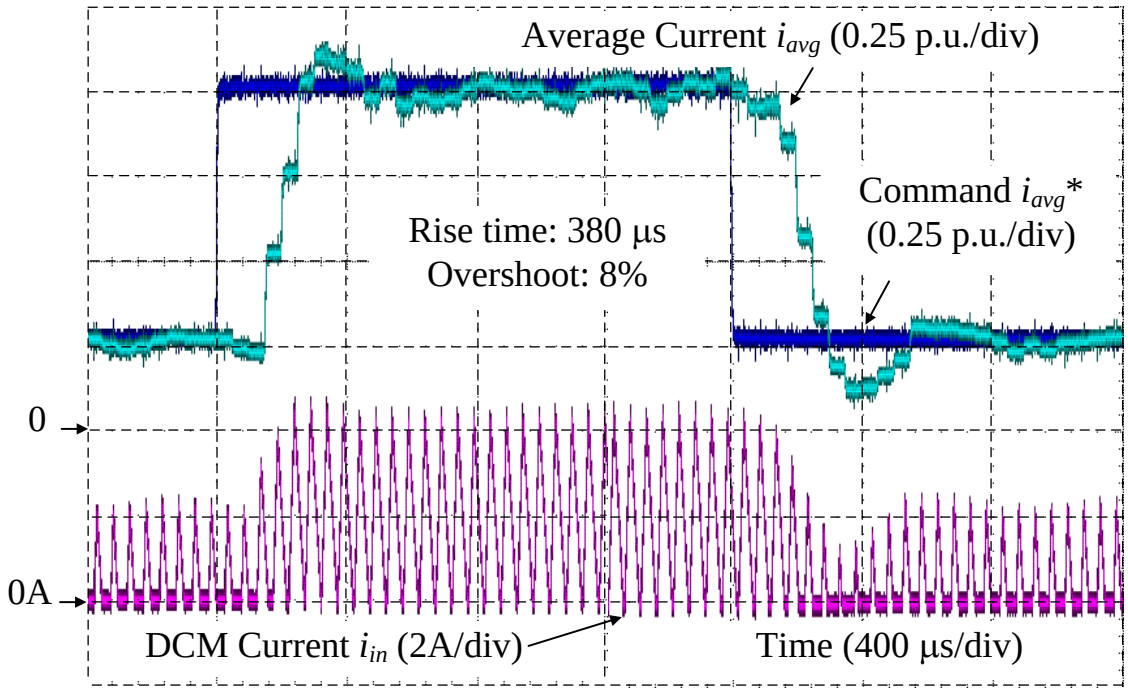



Fig. 3.12. Frequency characteristics of closed-loop transfer function between average inductor current and its reference using simplified model and complete model that includes also output voltage dynamic. The resonance occurs due to the second-order nature of the transfer function between the duty-ratio and the inductor current. Apart of that, the maximum gain difference between the simplified model and the complete model is smaller than 0.5 dB.

Fig. 3.13 illustrates the current step response obtained in experiment by




(3.13.a) Conventional CCM current response

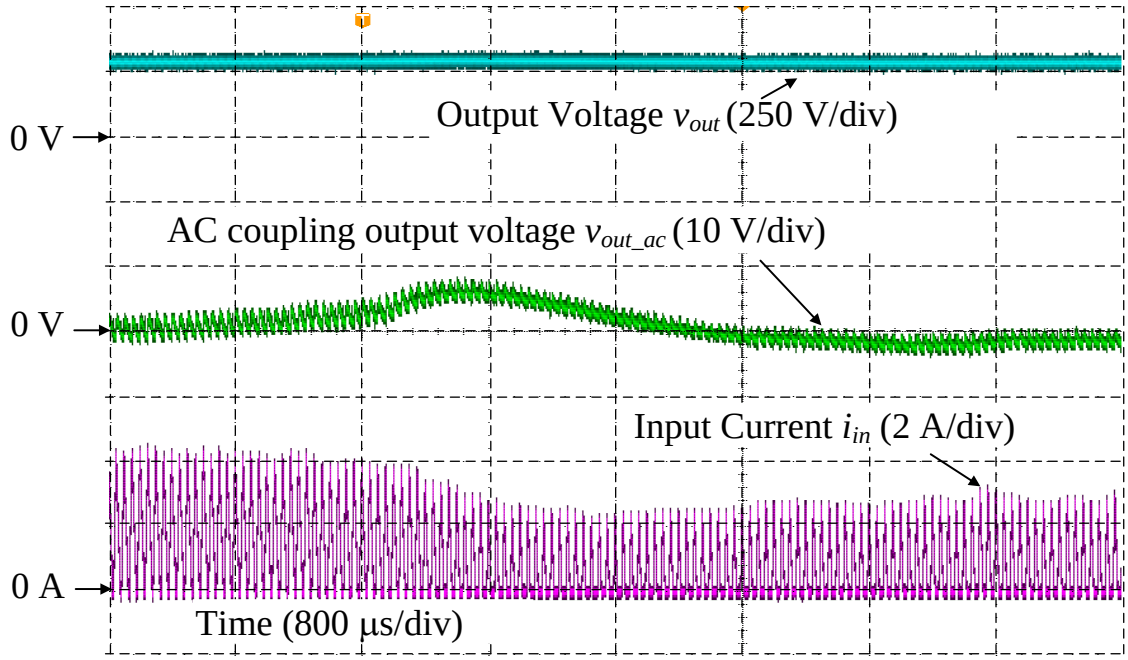



(3.13.b) Proposed DCM current response

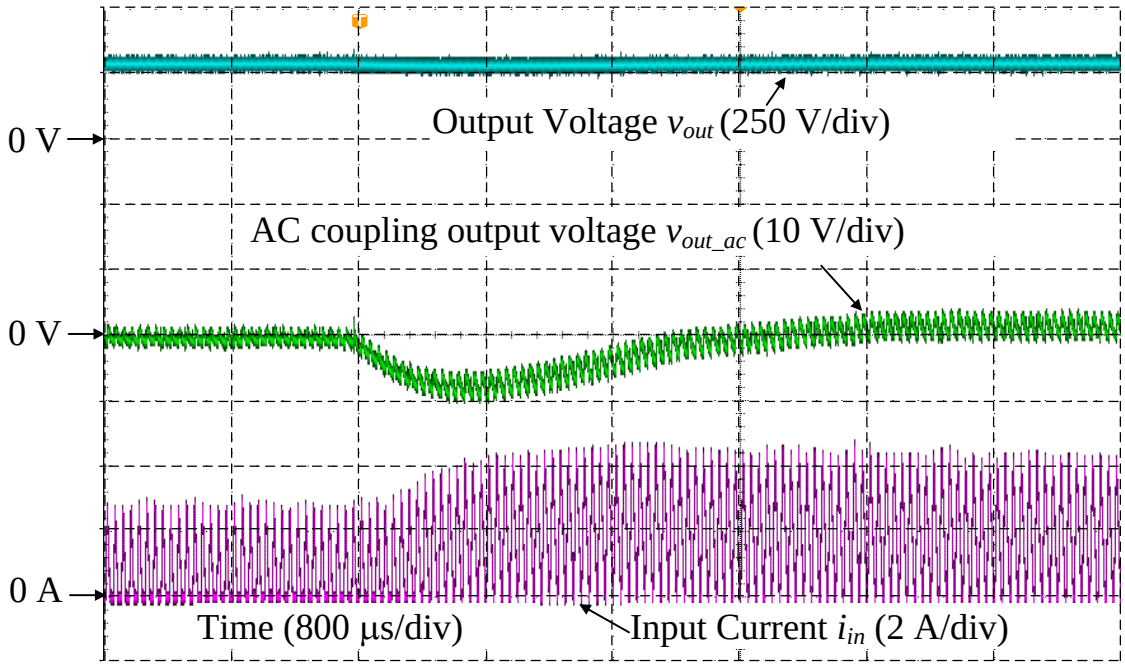
Fig. 3.13. Current step response by input current control with 2-kHz cutoff frequency in CCM and DCM. The DCM current response almost agrees with the conventional CCM current response.

the input current control with 2-kHz cutoff frequency at the switching frequency of 20 kHz. It is concluded that the DCM current response almost agrees with the conventional CCM current response. This confirms the validity of the proposed DCM nonlinearity compensation by experiment. Furthermore, the DCM nonlinearity compensation part is designed independently from the PI controller. Therefore, in order to further improve the performance of the DCM current control, the PID controller or the IP controller, which have been researched thoroughly for CCM operation, can be applied simply. Note that when the boost converter operates in CRM, the proposed DCM control can still be applied. However, the DCM nonlinearity compensation is required to be deactivated when the boost converter operates in CCM.

Fig. 3.14 shows the load transient response obtained in experiment by the output voltage control with 0.2-kHz cutoff frequency. The test is conducted with the load current step from 0.4 p.u. to 1 p.u. and vice versa. The overshoot voltage and the settling time are 9 V and 1660 μs, the errors of which compared to the designed values are 4.3% and 1.6%, respectively. The stability of the voltage control in the proposed DCM control is similar




(3.14.a) Load step change: 1.0 p.u. to 0.4 p.u.




(3.14.b) Load step change: 0.4 p.u. to 1.0 p.u.

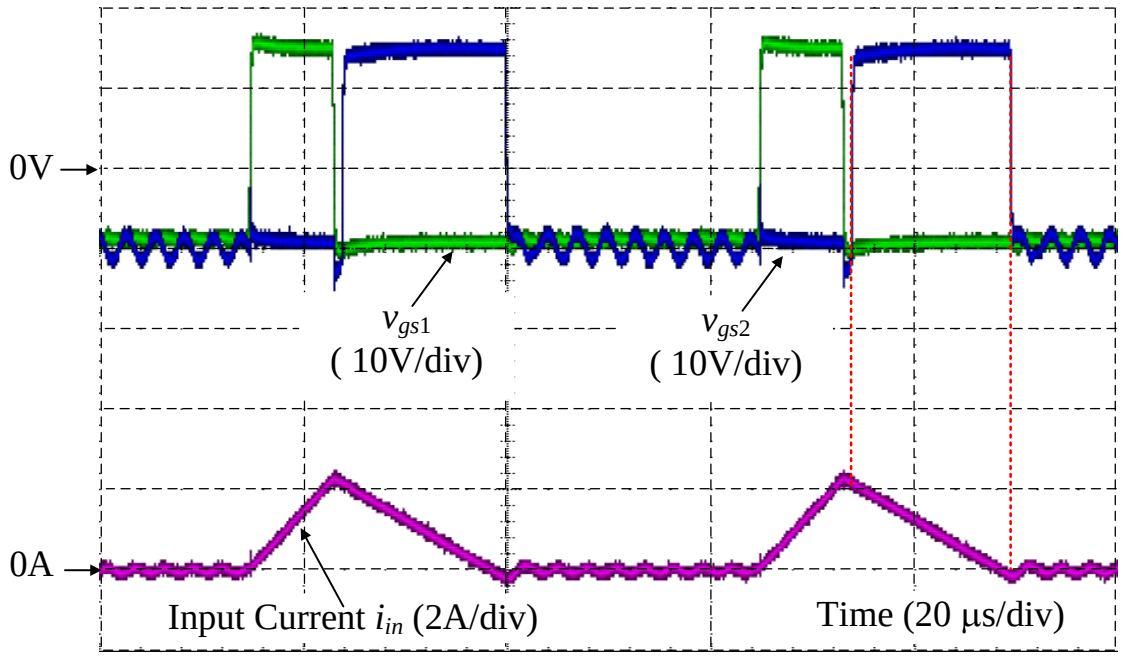
Fig. 3.14. Load transient response by output voltage control with 0.2-kHz cutoff frequency. The overshoot voltage and the settling time are 9 V and 1660 μs, the errors of which compared to the designed values are 4.3% and 1.6%, respectively [3-18].

to that in the conventional CCM control because the nonlinearity in the DCM current control is eliminated completely. Consequently, this implies that the bandwidth voltage control in DCM can be increased at least as same as CCM in order to minimize the output capacitance because the DCM operation can also eliminate the right-half plan zero in CCM [3-20].

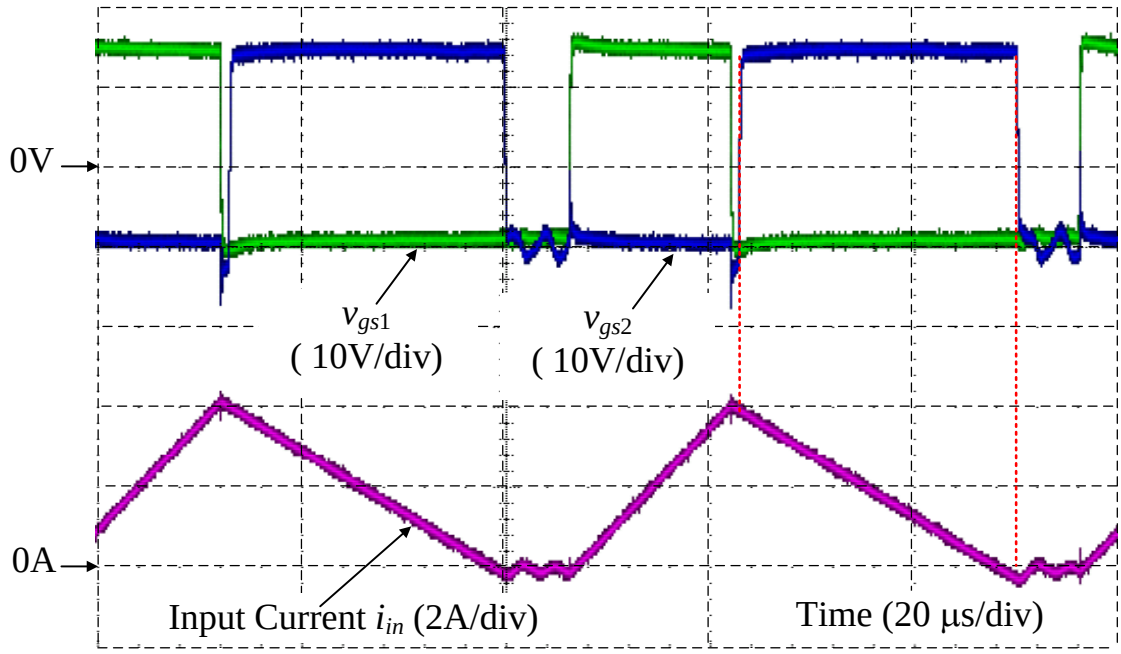
### 3.6.2 Discontinuous-Current-Mode Synchronous Switching Operation Waveforms, and Comparison of Efficiency and Computation Time

Fig. 3.15 illustrates the synchronous switching waveforms in DCM. It is concluded that $SW_2$ is turned off exactly when the current reaches zero, which achieves ZCS. Furthermore, before $SW_2$ is turned on, during the dead time, the current flows through the diode. Therefore, $SW_2$ turns on at the forward voltage of the diode, which is considered as ZVS. As a result, the synchronous switching in DCM causes almost no switching loss in $SW_2$. Furthermore, this proposed DCM synchronous switching can be realized without modifying the main circuit, which implies that the conversion efficiency can be increased simply.

Fig. 3.16 illustrates the efficiency comparison among the CCM synchronous switching, the DCM synchronous switching, and the DCM asynchronous switching with the same inductor $L_{HCR}$. The maximum efficiency of the DCM synchronous switching and the CCM synchronous switching are same as 98.7% because the circuit is designed in order to operate in CRM at full load. As the load becomes lighter, the efficiency of




(3.15.a) Switching signal at light load (0.3 p.u.)




(3.15.b) Switching signal at heavy load (0.9 p.u.)

Fig. 3.15. DCM synchronous switching. $SW_2$ is turned off exactly when the current reaches zero, which achieves ZCS.

the CCM synchronous switching decreases as explained in Fig. 3.1,

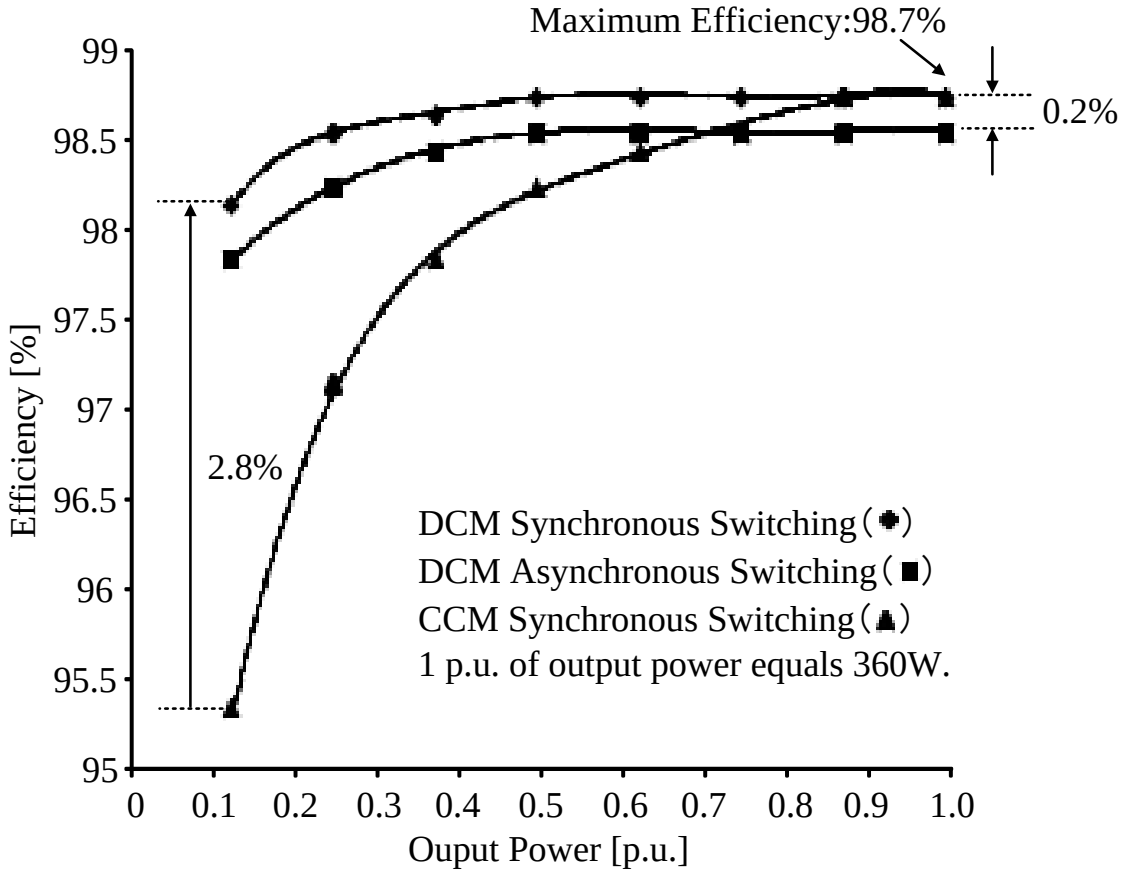



Fig. 3.16. Efficiency comparison among CCM synchronous switching, DCM synchronous switching and DCM asynchronous switching. The efficiency is maintained at high value above 98% over wide load range.

whereas the efficiency of the DCM synchronous switching is still maintained at high values over than 98%. In particular, at load of 0.125 p.u., the efficiency is improved by 2.8% when the DCM synchronous switching is applied. This efficiency improvement especially benefits the application with a frequent variation between light load operation and full load operation. On the other hand, compared to the DCM asynchronous

switching, the efficiency of the DCM synchronous switching is higher by 0.2% at all load range. This efficiency improvement is because the conduction loss of MOSFET is lower than that of a diode in the given switching device.

Table 3.3 shows the approximate computation time for all the arithmetic operations in the current control loop. Both division and square root digital calculations are time-consuming computation involving multiple clock cycles. In particular, when a STM32 Cortex-M4 microcontroller is applied to process 32-bit floating-point single-precision data, 14 clock cycles are required for a division or square root calculation, whereas 1 clock cycle is required for an addition or subtraction and 3 clock cycles are required for a multiplication [3-21]. In the conventional DCM current control, a division followed by a square root calculation is required to compute the DCM duty ratio as shown in Fig. 3.9(a). On the other hand, only one division is required in both the CCM current control as in Fig. 3.4 and the proposed DCM current control as in Fig. 3.9(b). Consequently, the computation time of the proposed DCM current control is longer only 6 clock cycles than the CCM current control, whereas the conventional DCM current control

TABLE 3.3.

COMPUTATION TIME IN CLOCK CYCLES FOR CURRENT CONTROL LOOP.

| Computation Time | CCM Current Control | Conventional DCM Current Control | Proposed DCM Current Control |
|---|---|---|---|
| PI controller | 9 | 9 | 9 |
| Duty-ratio feedforward | 16 | 0 | 0 |
| Nonlinearity compensation | 0 | 39 | 22 |
| Total | 25 (1 p.u.) | 48 ( 1.9 p.u. ) | 31 (1.2 p.u.) |

requires 35% longer computation time than the proposed DCM current control. Therefore, the proposed DCM current control helps in reducing the cost of the controller.

## 3.7 Conclusion

The approach to deal with the nonlinearity of DCM in this chapter was to utilize the duty ratio at the previous calculation period. This provided both the complete elimination of the DCM nonlinearity and the short computation time. Furthermore, the simple DCM synchronous switching without any modifications of the main circuit was realized to achieve high efficiency above 98% over wide load range, which helped in reducing the power consumption under light load conditions. In comparison with the CCM current control, the proposed DCM current control achieves the same current control bandwidth and improves the light load efficiency by 2.8% at most. Furthermore, the proposed DCM current control not only reduces the computation time by 35% but also increases the current control bandwidth by 47.5% compared to the conventional DCM current control. Consequently, the proposed DCM current control contributes into both the downsizing of the boost converter by the wide bandwidth current and voltage control, and the high efficiency over wide load range as well as short computation time.

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# Chapter 4

# Current Control for Discontinuous and Continuous Current Mode in Single-Phase Grid-Tied Inverter

## 4.1 Introduction

This chapter presents a current control method for the single-phase grid-tied inverter operating in both CCM and DCM, which is independent from the inductance, in order to achieve the inductance reduction without worsening the current total harmonic distortion (THD). The original idea in this chapter is that the DCM nonlinearity compensation is constructed by utilizing a duty ratio at a previous calculation period instead of using the inductance. Furthermore, the current mode is also determined without using the inductance by the comparison of the output duty ratios. Consequently,

the proposed CCM&DCM current control can be applied widely in the residential PV systems in order to minimize the *LCL* filters and further reduce the cost of the overall system. This chapter is organized as follows; in section 4.2, the zero-current clamping phenomenon is explained together with the problems of the conventional DCM nonlinearity compensation methods, then in section 4.3, the CCM&DCM current control based on the inductance-independent DCM nonlinearity compensation is proposed as the main part. After that, in section 4.4 the effectiveness of the proposed CCM&DCM current control is confirmed. Finally, in section 4.5, the conclusion of this chapter will be presented.

## 4.2 Zero-Current Clamping Phenomenon

Over last decades, the application of photovoltaic systems (PV) to residential areas has accelerated due to a continuously decrease in solar panel price. In the residential PV systems, single-phase grid-tied inverters are required in order to transmit solar DC power into AC single-phase grid. High efficiency and compact size with low cost are requirements for these inverters in order to further assist the penetration of the PV systems into the residential areas. In such grid-tied inverters, LCL filters are generally employed between the output of the inverter and the AC single-phase grid in order to suppress current harmonics and meet grid current harmonic constraints as defined by standards such as IEEE-1547 [4-1]. Inductors in the LCL filters account for major volume and cost of the inverter, which can be decreased by a low-inductance LCL filter design [4-2]-[4-6]. However, the reduction of the inductance implies a design of a high current ripple due to a high dc-link-voltage-to-inductance ratio. This high current ripple results in a current distortion phenomenon entitled zero-current clamping, in which the current distortion increases notably as the current ripple increases [4-7]-[4-12].

When the zero-current clamping occurs, the inverter operation changes from continuous current mode (CCM) to discontinuous current mode (DCM), which is well-known for its strong nonlinear behavior. In particular, the DCM operation exhibits a nonlinear duty-ratio-to-current transfer function, which significantly changes the converter dynamic; consequently, the current distortion increases when the same CCM controller is used to control the DCM current [4-13]-[4-15]. In past few years, many researches focusing on compensation methods for the DCM nonlinearity have been reported to solve this problem [4-14], [4-16]-[4-22]. However, the critical penalty of those methods is that the nonlinearity compensation for DCM is dependent on the inductance. In the residential PV systems, the inductors with high tolerance are generally employed in the inverter; furthermore, the grid-tied inverter is required to deal with severe changes of the ambience, i.e. the inductance varies frequently. When actual inductances are different from nominal values, the stability of such inductance-dependent control methods can no longer be guaranteed.

As development steps of the proposed current control, first, the DCM current control method for unipolar inverters has been proposed in [4-23];

next, this DCM current control method has been modified for bipolar inverters in [4-24]; finally, the current control method for bipolar inverters operating in both CCM and DCM under different power factors has been proposed in [4-25].

Fig. 4.1 depicts the circuit configuration of the single-phase grid-tied inverter. Although many DC/AC converter topologies such as, e.g. modular multilevel converters or flying capacitor multilevel converters [4-26]-[4-27], have been proposed for the grid-tied inverter, a typical

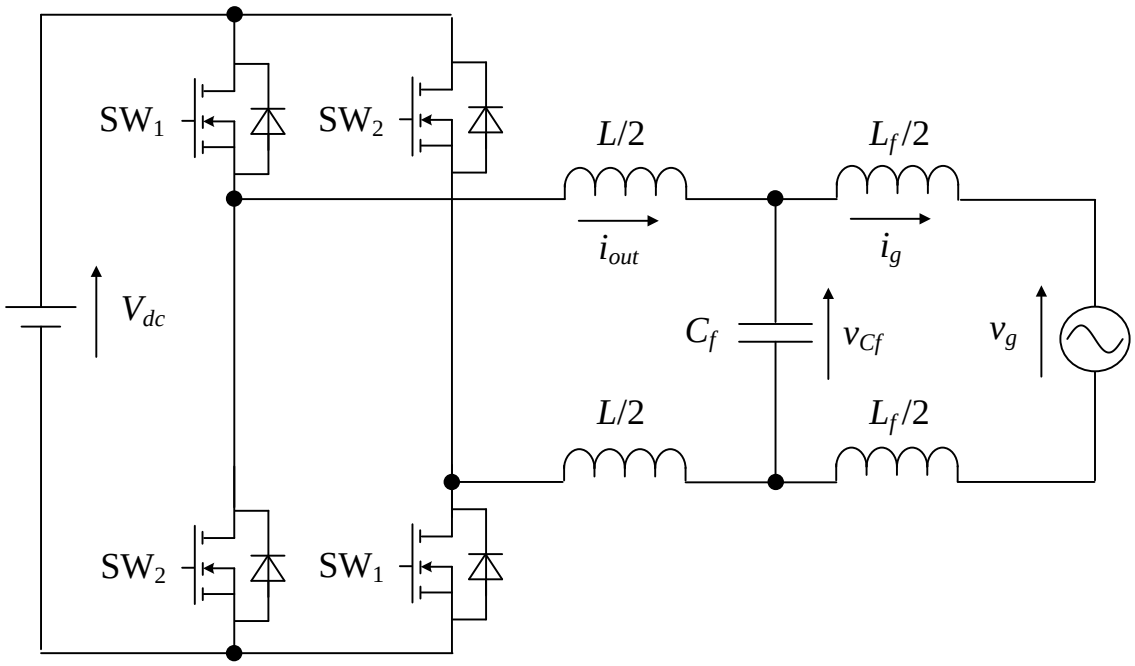
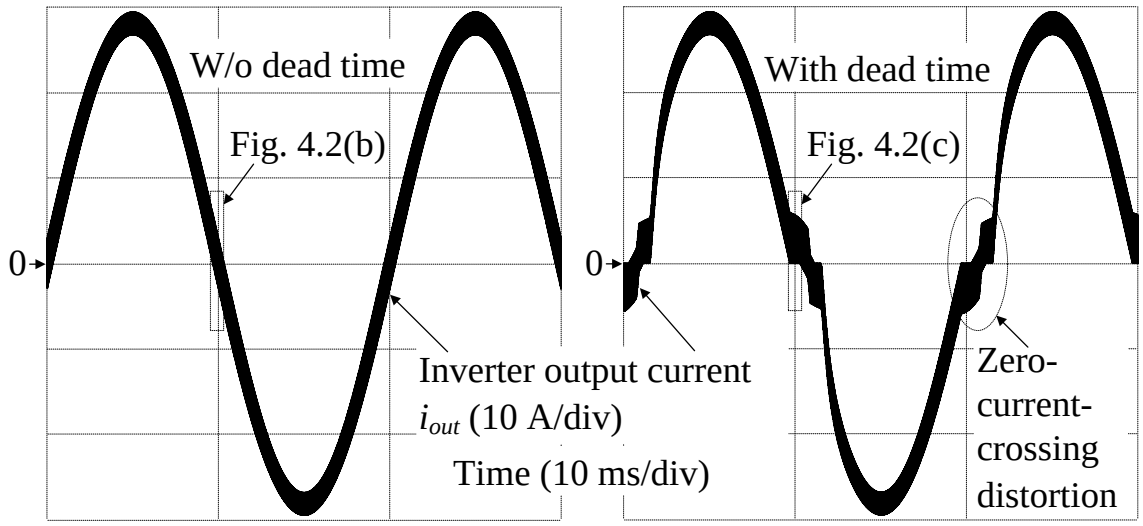


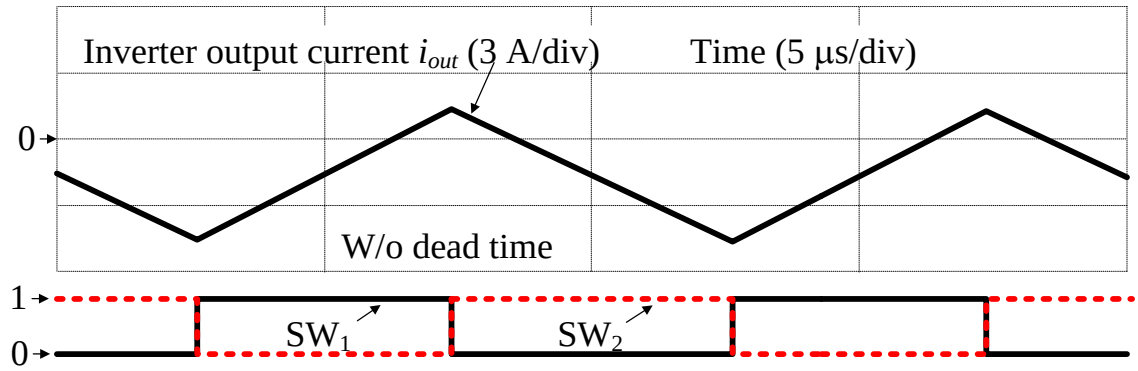

Fig. 4.1. Single-phase grid-tied inverter. An H-bridge inverter with a *LCL* filter is analyzed due to its simple configuration, which provides high fault-tolerant reliability. The inverter is operated under bipolar modulation and the impedance of each grid line is designed equally in order to minimize a common-mode current.

H-bridge inverter is analyzed due to its simple configuration, which provides high fault-tolerant reliability [4-28]. The *LCL* filter is used as an interface between the inverter and the grid in order to suppress the current harmonics of the inverter output current $i_{out}$. Compared to *L* filters or *LC* filters, the *LCL* filter can obtain effective switching harmonics attenuation with lower inductance requirements [4-29]. Meanwhile, in recent years, the application of wide bandgap semiconductor devices such as SiC or GaN enables the inverter to push the switching frequency up to several hundreds of kHz, further reducing the inductance of the *LCL* filter. However, the low-inductance *LCL* filter design significantly increases the zero-current-crossing distortion, ipso facto, that cannot satisfy the grid current harmonic constraints [4-7]-[4-12].

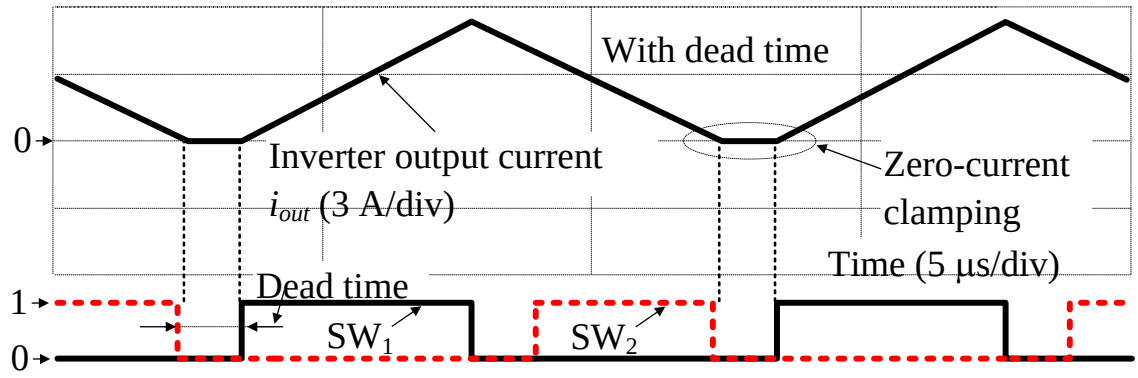
Fig. 4.2 describes the zero-current clamping phenomenon. When a dead-time is not in use, the inverter output current flows continuously over entire a switching period; hence, a sinusoidal current waveform is obtained. However, the zero-current clamping phenomenon occurs during the dead-time interval when the dead-time is applied in order to avoid an instantaneous turn-on of both two switching devices in one leg. Due to




(4.2.a) Inverter output current w/o dead time and with dead time




(4.2.b) Zoom-in current and switching signals w/o dead time




(4.2.c) Zoom-in current and switching signals with dead time

Fig. 4.2. Zero-current clamping phenomenon and zero-current-crossing distortion. The dead-time causes the zero-current clamping phenomenon in the vicinities of the zero-current crossing, which changes the inverter operation from CCM to DCM. The low current loop gain in DCM worsens the current response and causes the zero-current-crossing distortion. Note that the long dead-time is employed for better illustration.

this phenomenon, the inverter operation changes from CCM to DCM, which exhibits a nonlinear duty-ratio-to-current transfer function. In particular, the open loop gain in DCM is much lower than that in CCM as shown in Fig. 8 of [4-14]; consequently, the current distorts in the vicinities of the zero-current crossing due to the low current response in DCM when the same CCM controller is operated under DCM. The length of the zero-current clamping interval depends on the current ripple of the inverter output current $i_{out}$, the dead-time-to-switching-period ratio, and the power level. Therefore, the zero-current-crossing distortion is severe when the low-inductance design of the *LCL* filter is employed, i.e. the design of the high current ripple. The increase in the inverter-side inductance $L$ and the decrease in the dead time shorten the zero-current clamping interval and might reduce the zero-current-crossing distortion; however, the filter volume becomes large and the dead time is limited by the switching speed of the switching devices.

One of the approaches to deal with the zero-current-crossing distortion is to eliminate the zero-current clamping phenomenon. In [4-30], the turn-on and turn-off moment of the switching devices are adjusted when

the current is in the vicinities of the zero-current crossing in order to maintain the continuous flow of the current over entire a switching period. Hence, the current control performance remains unchanged and the zero-current-crossing distortion does not occur. However, the turn-on and turn-off moments are varied according to the current ripple, which depends on the inverter-side inductance $L$, i.e. an inductance-dependent method.

As other solutions, many current control methods for converters operating in both CCM and DCM have been proposed [4-14], [4-16]-[4-22]. A CCM&DCM control for practical applications has to deal with two main challenges; the DCM nonlinearity compensation and the mode detection between CCM and DCM. In the adaptive dead-time compensation method and the turn-off transition compensation method [4-16]-[4-17], the dead-time-induced error-voltage compensation is modified and fed forward into the output of the controller in order to compensate for the DCM nonlinearity when the zero-current clamping phenomenon occurs. Nevertheless, both methods exhibit the requirements which restrict the employment over a wide range of application. In particular, adjustment parameters for the adaptive dead-time compensation must be properly

tuned for each individual system [4-16]. Meanwhile, accurate device parameters, e.g. parasitic capacitances, are required for the turn-off transition compensation method [4-17]. Meanwhile, the conventional CCM grid-voltage feed forward is modified as shown in Fig. 10 of [4-14] or [4-22] to compensate the DCM nonlinearity, whereas the mode is simply detected by comparing the output of the feed forward. One of the disadvantages of this method is that, the feed forward for DCM is a function of the inductance, which still makes the control stability sensitive to the circuit parameter.

In [4-18], the DCM nonlinearity compensation is avoided by the design of a wide bandwidth current controller, whereas the mode detection is achieved by the zero-current detection. The wide bandwidth current controller can deal with the low open loop gain in DCM; however, this design requires a high speed microcontroller per se and is undesirable in term of cost reduction. In addition, the zero-current detection faces the challenge where the current does not remain at zero during the zero-current clamping interval. Instead, the actual current oscillates in the net comprised of the inverter-side inductor and parasitic capacitors of the switching

devices [4-19]. Therefore, the zero-current detection must be tuned whenever any circuit components are changed. In [4-20]-[4-21], the DCM nonlinearity compensation is also avoided by the design of a DCM current feed forward control. The principle of the DCM current feedforward control is to design the controller based on the reduced-order model or the full-order model [4-14]. An advantage of the feedforward control is the unrequired current sensor. However, a mismatch between the nominal values and the actual values of the circuit parameters still results in an instability of the control system. As the motivation for the achievement of the inductance reduction without worsening the current THD, it is necessary to realize the DCM nonlinearity compensation and the mode detection with a feature as inductance-independence.

## 4.3 Current Control for Discontinuous Current Mode and Continuous Current Mode

This section proposes the inductance-independent current control for the single-phase grid-tied inverter operating in both CCM and DCM as the main part. First, the derivation of the DCM nonlinearity compensation, where the use of the inductance is avoided by the duty ratio at previous calculation period, is explained in section 4.3.1 and 4.3.2. Next, the mechanism of the mode detection between CCM and DCM without using the inductance is explained in section 4.3.3.

### 4.3.1 Circuit Model Derivation

Fig. 4.3 depicts the current path and the inverter output current waveform in DCM when the grid voltage is positive. The filter inductor $L_f$ and the filter capacitor $C_f$ are omitted due to the simplification. In order to derive the nonlinearity compensation for DCM, the circuit model in DCM is required. First, let $D_1$, $D_2$ and $D_3$ denote the duty ratios of the first, the second and the zero-current interval. Average small signal modeling technique is used to model the inverter for the current control loop design [4-13]. The inductor voltage in mode 1, mode 2 and mode 3 is given by

(4.1)-(4.3), respectively,

$$v_{L1} = V_{dc} - v_g \quad (4.1)$$

$$v_{L2} = -\left(V_{dc} + v_g\right) \quad (4.2)$$

$$v_{L3} = 0 \quad (4.3)$$

where $V_{dc}$ is the dc-link voltage and $v_g$ is the grid voltage. Then, the inductor voltage during a switching period is expressed by (4.4),

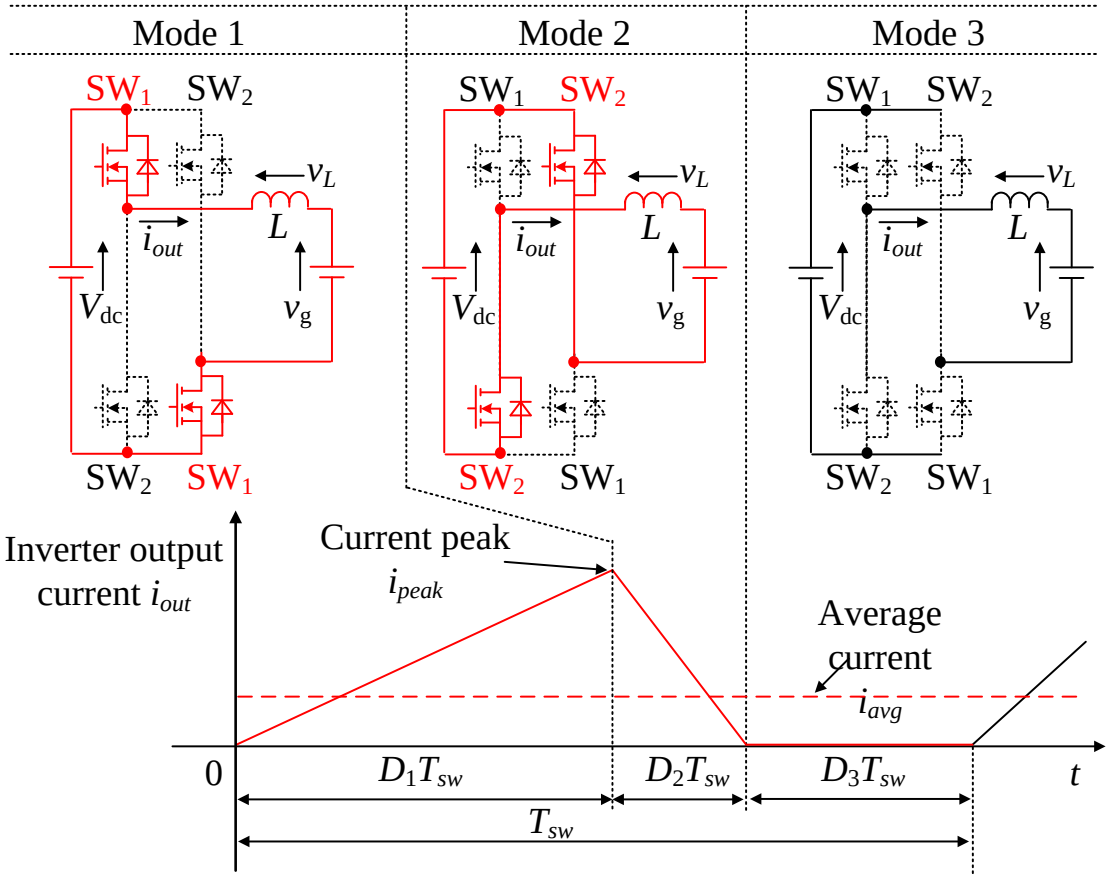



Fig. 4.3. Current path and inverter output current waveform in DCM when the grid voltage is positive. The zero current interval $D_3T_{sw}$ occurring in DCM introduces the nonlinearities into the transfer function [4-13]-[4-15].

$$\begin{aligned} v_L &= D_1 v_{L1} + D_2 v_{L2} + D_3 v_{L3} \\ &= D_1\left(V_{dc} - v_g\right) - D_2\left(V_{dc} + v_g\right) \end{aligned} \quad \text{.....} (4.4)$$

The average current and the current peak of the inverter output current are given by (4.5)-(4.6), respectively,

$$i_{avg} = \frac{i_{peak}}{2}\left(D_1 + D_2\right) \text{.....} (4.5)$$

$$i_{peak} = \frac{V_{dc} - v_g}{L} D_1 T_{sw} \text{.....} (4.6)$$

where $T_{sw}$ is the switching period. Substituting (4.6) into (4.5) and solving the equation for the duty ratio $D_2$, then the duty ratio $D_2$ is expressed by (4.7),

$$D_2 = \frac{2Li_{avg}}{D_1 T_{sw}(V_{dc} - v_g)} - D_1 \text{.....} (7)$$

Substituting (4.7) into (4.4) in order to remove $D_2$, and representing (4.4) as a function of $D_1$, (4.8) is obtained,

$$\begin{aligned} L\frac{di_{avg}}{dt} &= v_L \\ &= V_{dc}\left(2D_1 - 1\right) - v_g + \left(V_{dc} + v_g\right)\left[1 - \frac{2Li_{avg}}{\left(V_{dc} - v_g\right)D_1 T_{sw}}\right] \end{aligned} \text{.....} (8)$$

Then, the DCM circuit model is established based on (4.8) [4-13].

Fig. 4.4 illustrates the circuit model of the inverter operating in DCM.

The dash line part does not exist when the inverter operates in CCM because the average current $i_{avg}$ equals to the half current peak $i_{peak}/2$; in other words, the CCM operation makes the zero-current interval $D_3T_{sw}$ shown in Fig. 4.3 disappear. However, the zero-current interval $D_3T_{sw}$ induces the nonlinearity into the transfer functions when the inverter operates in DCM, which worsens the current response in DCM when the same controller is applied for both CCM and DCM [4-13]-[4-15]. Therefore, the output of the controller is necessary to be compensated when

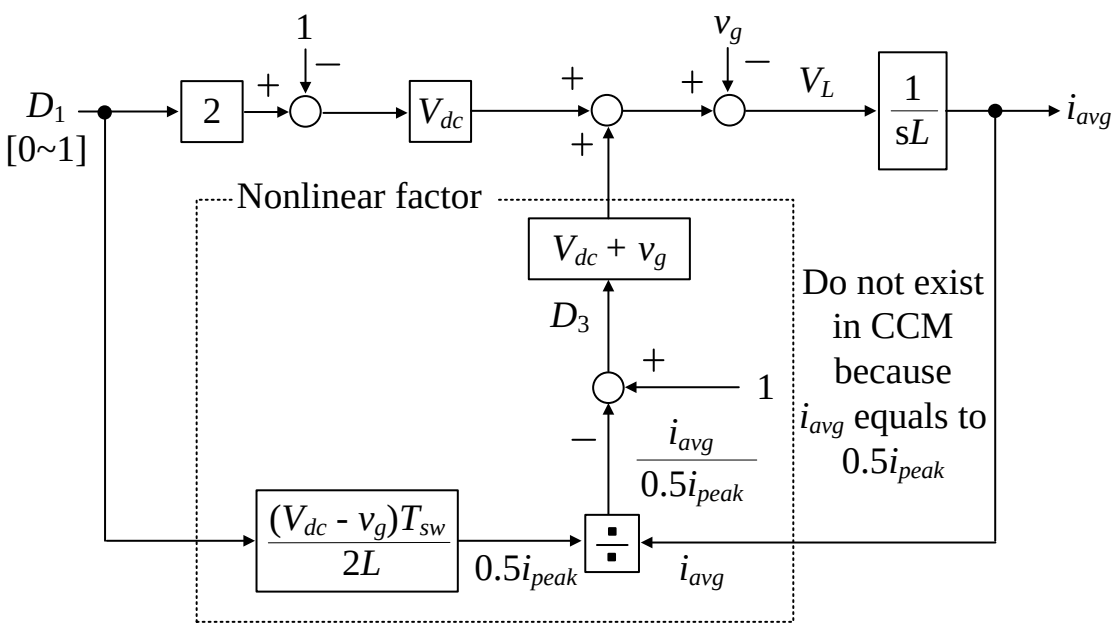



Fig. 4.4. Circuit model of inverter operating in DCM. The current control loop gain in DCM depends on the average current, i.e. the nonlinearities occurring in the duty-ratio-to-current transfer function and the grid-voltage-to-current transfer function.

the inverter operates in DCM. The derivation of the compensation for the DCM nonlinearity is explained as follows. First, the circuit model in Fig. 4.4 is linearized at steady-state points. In particular, the dc-link voltage, the grid voltage, the average current and the duty ratio when the inverter operates in the steady-state points can be expressed by (4.9)-(4.12), respectively,

$$V_{dc} = V_{dc_s} + \Delta v_{dc} \quad (4.9)$$

$$v_g = v_{g_s} + \Delta v_g \quad (4.10)$$

$$i_{avg} = i_{avg_s} + \Delta i_{avg} \quad (4.11)$$

$$D_1 = D_{1_s} + \Delta D_1 \quad (4.12)$$

where $V_{dc_s}$, $v_{g_s}$, $i_{avg_s}$ and $D_{1_s}$ are the dc-link voltage, the grid voltage, the average current and the duty ratio at the steady-state points, whereas $\Delta V_{dc_s}$, $\Delta v_{g_s}$, $\Delta i_{avg_s}$ and $\Delta D_{1_s}$ are the small signals of the dc-link voltage, the grid voltage, the average current and the duty ratio, respectively. The fluctuation of the dc-link voltage is considered to be small; consequently, the small signal of the dc-link voltage, i.e. the dc-link voltage dynamic, $\Delta V_{dc_s}$ is negligible. The circuit model in Fig. 4.4 is linearized at the steady-state points by substituting (4.9)-(4.12) into (4.8) [4-13].

### 4.3.2 Nonlinearity Compensation with Duty at Previous Calculation Period

Fig. 4.5 depicts the linearized circuit model of the inverter operating in DCM. In order to simplify the coefficients $i_{avg_s}$ in the linearized circuit model, the relationship between the coefficients $i_{avg_s}$ and the duty ratio $D_{1_s}$ at the steady-state points are derived by substituting the differential of the inductor average current $di_{avg}/dt$ in (4.8) as zero [4-13]-[4-14],

$$i_{avg_s} = \frac{D_{1_s}^2 T_{sw} V_{dc_s}\left(V_{dc_s} - v_{g_s}\right)}{L\left(V_{dc_s} + v_{g_s}\right)} \quad \text{.....} (4.13)$$

Then, (4.13) is substituted into Fig. 4.5 in order to express all the

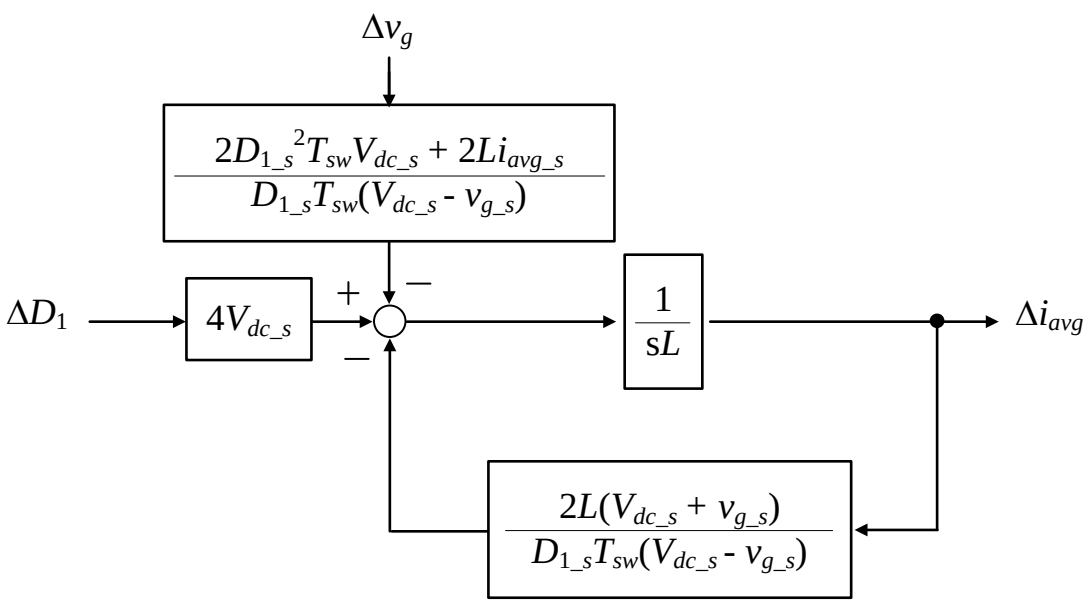



Fig. 4.5. Linearized circuit model of inverter operating in DCM. The current control of DCM obtains the same dynamic as in CCM by compensating the DCM nonlinearity at the output of the controller.

coefficients as functions of the duty ratio $D_{1_s}$.

Fig. 4.6 shows the simplified and linearized circuit model. Two duty-ratio-dependent factors occur in the duty-ratio-to-current transfer function and the grid-voltage-to-current transfer function when the inverter operates in DCM. If these duty-ratio-dependent factors are compensated at the output of the controller, the same CCM current dynamic can be obtained when the inverter operates in DCM; therefore, the value of the duty ratio $D_{1_s}$ at the steady-state points is necessary. In the conventional DCM nonlinearity compensation method [14], the value of $D_{1_s}$ is

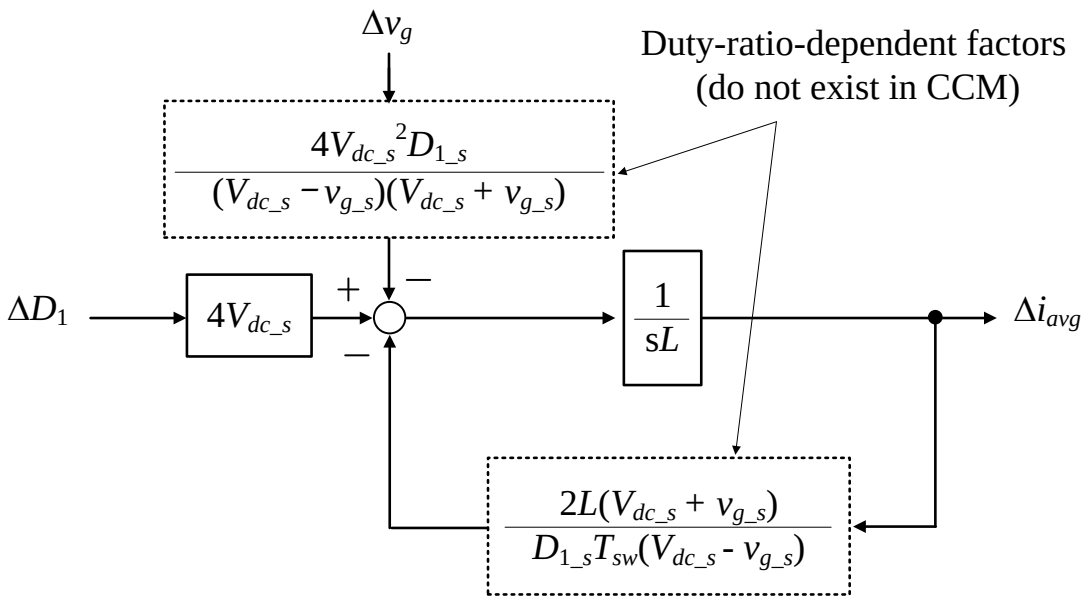



Fig. 4.6. Simplified and linearized circuit model. The value of the duty ratio $D_{1_s}$ at steady-state points is required in order to compensate for the duty-ratio-dependent factors occurring when the inverter operates in DCM.

estimated based on (4.14), which is derived from (4.13),

$$D_{1_s} = \sqrt{\frac{Li_{avg_s}\left(V_{dc_s} + v_{g_s}\right)}{T_{sw}V_{dc_s}\left(V_{dc_s} - v_{g_s}\right)}} \quad \text{.....} (4.14)$$

where $i_{avg_s}$, $V_{dc_s}$, and $v_{g_s}$ are extracted from the detection values of the average current, the dc-link voltage and the grid voltage. It is obvious that (4.14) is a function of the inductance $L$; hence, the conventional DCM nonlinearity compensation method is inductance-dependent. The characteristic of circuit-parameter-dependency prevents the conventional method from the application of the residential PV systems, where the accurate value of $L$ is difficult to obtain as mentioned in section II. On the other hand, the estimation of $D_{1_s}$ by the duty ratio at the previous calculation period is proposed to avoid the dependency of $L$ as the originality of this paper. Hence, the circuit model of the inverter operating in DCM is necessary to be analyzed in the discrete model of Fig. 4.6.

Fig. 4.7 depicts the discretized circuit model of the inverter operating in DCM. The duty-ratio-dependent factors in Fig. 4.7 are necessary to be set as 1 when the circuit operates in DCM in order to compensate the DCM nonlinearity at the output of the controller designed in CCM. In particular, the steady-state values of $V_{dc_s}$ and $v_{g_s}$ are obtained by the detection values

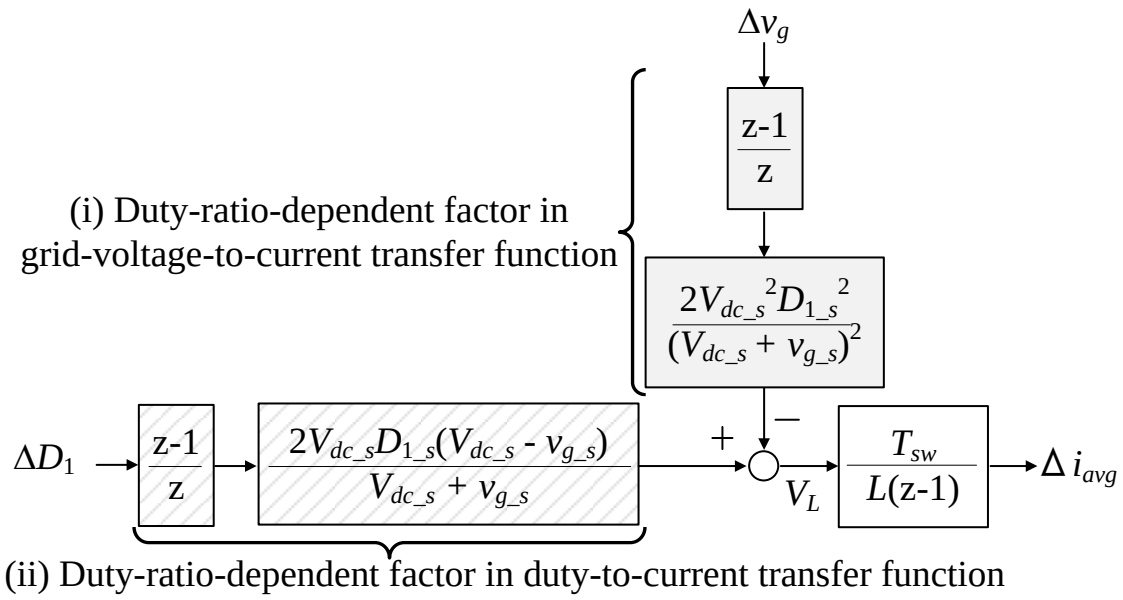
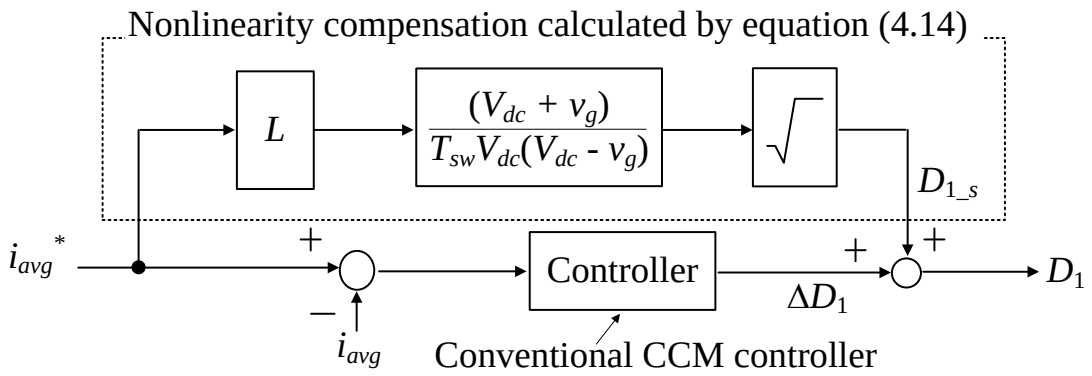


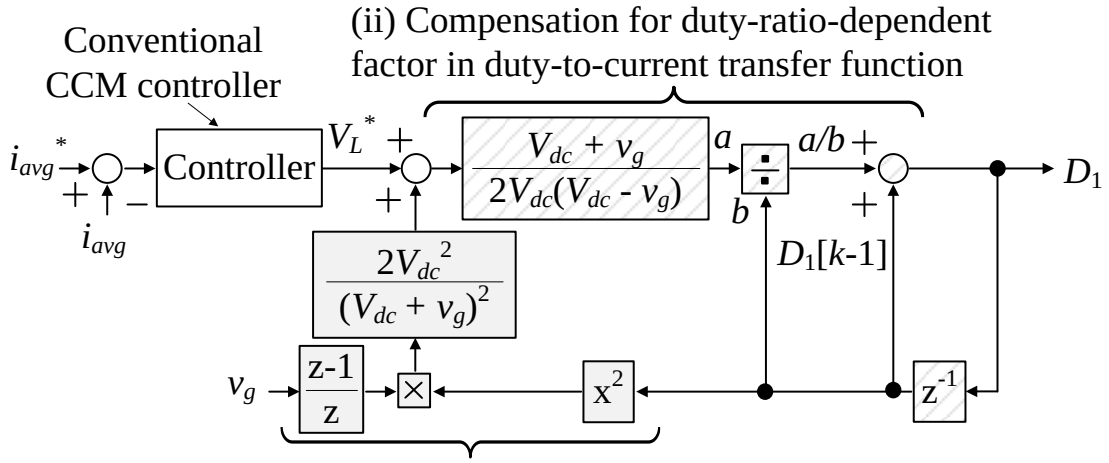

Fig. 4.7. Discretized circuit model of inverter operating in DCM. The original idea of the DCM nonlinearity compensation is to estimate the duty ratio at the steady-state points by the duty ratio at the previous calculation. Consequently, the inductance is not required in the DCM nonlinearity compensation.

of the dc-link voltage and the grid voltage, whereas the steady-state duty ratio $D_{1_s}$ is estimated by the duty ratio $D_1[k\text{-}1]$ at the previous calculation period.

Fig. 4.8 illustrates the conventional DCM nonlinearity compensation in Fig. 10 of [4-14], and the proposed DCM nonlinearity compensation. The same principle of two methods is the estimation of $D_{1_s}$ in order to compensate for the DCM nonlinearity. In the conventional method, $D_{1_s}$ is estimated by using the current command $i_{avg}^*$ and (4.14); consequently, this




(4.8.a) Conventional DCM nonlinearity compensation in [14]




(4.8.b) Proposed DCM nonlinearity compensation

Fig. 4.8. Conventional and proposed DCM nonlinearity compensation. The main difference between the conventional and proposed method is that, the DCM nonlinearity compensation is constructed by utilizing the duty ratio at the previous calculation period; hence, this makes the control system inductance-independent.

leads to the inductance-dependence. On the other hand, in the proposed method, $D_{1_s}$ is estimated by using the duty ratio $D_1[k\text{-}1]$ at the previous calculation period, which provides the control system

inductance-independence and the same CCM current response when the inverter operates in DCM [4-15]. Note that the above analysis is conducted when the grid voltage is positive; however, the same analysis procedure can be applied when the grid voltage is negative. For the sake of brevity, the derivation for the circuit model in DCM for the negative grid voltage is simplified as follows.

Fig. 4.9 depicts the current path and the inverter output current waveform in DCM when the grid voltage is negative. The same circuit model of Fig. 4.4 is obtained even when the grid voltage is negative; therefore, the similar DCM nonlinearity compensation is applied with the negative grid voltage. However, the applying order of mode 1 and mode 2 in Fig. 4.9 is flipped compared to that in Fig. 4.3, which implies that the output of the controller system $D_1$ in Fig. 4.8(b) has to be applied to the switch $SW_1$ when the grid voltage is positive, and inversely, $D_1$ has to be applied to the switch $SW_2$ when the grid voltage is negative. This switching signal generation is the main difference between the DCM operation and the CCM operation, where the switching signal of $SW_2$ in CCM is the inverse switching signal of $SW_1$. In the DCM operation, the inverse

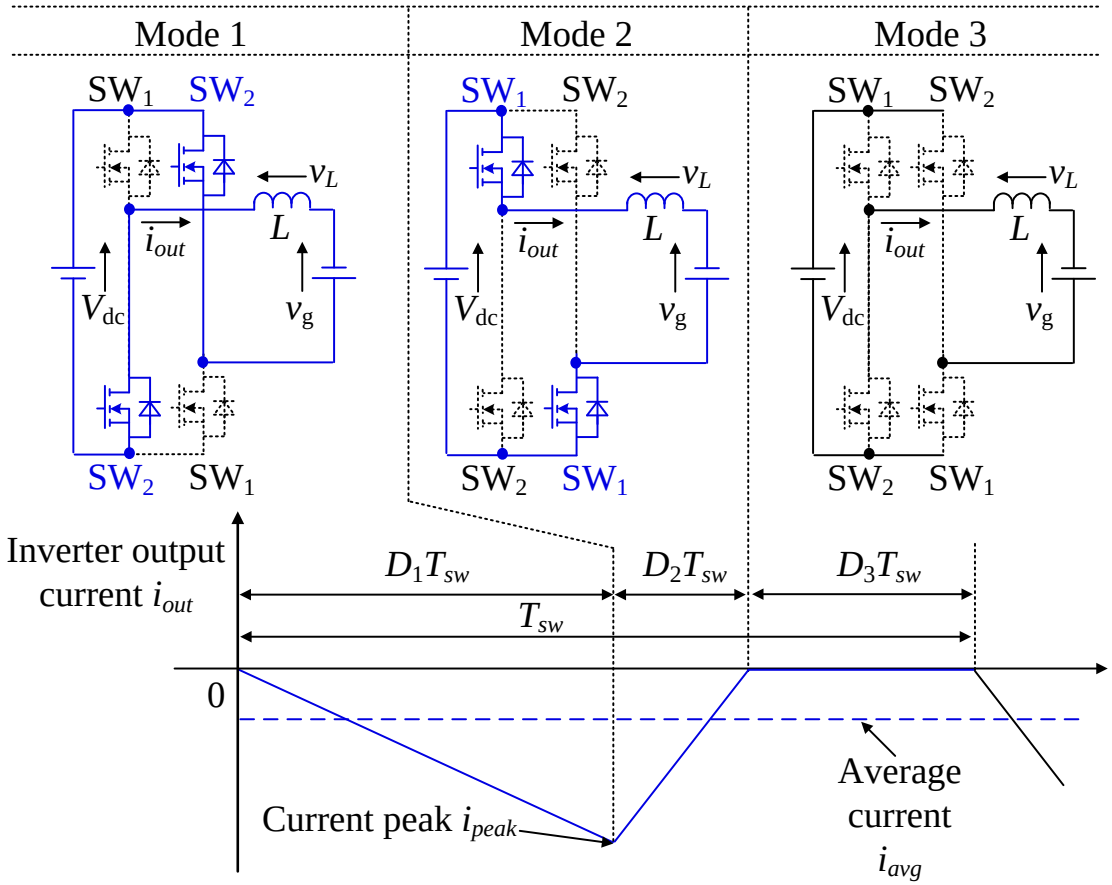



Fig. 4.9. Current path and inverter output current waveform in DCM when the grid voltage is negative. The same analysis procedure when the grid voltage is positive can be applied with the negative grid voltage.

switching signal of each switch does not equal to the switching signal of the other switch due to the occurrence of the zero-current interval $D_3T_{sw}$. Meanwhile, the polarity of $v_g$ in Fig. 4.8(b), which should always be positive, becomes negative when the grid voltage is negative because $v_g$ is extracted from the detection value of the grid voltage. Therefore, the simple solution is to modify $v_g$ in Fig. 4.8(b) into the multiplication of $v_g$ and the polarity of $i_{avg}^*$.

Fig. 4.10 illustrates the proposed DCM current control for the grid-tied inverter and the variation of the duty ratio in DCM. Compared to Fig. 4.8(b), the multiplication of $v_g$ and the polarity of $i_{avg}^*$ is used in the compensation of the duty-ratio-dependent factors in order to obtain the DCM current dynamic as same as CCM regardless of the polarity of the grid voltage. The determination in which the output of the control system should be applied to $SW_1$ or $SW_2$, can be carried out by the comparison of the polarity of the grid voltage $v_g$ or the current command $i_{avg}^*$. However, this method might interrupt the continuous change of $D_1$, because the actual current phase $i_{avg}$ is lag compared to that of the current command $i_{avg}^*$. Instead, the polarity of $D_1$ is used to determine if $D_1$ should be applied to $SW_1$ or $SW_2$ in order to avoid the interruption of the continuous change of $D_1$. As mentioned above, the switching signal generation in DCM differs from that in CCM because both the switches $SW_1$ and $SW_2$ must be turned off during the zero-current interval $D_3T_{sw}$, which cannot be realized by the use of the inverse switching signal as in CCM. Therefore, the idea to operate the inverter under DCM is the alternate switching of $SW_1$ or $SW_2$ dependently on the polarity of $D_1$.

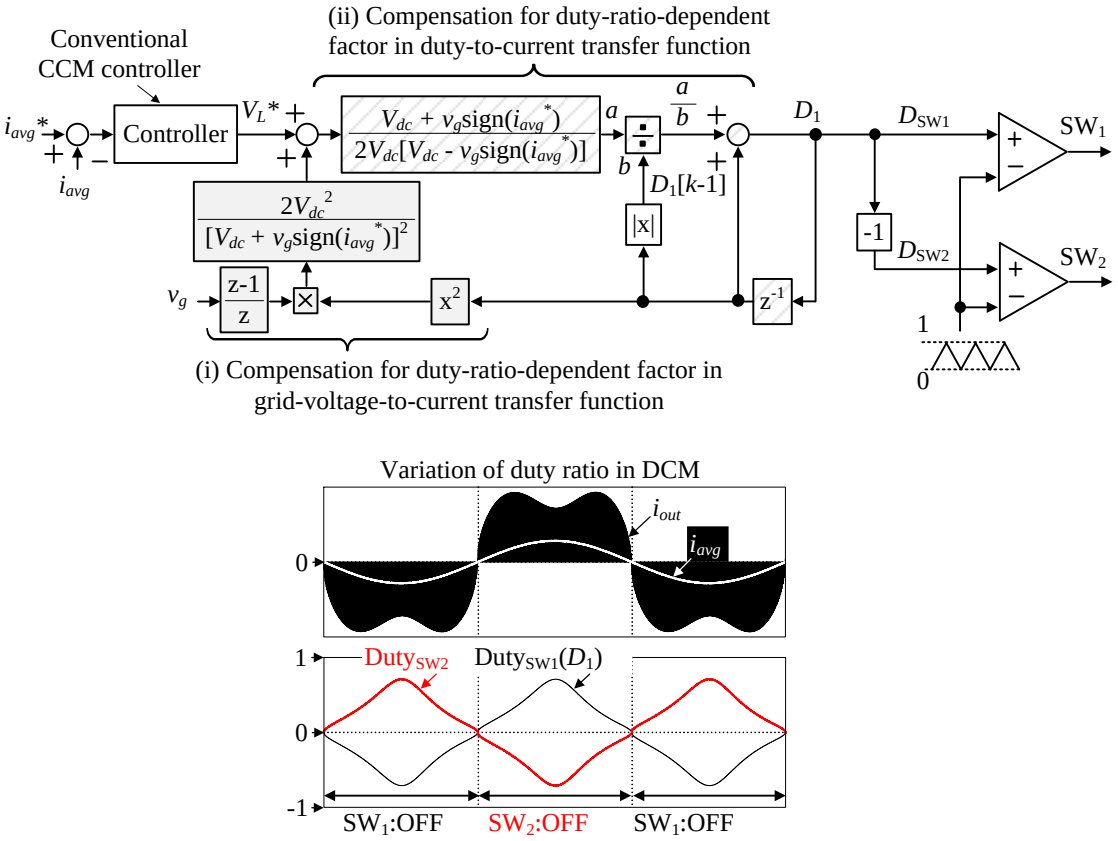



Fig. 4.10. Proposed DCM current control system for single-phase grid-tied inverter and variation of duty ratio in DCM. The polarity of $D_1$ is used to determine if $D_1$ should be applied to $SW_1$ or $SW_2$ in order to avoid the interruption of the continuous change of $D_1$.

Meanwhile, another difference between the CCM operation and the DCM operation observed from the variation of the duty ratio is that, the duty ratio of CCM only varies only around the value of 0.5, whereas the duty ratio in DCM decreases to zero when the average current reaches zero. The reason of the difference in the duty ratio variation is that the duty-ratio-to-current transfer function in CCM is linear, which implies the

duty ratio does not relate to the average current but only the change of the average current, whereas the duty-ratio-to-current transfer function in DCM is nonlinear, which means the duty ratio depends on the average current. The proposed DCM current control system is employed when the inverter is operated entirely in DCM even at a rated load. However, this design results in an extremely high current ripple, which significantly increases a conduction loss in the switching devices and requires a larger heat sink [4-6], [4-30]. Therefore, a design of a moderate current ripple, in which the inverter operates in both CCM and DCM, is preferred in order to minimize the *LCL* filter without increasing the inverter loss.

### 4.3.3 Current Mode Determination

Fig. 4.11 indicates the relationship among the CCM duty, the DCM duty and the current mode. The current mode detection between CCM and DCM is necessary when the inverter is designed to operate in both CCM and DCM. One of the conventional current mode detection method is the detection of the zero current in DCM [4-18]. However, the zero current detection faces many challenges in practical applications, one of which is the current oscillation during the zero-current interval $D_3T_{sw}$ shown in Fig.

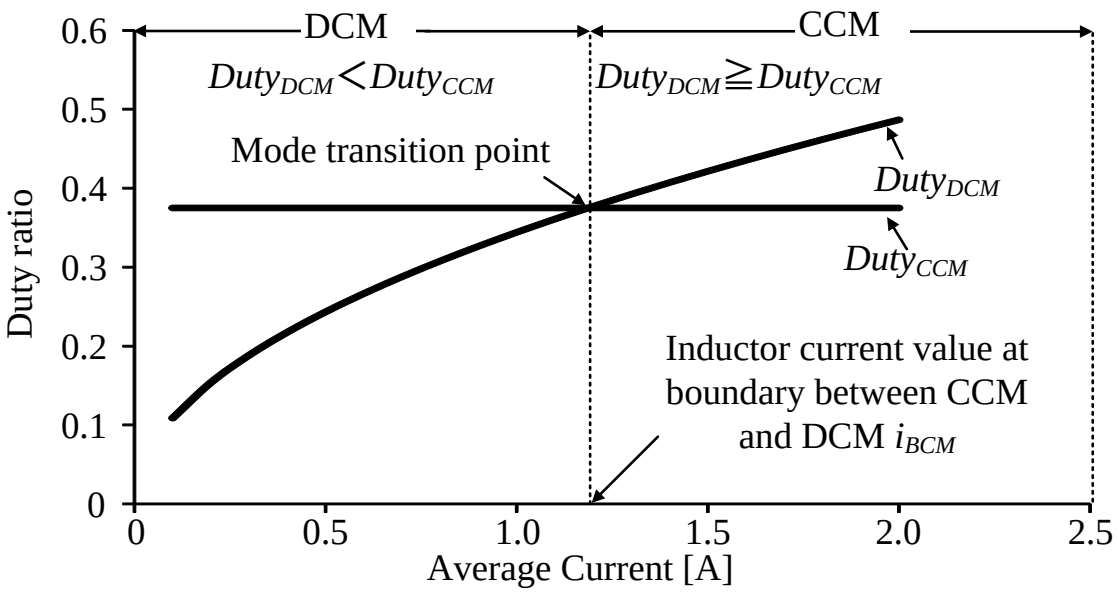



Fig. 4.11. Relationship among CCM duty, DCM duty and current mode. When the circuit operates in DCM, the DCM duty becomes smaller than the CCM duty and vice versa. The current mode determination is realized independently from the inductance by using this relation of the duty ratios.

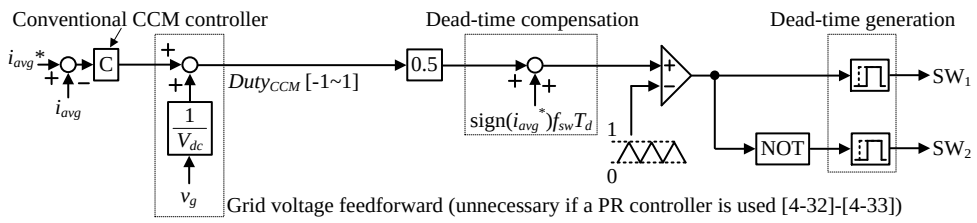
4.3 and Fig. 4.9. In particular, this current oscillation is caused by the energy oscillation between the inductor $L$ and the parasitic capacitance of the switches, which becomes more severe with a low inductance $L$ and a high switching frequency [4-19]. As another typical approach, the detection value of the average current $i_{avg}$ or the average current command $i_{avg}^*$ is compared with the current value $i_{BCM}$ at the boundary between CCM and DCM; if $i_{avg}$ is larger than $i_{BCM}$, CCM is determined as the operation mode and vice versa [4-20]. However, the inductance is used in the calculation of $i_{BCM}$ which implies the current mode determination is inductance-dependent. Consequently, when the actual inductor value is different from the nominal value, the current mode cannot be accurately determined by the conventional method. On the other hand, the proposed current mode determination focuses on the relationship among the CCM duty $Duty_{CCM}$, the DCM duty $Duty_{DCM}$ and the current mode. In particular, if $Duty_{CCM}$ is larger than $Duty_{DCM}$, DCM becomes the operation mode and vice versa. Note that $Duty_{CCM}$ is independent from the average current, whereas $Duty_{DCM}$ changes with the variation of the average current (cf. Fig. 4.10 of section 4.3.2). In general, $Duty_{CCM}$ is the output value of the controller,

which implies the calculation for $Duty_{CCM}$ is independent from the inductance. If the proposed DCM nonlinearity compensation in section 4.3.2 is employed, the calculation for $Duty_{DCM}$ also becomes inductance-independent. Consequently, if the relationship between $Duty_{CCM}$ and $Duty_{DCM}$ is used to determine the current mode, the inductance-independent current mode determination is achieved. In other words, the proposed inductance-independent DCM nonlinearity compensation in section 4.3.2 leads to the inductance-independent current mode determination.

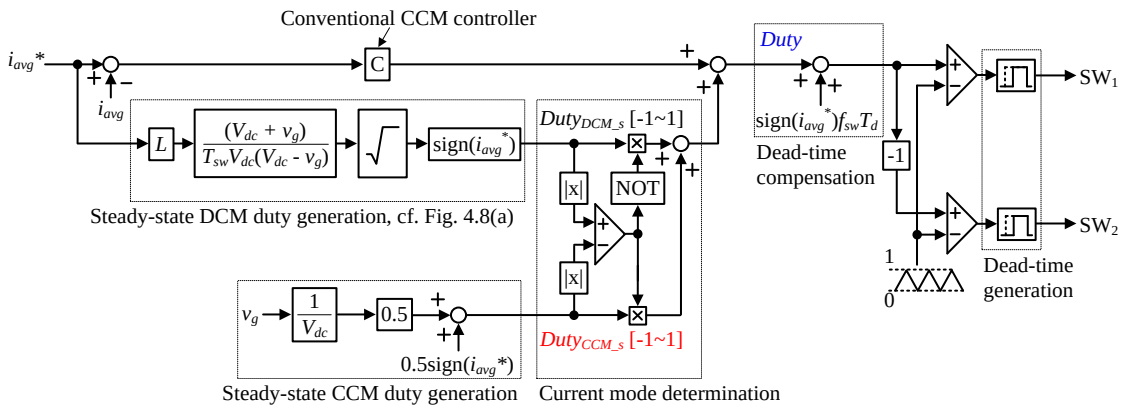
Fig. 4.12 describes the conventional CCM current control system, the conventional CCM&DCM current control system, and the proposed inductance-independent CCM&DCM current control system with the waveform of the current mode alternation. In the conventional CCM current control system, when a typical PI controller is employed, the grid voltage feedforward is required in order to enhance the disturbance suppression. Although the inductance might be used in the design of the controller, the conventional CCM current control system is inductance-independent per se if the bandwidth of the controller is properly

designed [4-31]. Note that the grid voltage feedforward can be eliminated if the proportional-resonant (PR) controller is applied [4-32]-[4-33]. Meanwhile, a typical two-level dead-time compensation is employed to compensate the dead-time-induced error voltage [4-34]-[4-35]. Nevertheless, the conventional CCM current control system cannot compensate for the DCM nonlinearity when the zero-current phenomenon becomes noticeable as the current ripple increases. In the conventional CCM&DCM current control system, first, both the steady-state DCM duty $Duty_{DCM_s}$ and the steady-state CCM duty $Duty_{CCM_s}$ are generated. Then, these two duty ratios are compared to each other; the smaller duty ratio is feed forward to the output of the controller to compensate for the grid voltage disturbance in CCM or the nonlinearity in DCM. It is obvious that the conventional CCM&DCM current control system is dependent on $L$. In the proposed CCM&DCM current control system, first, both the DCM duty $Duty_{DCM}$ and the CCM duty $Duty_{CCM}$ are generated. Then, the absolute value of these two duty ratios are compared to each other; the smaller duty ratio is used to generate the switching signal for the switches. Note that the absolute operators are used with the consideration of the negative grid

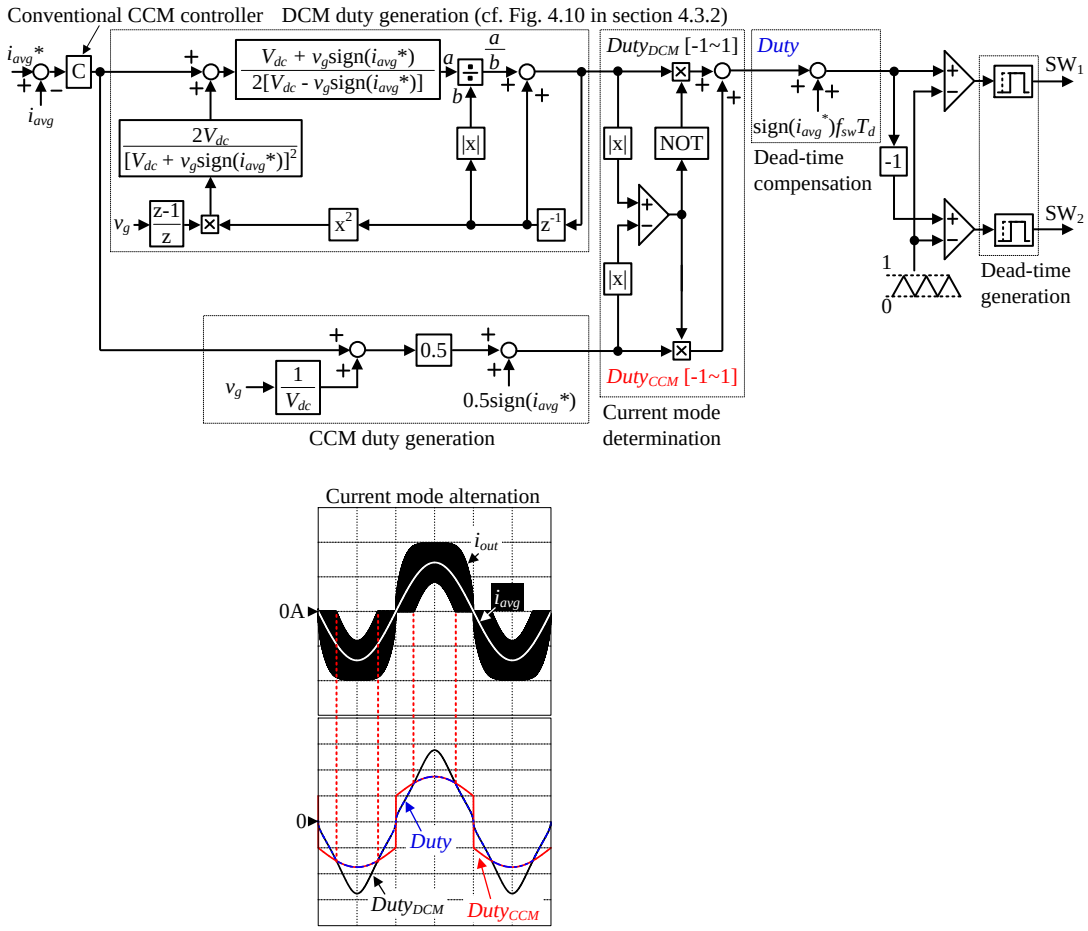
voltage as shown in the waveform of the current mode alternation in Fig. 4.12(c). The original idea of the inverter control for the operation in both DCM and CCM is that as first step, the duty ratio at the previous calculation period is used to compensate the DCM nonlinearity regardless of $L$, then two outputs of the inductance-independently generated duty ratios are compared to each other in order to determine the current mode. Consequently, the CCM&DCM current control system can perform the current control independently from $L$.




(4.12.a) Conventional CCM current control system




(4.12.b) Conventional CCM&DCM current control system, cf. Fig. 10 of [4-14]




(4.12.c) Proposed inductance-independent CCM&DCM current control system with waveform of current mode alternation

Fig. 4.12. Conventional CCM current control system, conventional CCM&DCM current control system, and proposed inductance-independent CCM&DCM current control system with waveform of current mode alternation. The constant-gain conventional CCM current control system cannot compensate for the DCM nonlinearity, whereas the conventional CCM&DCM current control system is dependent on the inductance. On the other hand, the proposed CCM&DCM current control system compensates for the DCM nonlinearity and determines the current mode independently from the inductance.

# 4.4 Experimental Results

## 4.4.1 Construction and Assembly

Table 4.1 depicts the experimental parameters, whereas Fig. 4.13 shows the 4-kW 100-kHz prototype of the single-phase grid-tied inverter. With a relatively mature development, SiC switching devices are chosen to operate

TABLE 4.1.
EXPERIMENTAL PARAMETERS.

| **Circuit Parameter** | | |
|---|---|---|
| $V_{dc}$ | Dc-link voltage | 350 V |
| $v_g$ | Grid voltage | 200 Vrms |
| $P_n$ | Nominal power | 4 kW |
| Switching device (SiC MOSFET) | | SCT303AL (ROHM) |
| Core material and Litz wire | | Ferrite N87, 504/ϕ0.1 |
| $f_g$ | Grid frequency | 50 Hz |
| $C_{dc}$ | Dc-link capacitance | 2720 μF |
| $C_f$ | Filter capacitance | 4 μF |
| $L_f$ | Filter inductance | 20 μH |
| $f_{sw}$ | Switching frequency | 100 kHz |
| **Current Controller Parameter** | | |
| $f_{samp}$ | Sampling frequency | 25 kHz |
| $\zeta$ | Damping factor | 1.2 |
| $f_c$ | Cutoff frequency | 1 kHz |
| $T_d$ | Dead time | 500 ns |

the inverter at the high switching frequency of 100 kHz; consequently, the *LCL* filter can be minimized due to a design of a high cutoff frequency. A natural cooling method is preferred for the residential PV systems in order to eliminate a periodic maintenance of cooling fans. Electrolytic capacitor with high ratio between the capacitance and volume is chosen to absorb the single-phase power fluctuation as a passive energy buffer method [4-27].

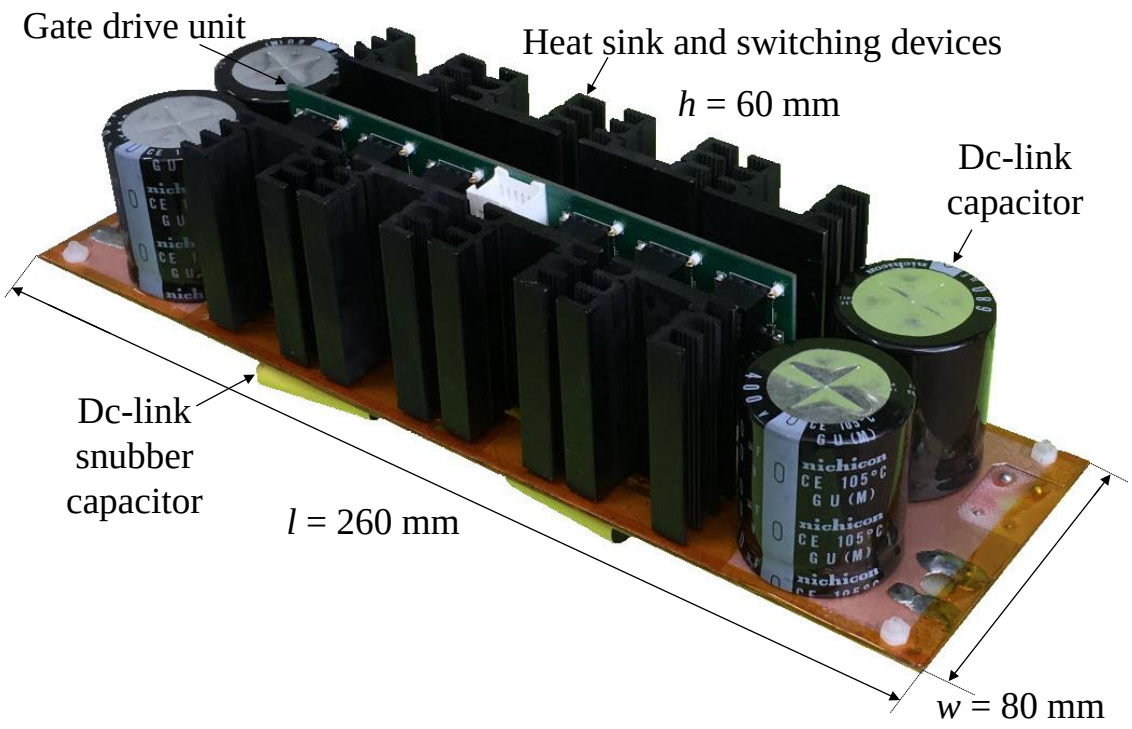



Fig. 4.13. 4-kW 100-kHz prototype of single-phase grid-tied inverter. SiC switching devices are chosen to operate the inverter at high switching frequency of 100 kHz, whereas two switching devices are connected in parallel to reduce the conduction loss in each device and enable the employment of natural cooling. Meanwhile, four electrolytic capacitors of 680-μF are connected in parallel at the dc link to absorb the single-phase power fluctuation and maintain a low dc-link voltage ripple.

These capacitors are designed with a consideration of a capacitor current ripple to avoid a temperature rise due to an equivalent series resistance of capacitors, which is the main cause of the lifetime decrease of the electrolytic capacitor [4-36]. Note that the operation frequency of the microcontroller is synchronized with the sampling frequency of 25 kHz despite of the high switching frequency of 100 kHz; this enables the use of general-purpose microcontrollers. Furthermore, PI controller is chosen to use in the residential PV system due to its mature development and research.

Table 4.2 depicts the minimum required dead time consideration. The dead time design is conducted in consideration of the following factors: the maximum drain current of 60 A, the gate resistor of 3 Ω, the maximum ambient temperature of 50°C, and the high-volume production. Consequently, the dead time is finally designed to 500 ns. The design of the dead time is beyond the scope of this paper, so this design is not explained in detail.

Fig. 4.14 depicts the prototypes of the inverter-side inductors $L$ under different conditions of the inductor impedance $\%Z_L$. Note that in the $LCL$

TABLE 4.2.
MINIMUM REQUIRED DEAD TIME IN CONSIDERATION OF MAXIMUM DRAIN CURRENT, GATE RESISTOR, AND MAXIMUM AMBIENT TEMPERATURE.

| Ambient temperature [$^{o}$C] | 25 | 25 | 25 | 50 |
|---|---|---|---|---|
| Maximum current [A] | 18 | 60 | 60 | 60 |
| Gate resistor [Ω] | 0 | 0 | 3 | 3 |
| $t_{d(GDU)}$ [ns] | 100 | 100 | 100 | 100 |
| $t_{d(off)}$ [ns] | 48 | 48 | 48 | 48 |
| $t_f$ [ns] | 27 | 67 | 90 | 180 |
| $T_{d_min}=t_{d(GDU)}+t_{d(off)}+t_f$ | 175 | 215 | 238 | 328 |

filter design, the inductor impedance, which is normalized by the inverter total impedance, is generally used to compare the inductance. Ferrite is chosen to be the core material in order to minimize the core loss at the switching frequency of 100 kHz, whereas Litz wire is used to minimize the winding loss coming from the proximity effect and the skin effect [4-37]. The inverter-side inductor impedance is minimized with the consideration of the increase in the conduction loss of the switching devices due to the high inductor current ripple [4-30]. It can be observed that the inductor volume (including bobbins) is reduced by 51% when the inverter-side inductor impedance $\%Z_L$ is reduced from 1.8% to 0.5%. Note that the

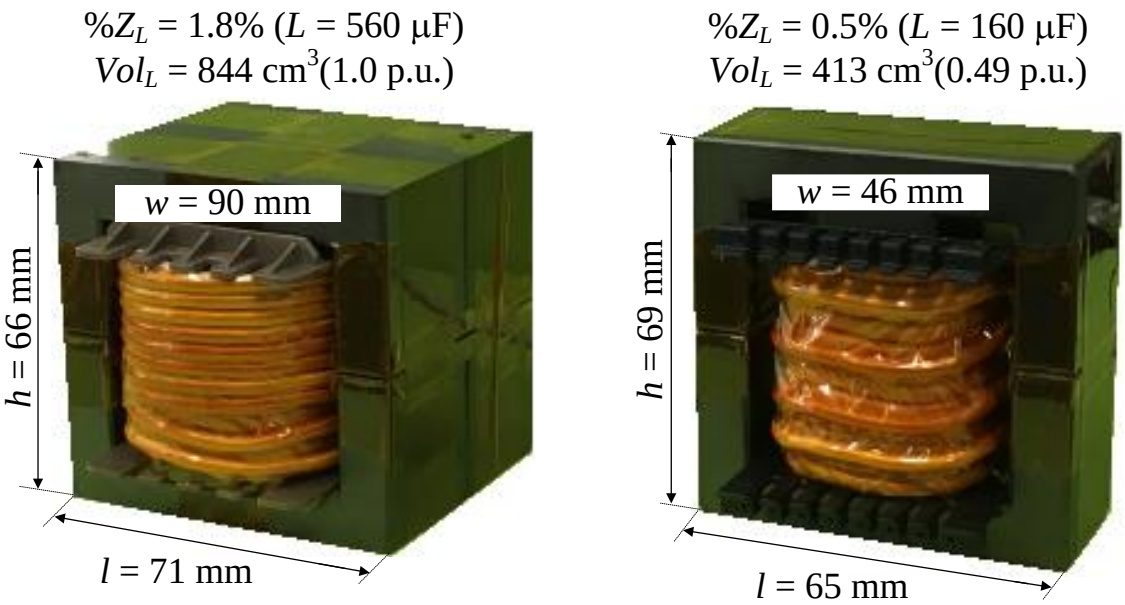


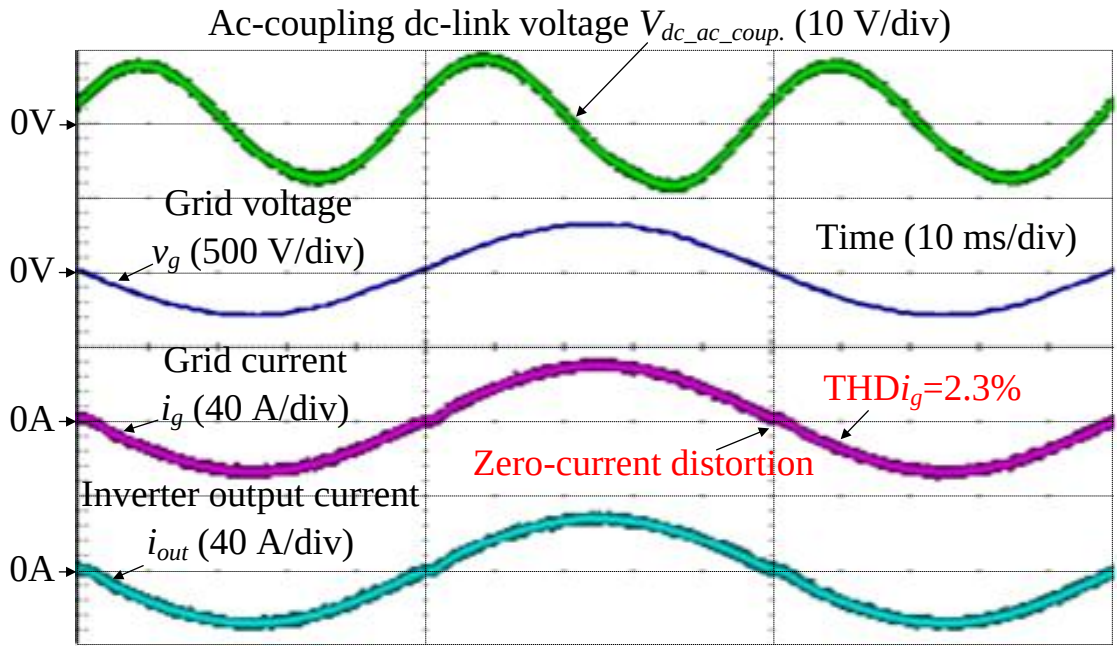

Fig. 4.14. Prototypes of inverter-side inductors under different conditions of inductor impedance. Note that only one inductor in one line indicated by $L/2$ in Fig. 4.1 is shown, whereas the impedance, the inductance and the inductor volume (including bobbins) are calculated from two inductors in two lines. In particular, the inductor volume is reduced by 51% due to the reduction of the inverter-side inductor impedance %$Z_L$ from 1.8% to 0.5%.

minimization of the inverter-side inductor impedance is also restricted due to the practical limits of the sampling frequency, the current sensor measurement, and the current control bandwidth. For instance, the grid-tied inverter is required to meet the fault-ride-through (FRT) requirements of the grid code [4-38]; one of the regulations is that the current overshoot rate below 150% of the maximum current at rated load must be maintained even when the grid faults occur, e.g. the short-circuit of the grid. In the

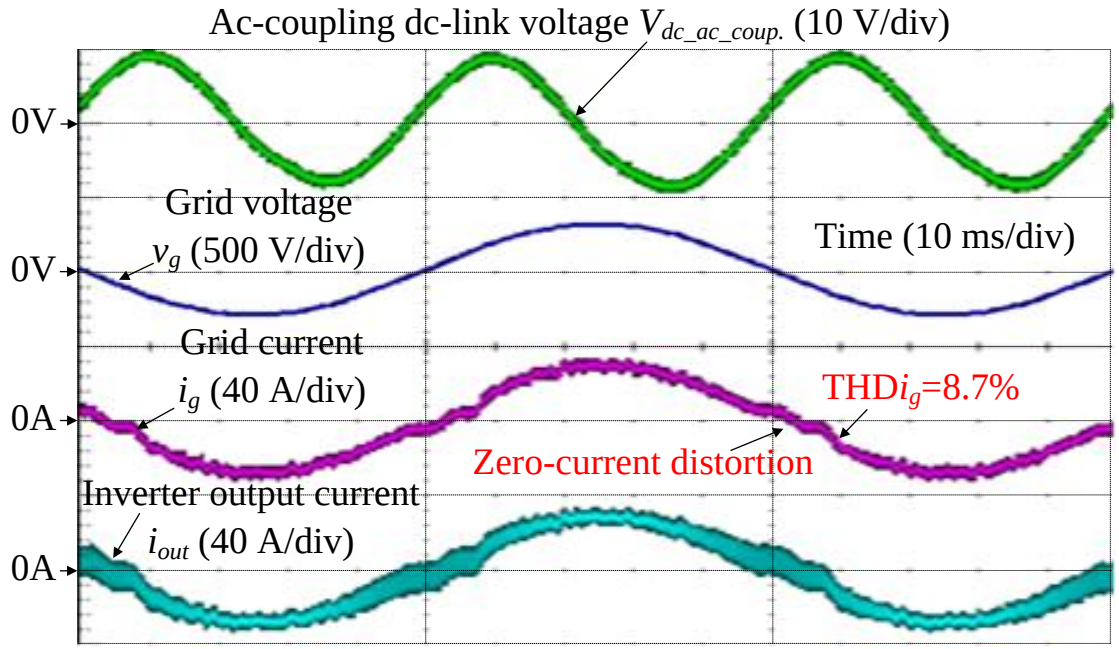
practical application, there is delay time in the current detection due to the current sensor or the sampling frequency. Consequently, the smaller the inductance is reduced, the more difficult it becomes to achieve the current overshoot rate during the grid faults below 150% of the maximum current at the rated load.

### 4.4.2 Operation Verification

Fig. 4.15 describes the inverter operation waveforms with the conventional CCM current control at a rated load of 4 kW and at a light load of 2 kW under two conditions of $\%Z_L$. Fig. 4.15(a)-(b) shows the operation waveforms at the rated load of 4 kW, whereas Fig. 4.15(c)-(d) shows the operation waveforms at the light load of 2 kW. Fig. 4.15(a), (c) shows the operation waveforms with $\%Z_L$ of 1.8%, whereas Fig. 4.15(b), (d) shows the operation waveforms with $\%Z_L$ of 0.5%. The grid current THD (up to $40^{th}$ order of the harmonic component) is measured by a YOKOGAWA WT1800 power meter. As mentioned in section 4.2, the length of the zero-current clamping interval depends on the current ripple of the inverter output current $i_{out}$, the dead-time-to-switching-period ratio, and the power level. Note that the low-inductance design leads to the high switching current ripple; therefore, when $\%Z_L$ is reduced from 1.8% to 0.5%, the grid current THD at the rated load of 4 kW increases from 2.3% to 8.7% as shown in Fig. 4.15(a)-(b). Similarly, comparing Fig. 4.15(a)-(b) with Fig. 4.15(c)-(d), when the power level decreases from 4 kW to 2 kW, the grid current THD increases from 2.3% and 8.7% to 3.9% and 12.4%,

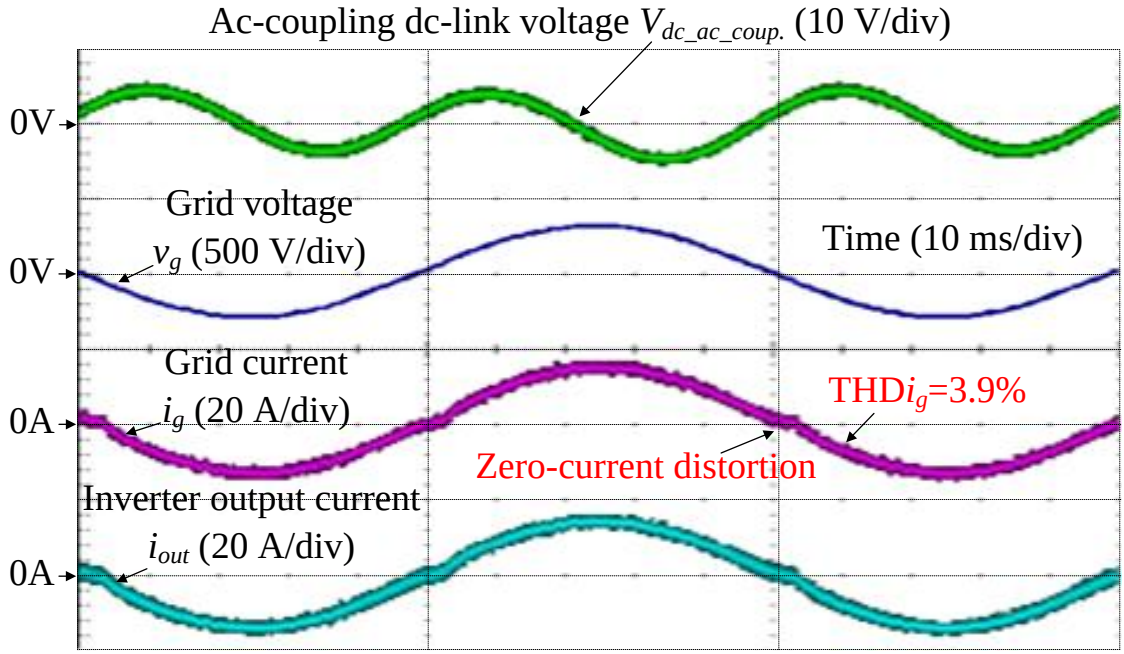



(4.15.a) Conventional CCM control, %$Z_L$=1.8%, rated load of 4 kW

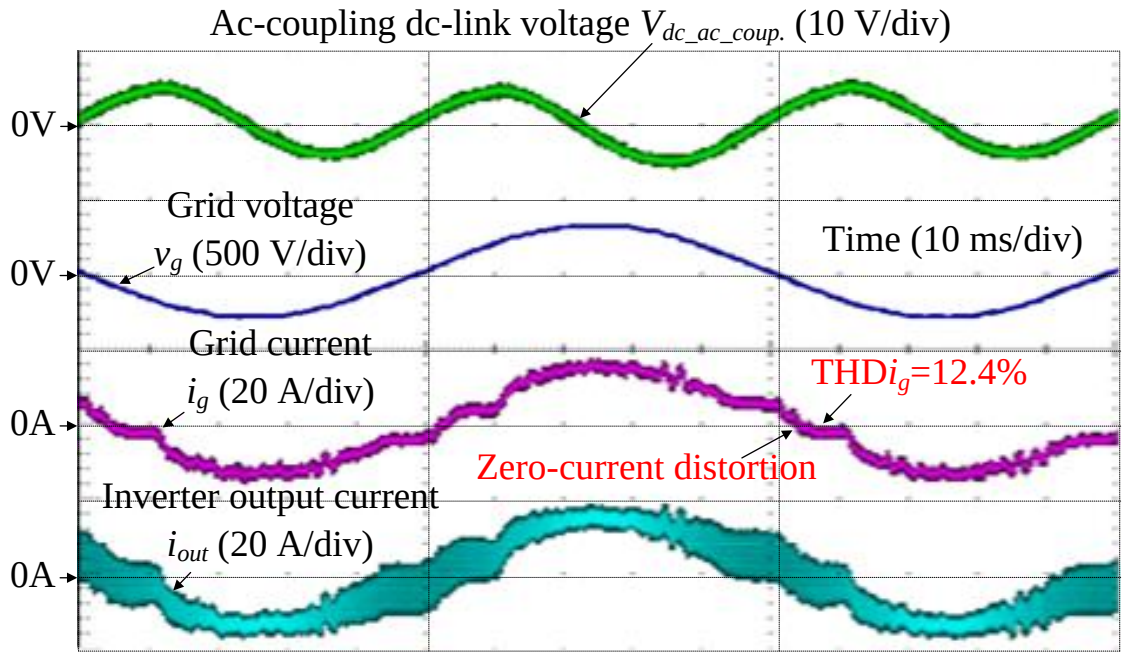



(4.15.b) Conventional CCM control, %$Z_L$=0.5%, rated load of 4 kW

respectively. According to standards such as IEEE-1547 [4-1], the grid




(4.15.c) Conventional CCM control, %$Z_L$=1.8%, light load of 2 kW




(4.15.d) Conventional CCM control, %$Z_L$=0.5%, light load of 2 kW

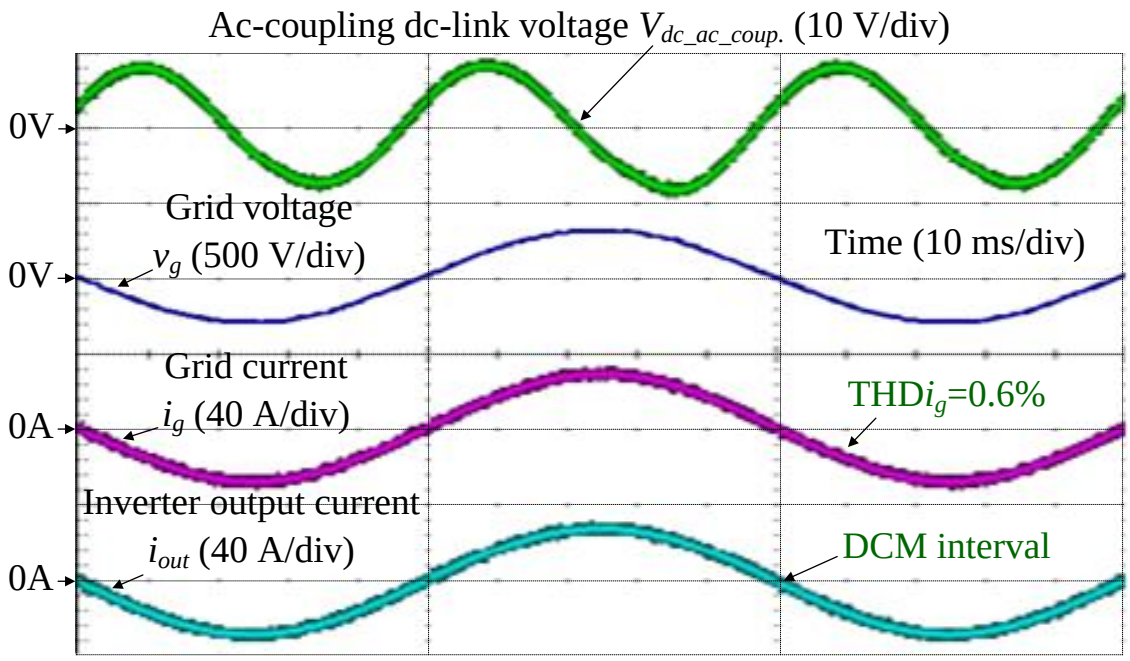
Fig. 4.15. Operation waveforms of conventional CCM control at rated load of 4 kW and at light load of 2 kW under two conditions of %$Z_L$. The low-inductance design results in the high current ripple, which increases the zero-current distortion with the conventional CCM control. Consequently, the grid current THD of 8.7% at the rated load with %$Z_L$ of 0.5% does not satisfy the harmonic constraint regulated by standards.

current THD at the rated load must be lower than 5%; hence, the inductor

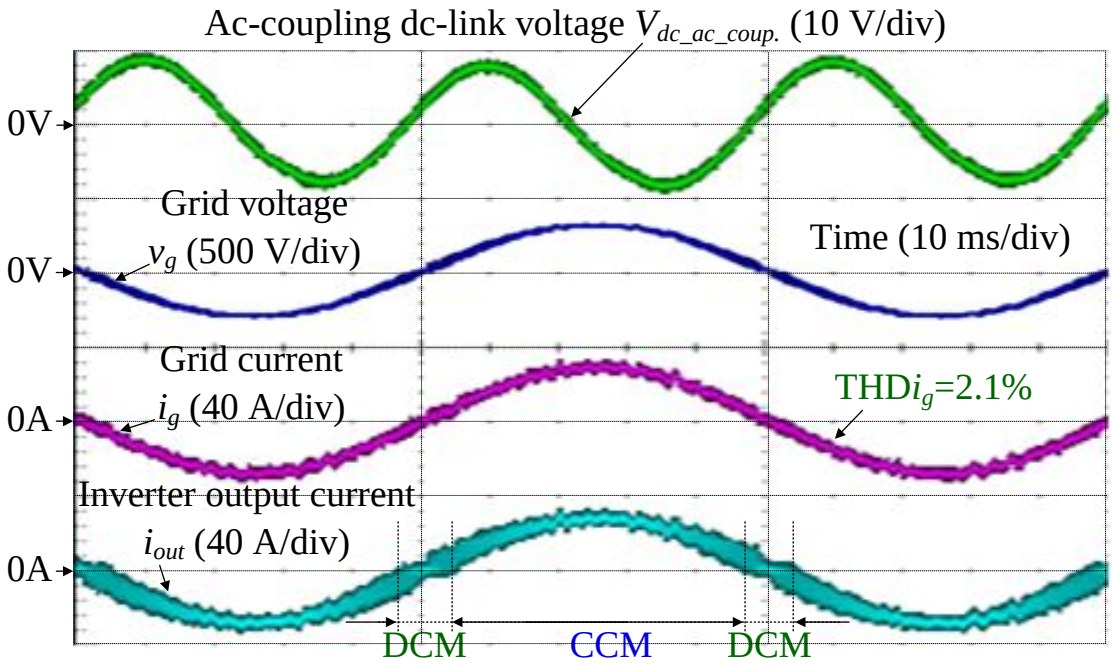
impedance design of 0.5% with the conventional CCM current control system, of which the grid current THD at the rated load is 8.7%, does not satisfy the harmonic constraint. Consequently, it is confirmed by experimental results that the inductance reduction with the conventional CCM current control, of which the aim to achieve the small volume and low cost of the inductors, is limited due to the zero-current distortion.

Fig. 4.16 describes the inverter operation waveforms with the proposed CCM&DCM current control at the rated load of 4 kW and at the light load of 2 kW under two conditions of $\%Z_L$. Fig. 4.16(a)-(b) shows the operation waveforms at the rated load of 4 kW, whereas Fig. 4.16(c)-(d) shows the operation waveforms at the light load of 2 kW. Fig. 4.16(a), (c) shows the operation waveforms with $\%Z_L$ of 1.8%, whereas Fig. 4.16(b), (d) shows the operation waveforms with $\%Z_L$ of 0.5%. It can be observed clearly from Fig. 4.16(b), (d) that the inverter is intentionally operated under DCM in the vicinities of the zero-current crossing. Due to the DCM nonlinearity compensation, the same current dynamic as CCM is achieved during the DCM interval; hence, the zero-current distortion is eliminated. In particular, the proposed CCM&DCM current control reduces the grid current THD at

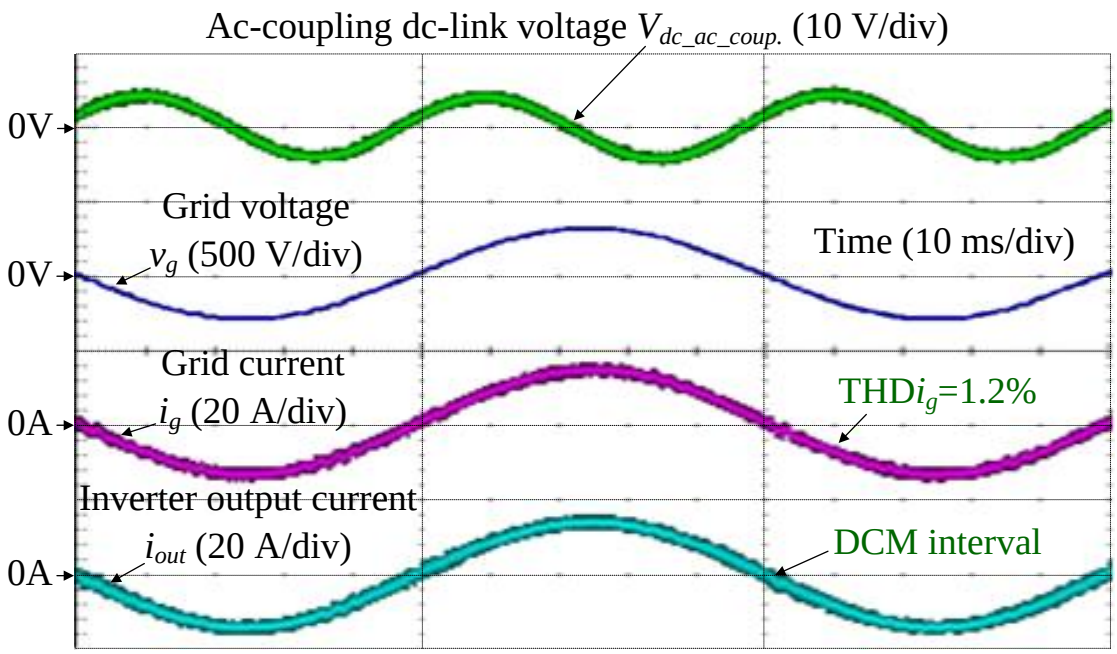
the rated load from 8.7% to 2.1% compared to that of the conventional



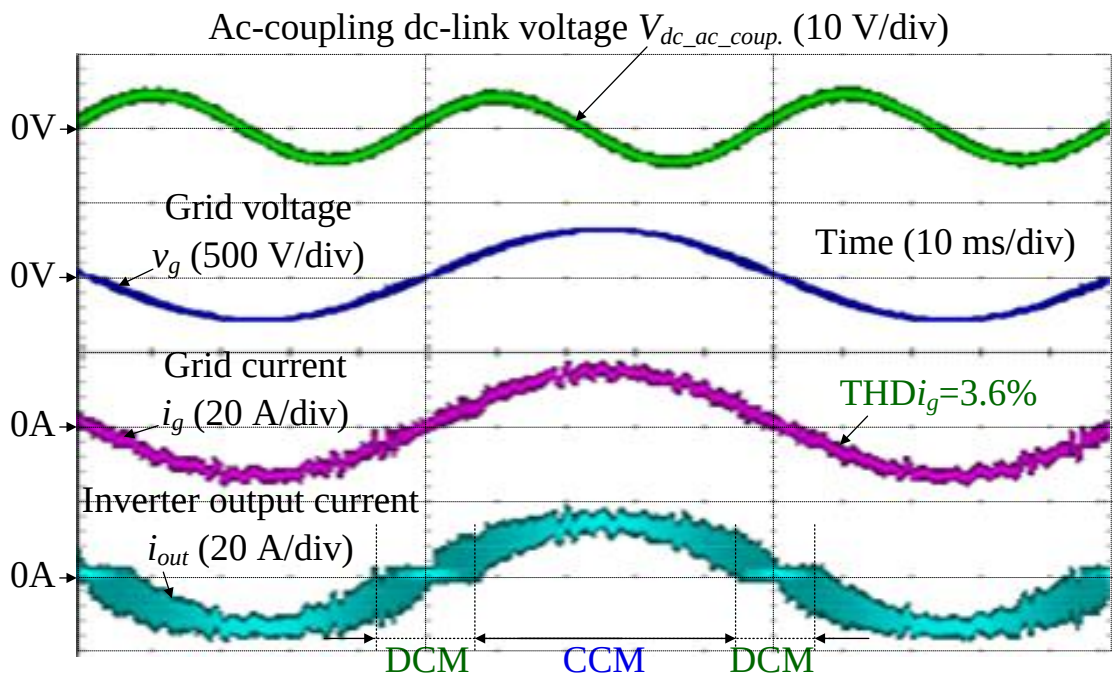

(4.16.a) Proposed CCM&DCM control, %$Z_L$=1.8%, rated load of 4 kW




(4.16.b) Proposed CCM&DCM control, %$Z_L$=0.5%, rated load of 4 kW




(4.16.c) Proposed CCM&DCM control, %$Z_L$=1.8%, light load of 2 kW

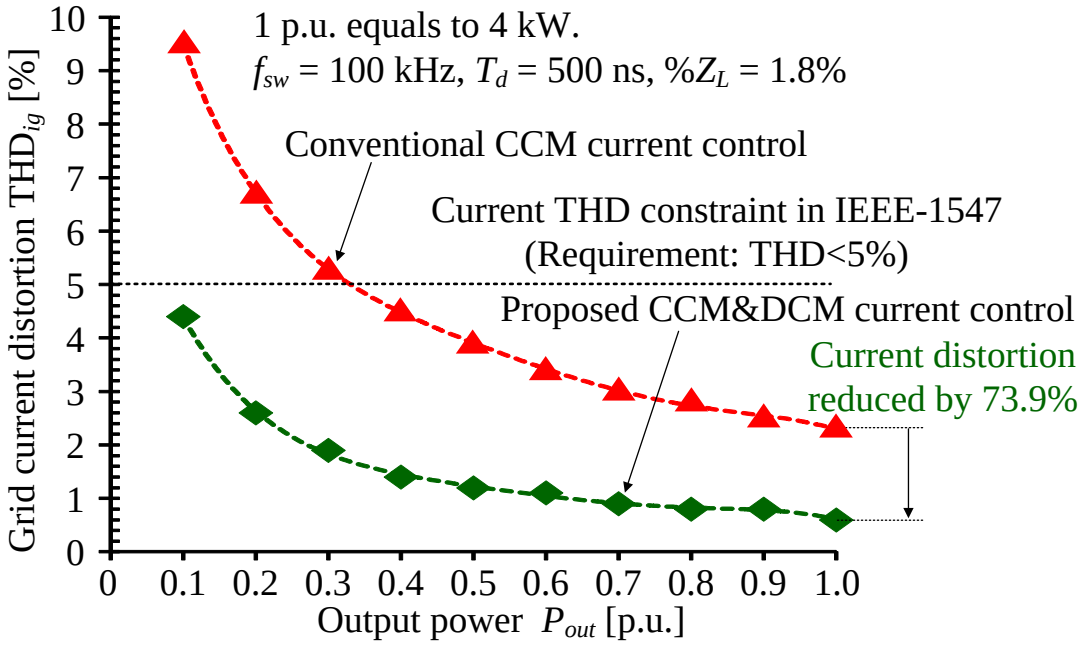



(4.16.d) Proposed CCM&DCM control, %$Z_L$=0.5%, light load of 2 kW

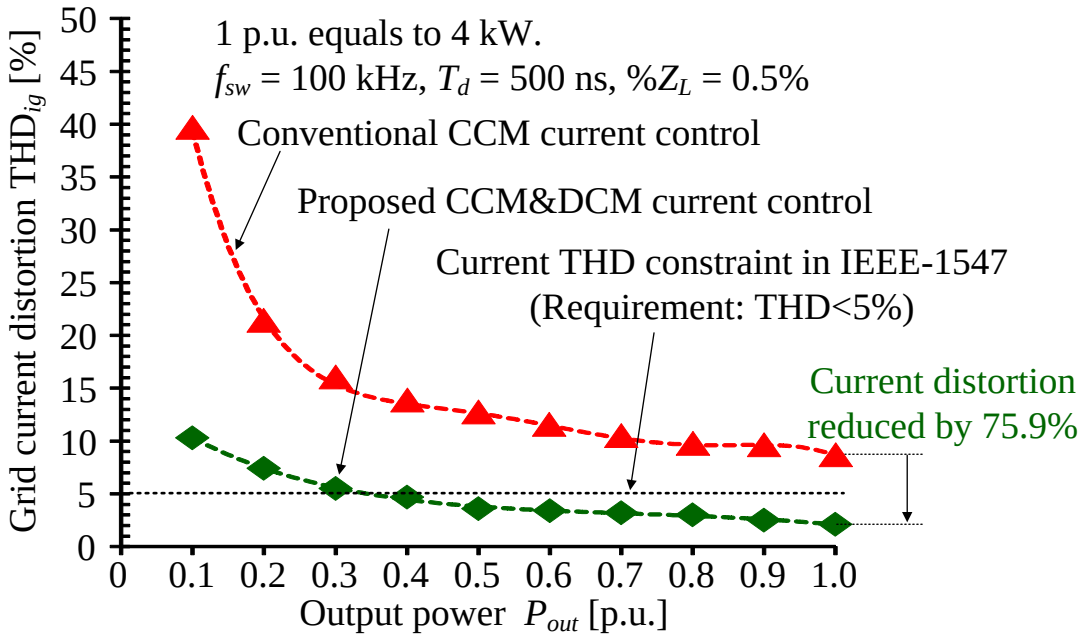
Fig. 4.16. Operation waveforms of proposed CCM&DCM control at rated load of 4 kW and at light load of 2 kW under two conditions of %$Z_L$. Even with %$Z_L$ of 0.5%, the proposed CCM&DCM current control can still maintain the grid current THD at the rated load below 5%, which satisfies the harmonic constraint regulated by standards such as IEEE-1547 [1].

CCM current control with %$Z_L$ of 0.5%. Therefore, the proposed CCM&DCM current control enables the minimization of the inverter-side inductor impedance without violating the harmonic constraint regulated by standards such as IEEE-1547 [4-1].

Fig. 4.17 depicts the comparison of the grid current THD and the power factor characteristics of the conventional CCM current control and the proposed CCM&DCM current control. Fig. 4.17(a)-(b) shows the grid current THD with %$Z_L$ of 1.8% and 0.5%, whereas Fig. 4.17(c)-(d) shows the power factor with %$Z_L$ of 1.8% and 0.5%, respectively. In Fig. 4.17(a)-(b), the proposed CCM&DCM current control reduces the current distortion at the rated load by 73.9% and 75.9% with %$Z_L$ of 1.8% and 0.5% compared to those of the conventional CCM current control, respectively. Moreover, the grid current THD over entire load range from 0.1 p.u. to 1.0 p.u. is reduced with the proposed CCM&DCM current control. Consequently, the power factors of the proposed CCM&DCM current control over entire load range from 0.1 p.u. to 1.0 p.u. with %$Z_L$ of 1.8% and 0.5% are improved compared to those of the conventional CCM current control as shown in Fig. 4.17(c)-(d), respectively. In particular, the

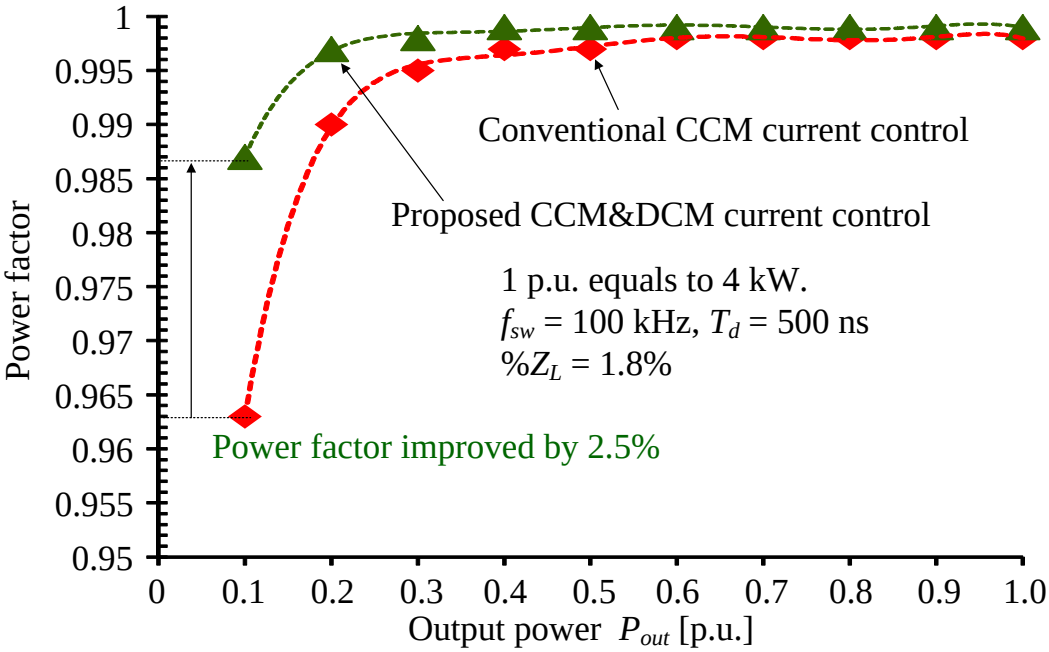



(4.17.a) Grid current THD characteristic of %$Z_L$=1.8%

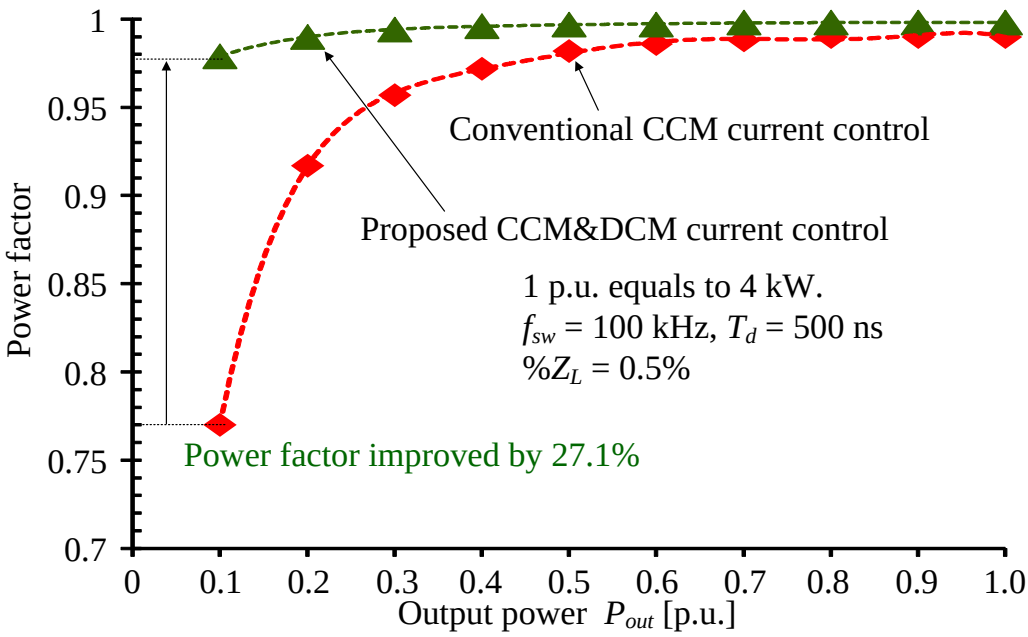



(4.17.b) Grid current THD characteristic of %$Z_L$=0.5%

power factor at the light load of 0.1 p.u. with %$Z_L$ of 0.5% is improved by 27.1% when the proposed CCM&DCM current control is applied.



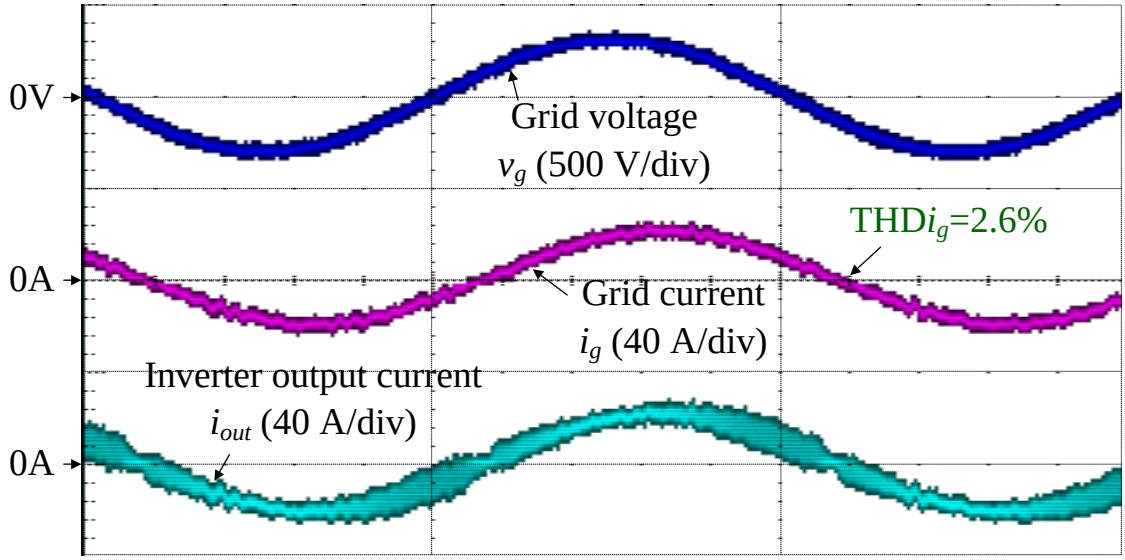

(4.17.c) Power factor characteristic of %$Z_L$=1.8%



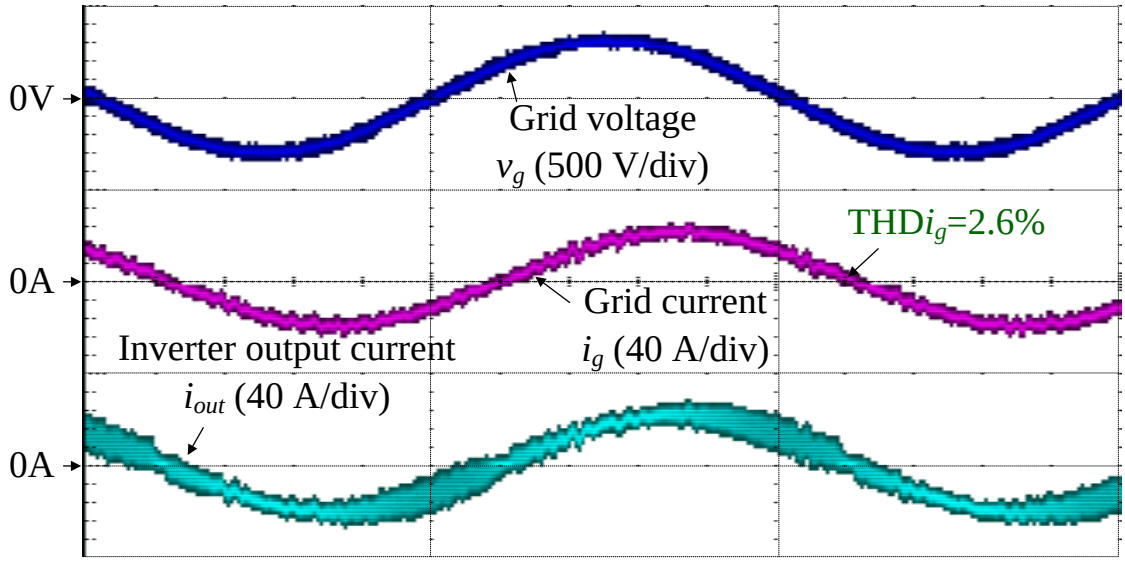

(4.17.d) Power factor characteristic of %$Z_L$=0.5%

Fig. 4.17. Grid current THD and power factor characteristics of conventional CCM current control and proposed CCM&DCM current control. The proposed CCM&DCM current control reduces the current distortion at the rated load by 73.9% and 75.9% with %$Z_L$ of 1.8% and 0.5% compared to those of the conventional CCM current control, respectively. Furthermore, the power factors of the proposed CCM&DCM current control over entire load range from 0.1 p.u. to 1.0 p.u. with %$Z_L$ of 1.8% and 0.5% are also improved compared to those of the conventional CCM current control.

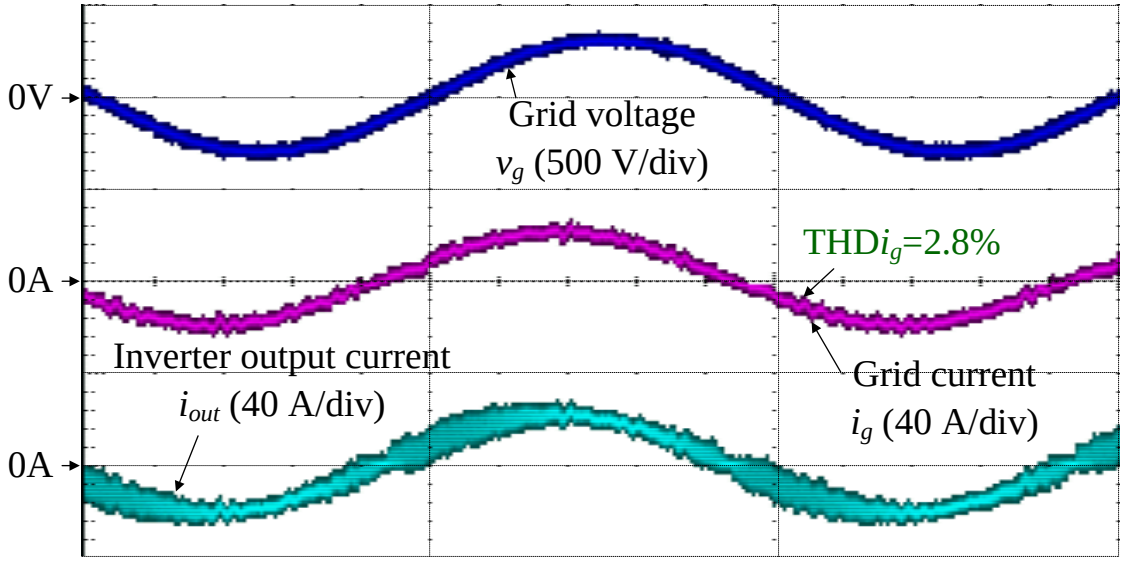
Fig. 4.18 describes the inverter operation waveforms with the proposed CCM&DCM current control under low power factor with %$Z_L$ of 0.5%. During normal operation, the grid-tied inverter is required to operate at



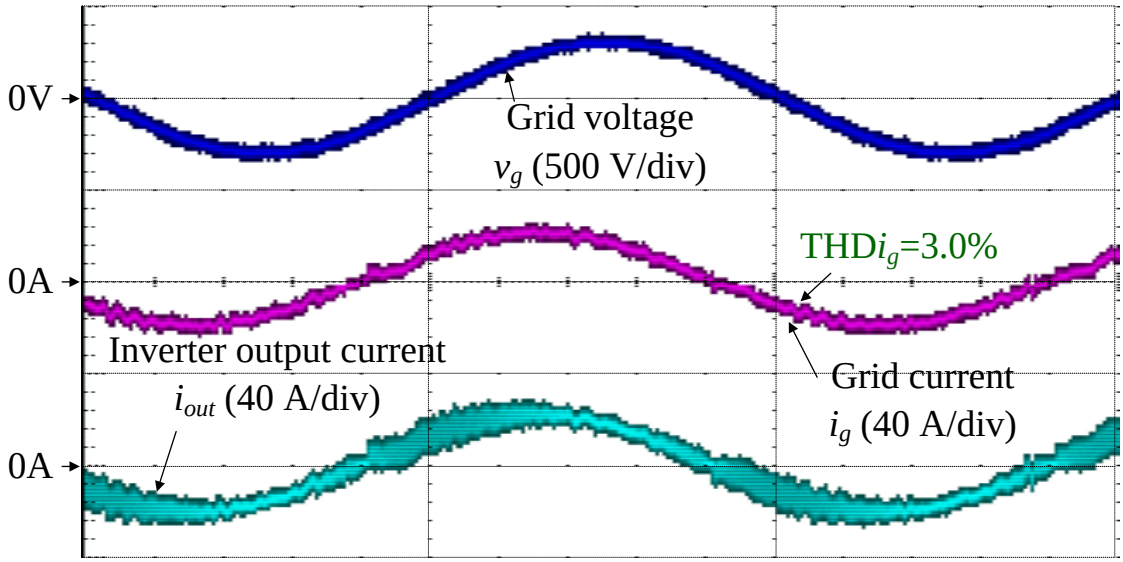

(4.18.a) Inverter operation with low power factor of 0.9 (Lagging)




(4.18.b) Inverter operation with low power factor of 0.8 (Lagging)




(4.18.c) Inverter operation with low power factor of 0.9 (Leading)



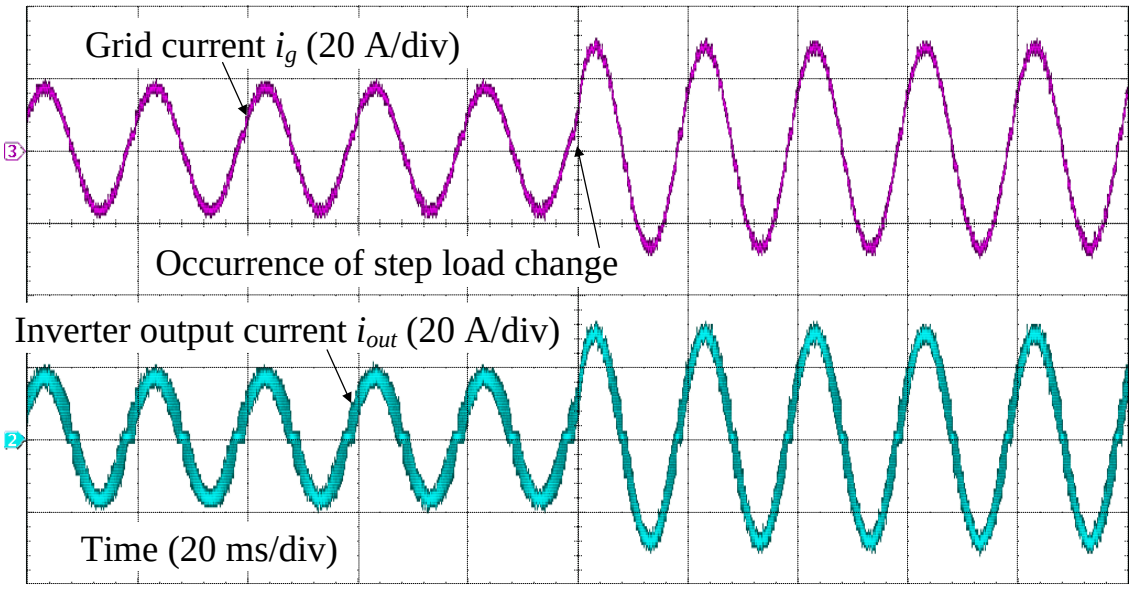

(4.18.d) Inverter operation with low power factor of 0.8 (Leading)

Fig. 4.18. Proposed CCM&DCM current control operation under low power factor with %$Z_L$ of 0.5%. When the grid variations occur, i.e. frequency instability or grid voltage sag, the grid-tied inverter is necessary to operate under a low power factor in order to avoid more serious events, e.g. power outage or voltage flickering.

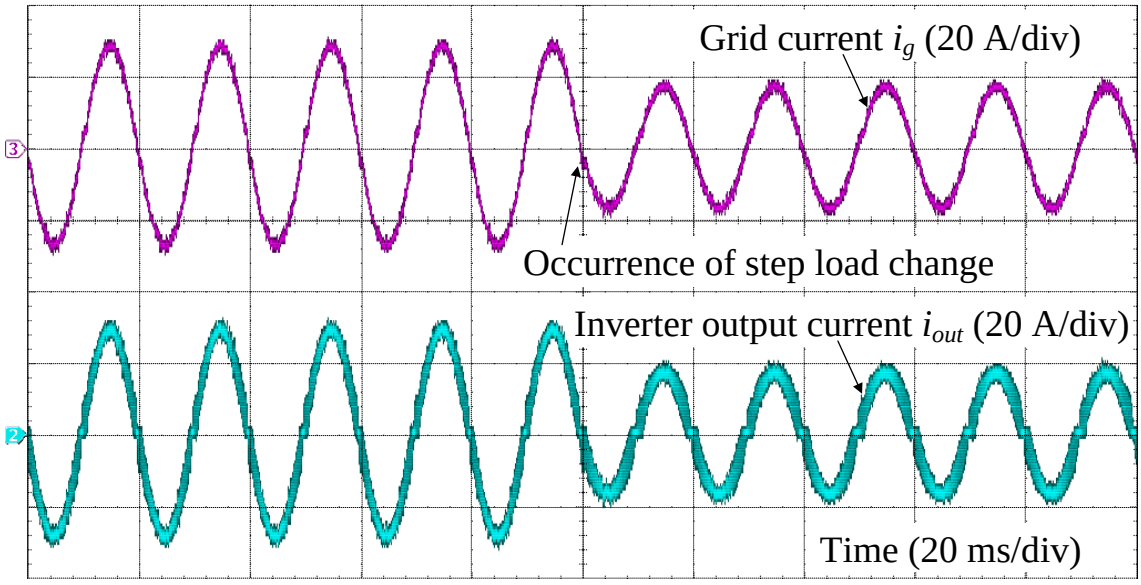
unity power factor with maximum power point tracking in order to extract as much energy as possible from the PV panels [4-32]. However, when the

grid variations occur, i.e. frequency instability or grid voltage sag, the grid-tied inverter is also necessary to operate under low power factor [4-33]. As shown in Fig. 4.18, the proposed CCM&DCM current control still maintains a low grid current THD under the low power factor.

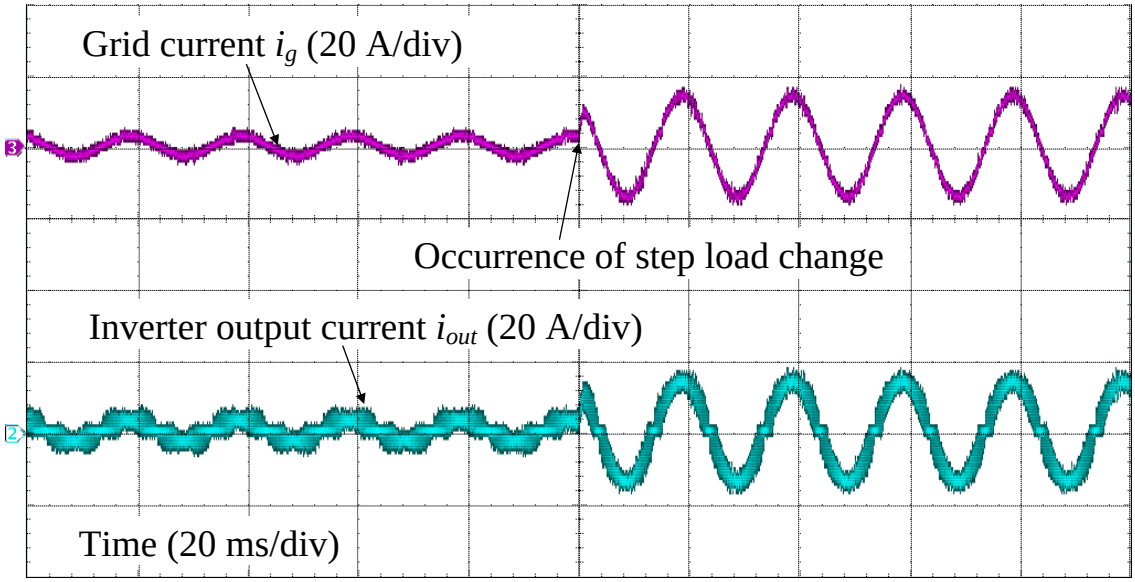
Fig. 4.19 describes the inverter operation waveforms with the proposed CCM&DCM current control under step load change with $\%Z_L$ of 0.5%. Fig. 4.19 (a)-(b) shows the current response with the step load change from 60% to 100% and vice versa, whereas Fig. 4.19 (c)-(d) depicts the current response with the step load change from 10% to 50% and vice versa, respectively. Note that the step load change in Fig. 4.19 (a)-(b) occurs in the vicinities of the zero-current crossing, i.e. the DCM interval, whereas the step load change in Fig. 4.19 (c)-(d) occurs at the current peak, i.e. the CCM interval. It is observed that the transient waveform has low overshoot and fast convergence regardless of the moment of the step load change occurrence.



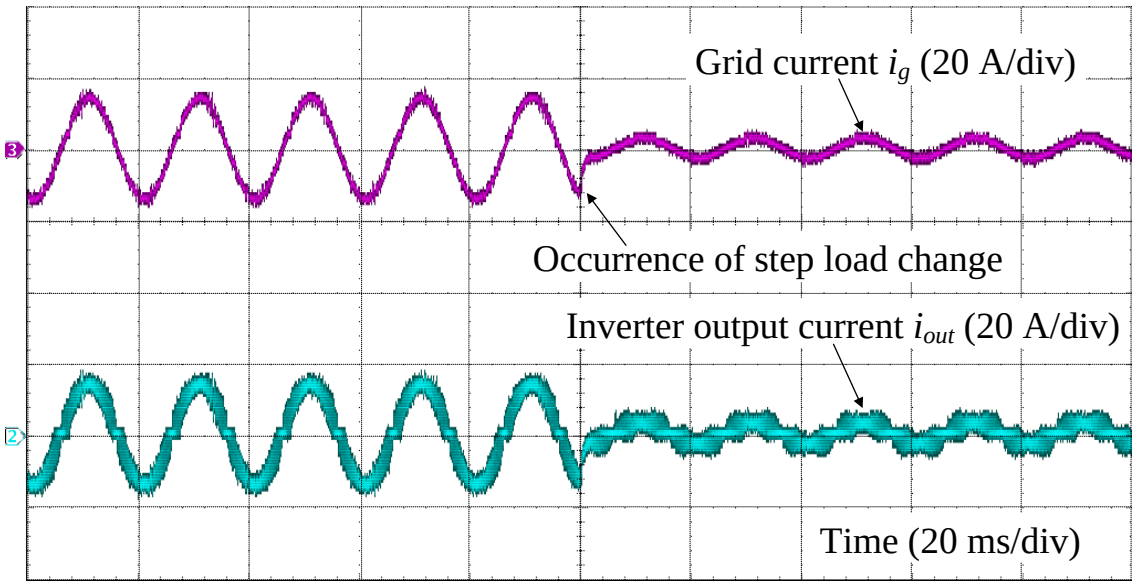

(4.19.a) Current response with step-up load change from 60% to 100%




(4.19.b) Current response with step-down load change from 100% to 60%




(4.19.c) Current response with step-up load change from 10% to 50%

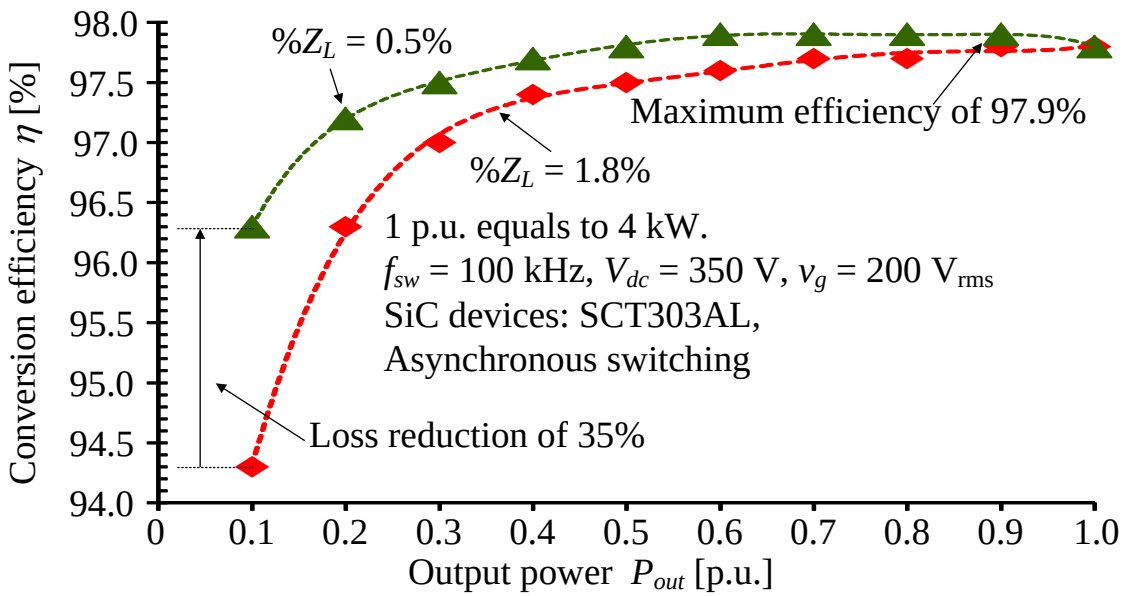



(4.19.d) Current response with step-down load change from 50% to 10%

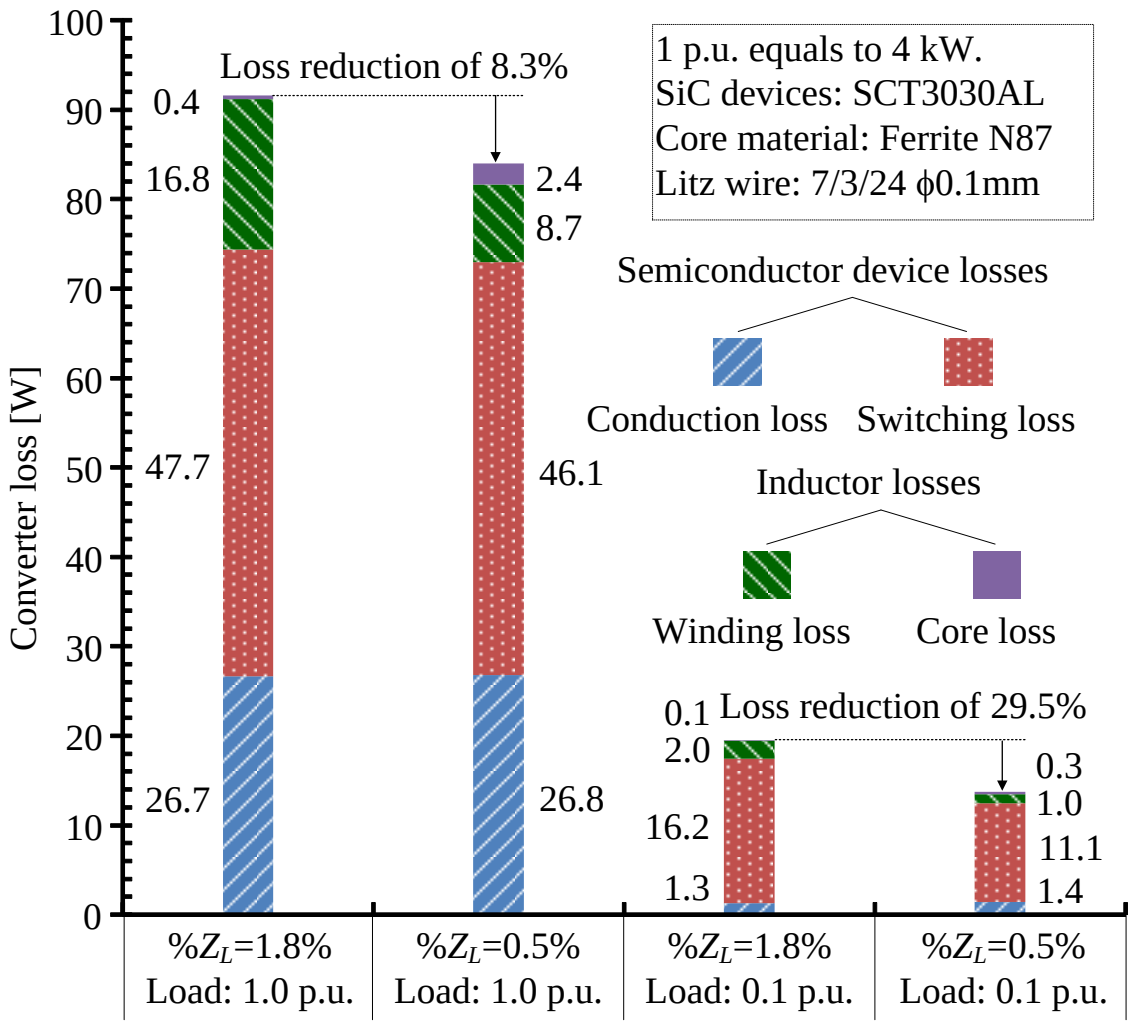
Fig. 19. Proposed CCM&DCM current control operation under step load change with $\%Z_L$ of 0.5%. The transient waveform has low overshoot and fast convergence when the step load change occurs either in the vicinities of the zero-current crossing, i.e. the DCM interval, or at the current peak, i.e. the CCM interval.

### 4.4.3 Comparison of Efficiency, Inductor Material Cost and Computation Time

Fig. 4.20 depicts the efficiencies and the loss distribution with the proposed CCM&DCM current control with $\%Z_L$ of 1.8% and 0.5%. The efficiencies are measured by a YOKOGAWA WT1800 power meter, whereas the semiconductor device losses and the inductor losses are obtained from simulators, i.e. PLECS and GeckoMAGNETICS. In Fig. 4.20(a), the maximum efficiency of 97.9% is achieved with $\%Z_L$ of 0.5% from the load range of 0.6 p.u. to 0.9 p.u., whereas the efficiency at the rated load of 4 kW is 97.8%. The efficiency with $\%Z_L$ of 0.5% is higher




(4.20.a) Efficiency characteristics




(4.20.b) Loss distribution

Fig. 4.20. Efficiency and loss distribution with proposed CCM&DCM current control with %$Z_L$ of 1.8% and 0.5%. The maximum efficiency of 97.9% is achieved over a wide load range from 0.6 p.u. to 0.9 p.u.. The switching loss and conduction loss of SiC devices occupies for a majority of the converter loss. Therefore, the efficiency might be further improved by the application of GaN devices to reduce the switching loss and the employment of the synchronous switching to reduce the conduction loss.

than that with %$Z_L$ of 1.8% over entire load range; in specific, the loss at the light load of 0.1 p.u. with %$Z_L$ of 0.5% is reduced by 35% compared to

that with %$Z_L$ of 1.8%. This efficiency improvement especially benefits the PV application with a frequent variation between the light load operation and the heavy load operation. In Fig. 4.20(b), the converter losses with %$Z_L$ of 1.8% and 0.5% at the rated load of 1.0 p.u. and the light load of 0.1 p.u. are demonstrated. At the rated load of 1.0 p.u., compared to %$Z_L$ of 1.8%, the conduction loss and the core loss with %$Z_L$ of 0.5% increase, whereas the switching loss and the winding loss with %$Z_L$ of 0.5% decrease. The increase in the conduction loss and the core loss occurs due to the increase of the current ripple when %$Z_L$ is reduced from 1.8% to 0.5%. On the other hand, the reduction of %$Z_L$ requires less winding wire in the inductor; consequently, the winding loss of the inductor decreases. Regarding to the switching loss, there are two main factors causing the decrease in the switching loss when %$Z_L$ is reduced from 1.8% to 0.5%: the increase in the current ripple, and the DCM operation in the vicinities of the zero-current crossing. First, compared to the low current ripple, the high current ripple makes the semiconductor devices turn off at higher current and turn on at lower current, which results in the increase in the turn-off switching loss and the decrease in the turn-on switching loss. In SiC-MOSFET, the

turn-on switching loss is usually higher than the turn-off switching loss due to the occurrence of the diode reverse recovery and the parasitic capacitance discharge at the turn on. Hence, the increase in the current ripple benefits the reduction in the switching loss. Second, during the DCM operation, the turn-on loss is significantly reduced due to zero-current turn-on. Hence, the increase in the current ripple results in longer DCM intervals around the zero-current crossing points, which helps to reduce the switching loss. This switching loss reduction effect with the DCM operation is clearly observed at the light load of 0.1 p.u., where the DCM interval becomes longer. In particular, at the light load of 0.1 p.u., compared to $\%Z_L$ of 1.8% (low current ripple, short DCM intervals), the switching loss of $\%Z_L$ of 0.5% (high current ripple, long DCM intervals) is reduced from 16.2 W to 11.1 W. Furthermore, it can be concluded from Fig. 4.20(b) that the switching loss and conduction loss of SiC devices occupies for a majority of the converter loss. Therefore, the efficiency might be further improved by the application of GaN devices to reduce the switching loss and the employment of the synchronous switching to reduce the conduction loss. Note that the difference in the loss reduction between Fig.

4.20(a) and (b), occurs due to the loss calculation error in the simulators.

Fig. 4.21 describes the cost breakdown of the inverter-side inductor material under two designs of $\%Z_L$. The ferrite core material can provide a lower core loss at the high switching frequency of several hundreds of kHz compared to other core materials such as, e.g. silicon steel, amorphous iron or nanocrystals [4-41]-[4-42]. Nevertheless, a ferrite characteristic of a low saturation flux density requires a large amount of the core material. Consequently, the core material cost dominates the overall inductor

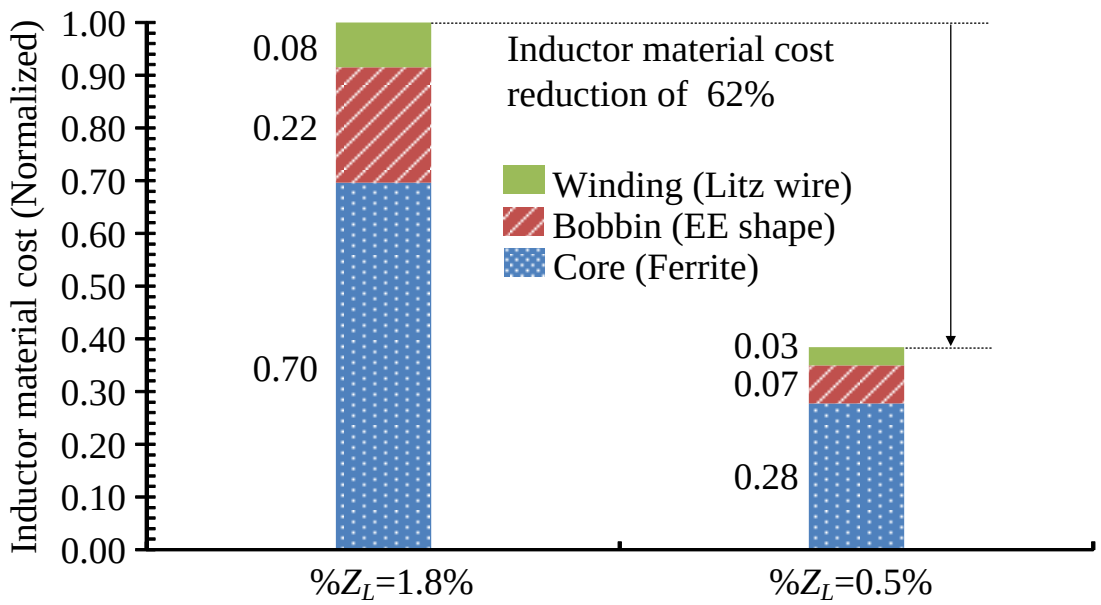



Fig. 4.21. Cost breakdown of inverter-side inductor material under two designs of $\%Z_L$. A cost reduction of 62% in the inductor material is achieved when decreasing the inverter-side inductor impedance from 1.8% to 0.5%. Note that the cost calculation is based on the actual price of the prototype components, and is normalized by the $\%Z_L$ design of 1.8%.

material cost. Furthermore, a cost reduction of 62% in the inductor material is achieved with the decrease in the inverter-side inductor impedance from 1.8% to 0.5%.

Table 4.3 shows the approximate computation time for all the arithmetic operations in three current control loops shown in Fig. 4.12. Both division and square root digital calculations are time-consuming computation involving multiple clock cycles. In particular, when a STM32 Cortex-M4 microcontroller is applied to process 32-bit floating-point single-precision data, 14 clock cycles are required for a division or square root calculation, whereas 1 clock cycle is required for an addition or subtraction and 3 clock cycles are required for a multiplication [4-43]. Note that the computation time for the division calculations can be shorten by using a look-up table [4-44]. In the conventional CCM current control, only additions and multiplication are required for three operations, i.e. the PI controller, the grid voltage feedforward and the dead-time compensation. Therefore, the computation time of the conventional CCM current control is the shortest with 27 clock cycles. In the conventional CCM&DCM current control, a square root calculation is required to compute the DCM

duty ratio as shown in Fig. 4.12(b), and two additional operations, i.e. the DCM duty generation and the current mode determination, are necessary. Meanwhile, in the proposed CCM&DCM current control, a square root calculation is unnecessary; however, multiple additions and multiplications are required in order to generate the DCM duty as shown in Fig. 4.12(c). Therefore, the computation time of the conventional and proposed CCM&DCM current control becomes approximately 3 times longer than

TABLE 4.3.
COMPUTATION TIME IN CLOCK CYCLES OF CURRENT CONTROL LOOP.

| Computation time [clock cycles] | Conventional CCM control (cf. Fig. 4.12(a)) | Conventional CCM/DCM control (cf. Fig. 4.12(b)) | Proposed CCM/DCM control (cf. Fig. 4.12(c)) |
|---|---|---|---|
| PI controller | 15 | 15 | 15 |
| Grid voltage feedforward | 4 | 0 | 0 |
| CCM duty generation | 0 | 8 | 9 |
| DCM duty generation | 0 | 36 | 37 |
| Current mode determination | 0 | 12 | 12 |
| Dead-time compensation | 8 | 8 | 8 |
| Total | 27 (1 p.u.) | 79 ( 2.9 p.u. ) | 81 (3.0 p.u.) |

that of the conventional CCM current control. Hence, the minimization of the inverter-side inductor is a trade-off between the computation time and the grid current THD.

## 4.5 Conclusion

This chapter presented a current mode control for the single-phase grid-tied inverter operating in both CCM and DCM in order to reduce the filter inductance without worsening the grid current THD. The proposed CCM&DCM current control satisfied the harmonic constraint defined in the grid standard such as IEEE-1547 even when the inverter-side inductor impedance is significantly reduced from 1.8% to 0.5%. The proposed CCM&DCM current control was compared with the conventional CCM current control and the conventional CCM&DCM current control.

First, with the employment of the conventional CCM current control, the grid current THD increased from 2.3% to 8.7% due to the zero-current clamping phenomenon when the inductor impedance was minimized from 1.8% to 0.5%. The conventional CCM current control could not compensate for the DCM nonlinearity to maintain the same current dynamic when the zero-current clamping occurred. On the other hand, the proposed CCM&DCM current control compensated for the DCM nonlinearity and reduced the grid current THD from 8.7% to 2.1% even with the low inductor impedance of 0.5%. Consequently, this inductor

impedance minimization achieved the reductions of 51%, 62% and 35% in the inductor volume, the inductor material cost and the inverter loss at the light load of 0.1 p.u., respectively. However, these improvements was traded off by the long computation time of the proposed CCM&DCM current control which was 3 times longer than that of the conventional CCM current control.

Second, in the conventional CCM&DCM current control, the inductance must be used in the DCM nonlinearity compensation, which made the control system dependent on the circuit parameter. This restricted the application of the conventional CCM&DCM current control method to the residential PV systems, where the accurate value of the inductance was generally difficult to obtain. On the other hand, the proposed CCM&DCM current control utilized the duty ratio at the previous calculation in order to both compensate for the DCM nonlinearity and detect the current modes regardless of the inductance.

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# Chapter 5

# Control for Discontinuous Current Mode in Three-Phase Grid-Tied Inverter

## 5.1 Introduction

This chapter presents a current control for the three-phase grid-tied inverter operated in discontinuous current mode to minimize the grid filter without worsening the current distortion. In order to deal with the zero-current clamping effect, the inverter is intentionally operated in DCM instead of CCM. In other words, the zero-current interval with the DCM operation is controlled, enabling a proper compensation for the nonlinear behavior. Consequently, the conventional dead-time feedforward compensation, i.e. two-level ACM, can be employed simply in order to

compensate the dead-time-induced error voltage and reduce the current distortion. The novelty of the proposed DCM control method is that the control of each phase current is separated into individual intervals in order to avoid the interference between the phase currents. Therefore, the proposed DCM control method without the interference decoupling simply achieves the sinusoidal current regulation in numerous applications. This chapter is organized as follows; in section 5.2, first, the zero crossing distortion phenomenon is explained. Then, the DCM current control is proposed as the main part. After that, in section 5.3 and 5.4, the effectiveness of the proposed DCM current control is confirmed in simulation and experiments. Finally, in section 5.5, the conclusion of this chapter will be presented.

## 5.2 Current Control for Discontinuous Current Mode

This section proposes the DCM current control for the three-phase grid-tied inverter operating in DCM as the main part. First, in section 5.2.1, the zero crossing distortion phenomenon is explained, then in section 5.2.2, the derivation of the circuit model is introduced. Next, in section 5.2.3, the DCM current control is presented based on the circuit model.

### 5.2.1 Zero Crossing Distortion

In the last decade, researches on photovoltaic system (PV) have accelerated due to an increasing demand of renewable and sustainable energy sources [5-1]-[5-4]. In the PV system, H-bridge three-phase grid-tied inverters are generally employed as an interface between solar panels and three-phase grid. In such grid-tied inverters, a grid filter is required to connect between an output of the inverter and the grid in order to filter out the current harmonics and to meet grid current harmonic constraints as defined by standards such as IEEE-1547 [5-5]-[5-6]. Due to the observation that inductors in the grid filter occupy a major volume of the inverter, an inductor value of the grid filter is necessarily reduced in order to minimize the grid filter as well as the inverter. However, this

reduction of the inductor value implies a design of a high switching current ripple due to a high dc-link voltage to inductance ratio. This high current ripple results in a current distortion phenomenon called zero-current clamping, where a current distortion increases notably as the switching current ripple increases [5-7].

Due to the zero-current clamping effect, the dead-time-induced error voltage exhibits a strong nonlinear behavior around zero-current crossing points. Hence, a conventional dead-time feedforward compensation method such as, e.g. two-level approximation compensation method (ACM) [5-8], cannot compensate for this nonlinear behavior of the dead-time-induced error voltage. Several compensation methods for the nonlinearity of the dead-time-induced error voltage such as an adaptive dead-time compensation method and a turn-off transition compensation method have been proposed to deal with this nonlinearity behavior and to reduce the zero-crossing current distortion [5-9]-[5-10]. Nevertheless, both methods exhibit the requirements which restrict the employment over a wide range of application. Adjustment mechanism parameters for the adaptive dead-time compensation must be properly tuned for each individual system

[5-9]. Meanwhile, accurate device parameters, e.g. parasitic capacitances, are required for the turn-off transition compensation method [5-10].

On the other hand, a single-stage multiphase inverter is proposed with the discontinuous current mode (DCM) control in order to generate multiphase currents with only one inductor [5-11], leading to a significant inductance reduction without worsening the current total harmonic distortion (THD). However, this method requires at least one bidirectional switching device for each phase; consequently, high conduction loss of the switching devices results in low efficiency. Meanwhile, the DCM control has been also proposed for two-stage three-phase grid-tied inverters [5-12]-[5-13]. The notable drawback with these DCM control methods is that the DCM control in one phase is interfered with other phases; leading to the complexity of the controller due to the requirement of the interference decoupling. Different from continuous current mode (CCM) control, the interference decoupling in the DCM operation is complicate due to the DCM nonlinearity [5-14] and requires many calculation efforts of the hardware [5-12]-[5-13]. Hence, the application of the conventional DCM control methods is limited.

Figure 5.1 depicts the H-bridge three-phase grid-tied inverter with a *LCL*-based grid filter. The minimization of the *LCL* filter generates a current with a high ripple in the inductors *L*. The filter stage with $L_f$ and $C_f$ can suppress the high-order current harmonics in order to meet grid current harmonic constraints as defined by standards such as IEEE-1547 [5-5]-[5-6].

Figure 5.2 describes the zero-crossing current distortion phenomenon. As the current ripple increases with the minimized *LCL* filter, the current distortion increases notably around the zero-crossing points due to the zero-current clamping effect, making the dead-time-induced error voltage

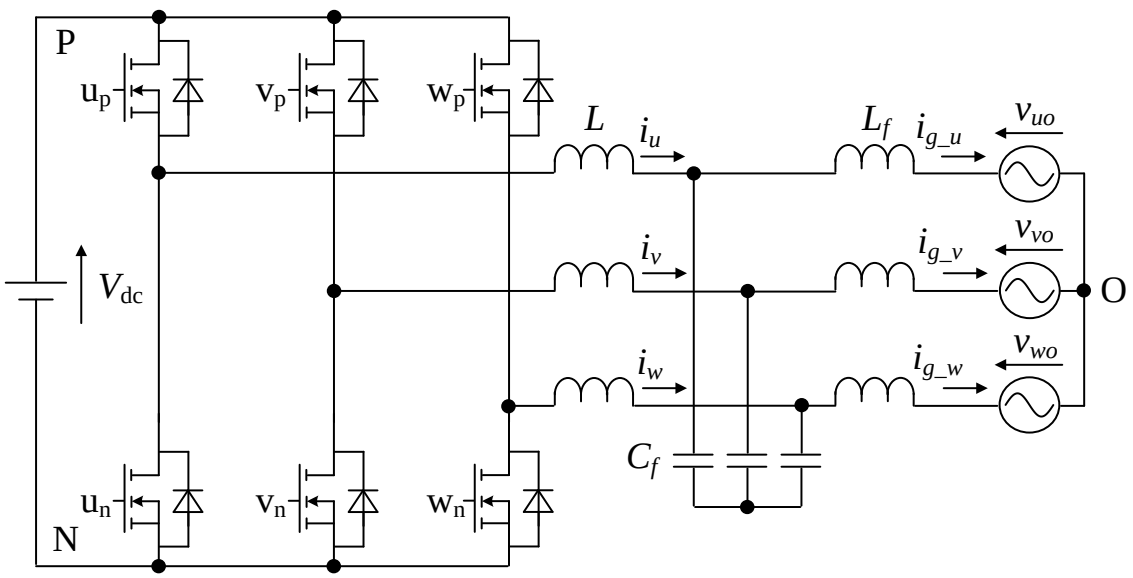
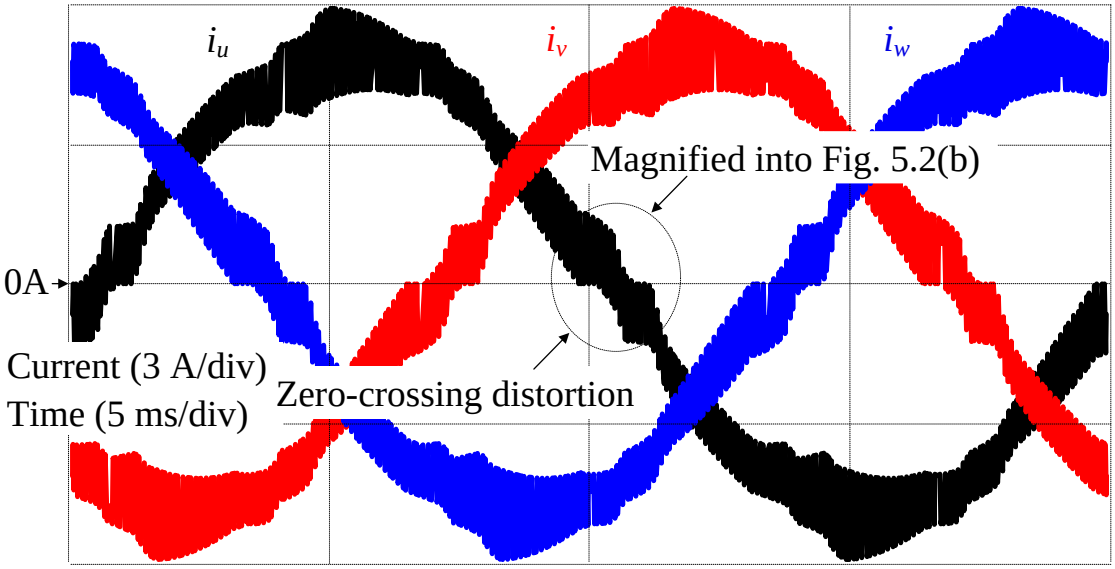
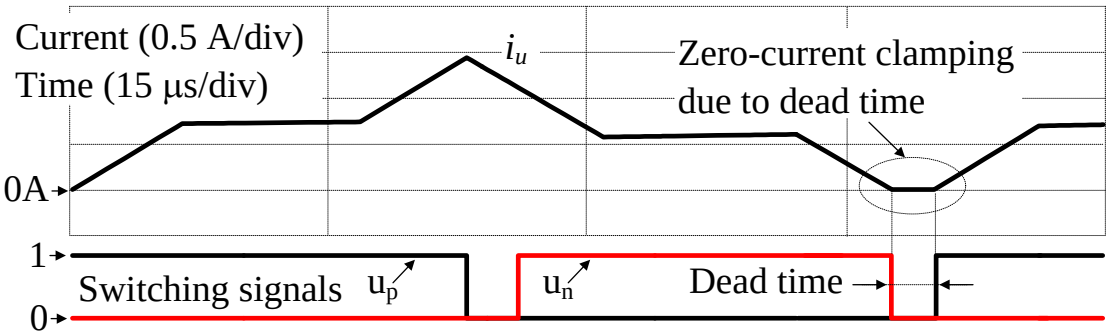



Fig. 5.1. H-bridge grid-tied three-phase inverter. This topology is employed due to its simple control and construction.

become nonlinear. Therefore, the employment of the conventional two-level ACM just further increases the current distortion.




(5.2.a) Zero-crossing distortions in inverter output currents

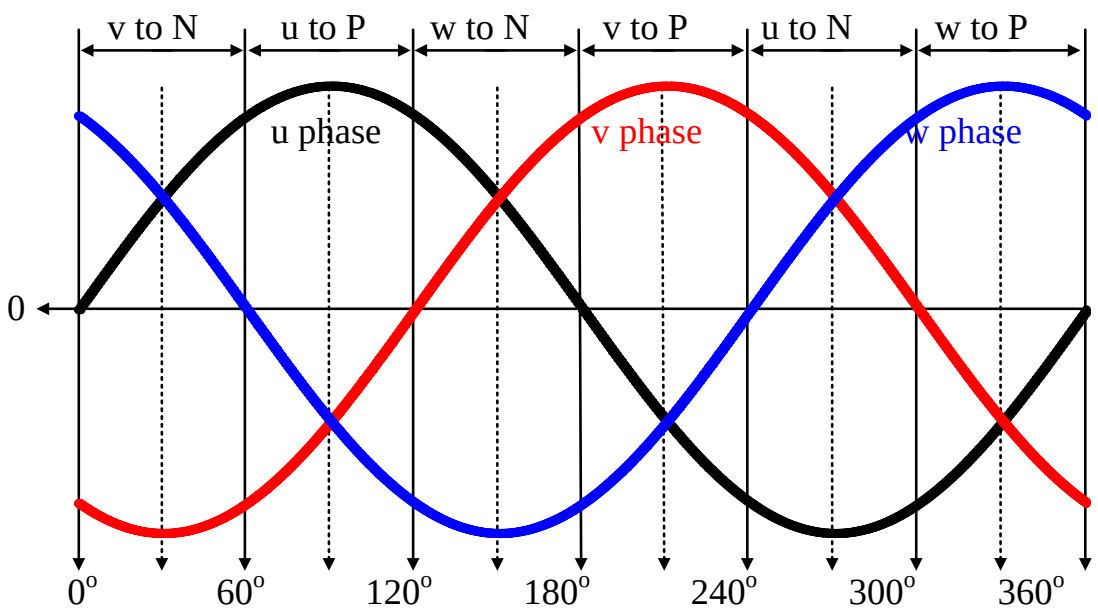



(5.2.b) Zero-current clamping effect due to dead-time

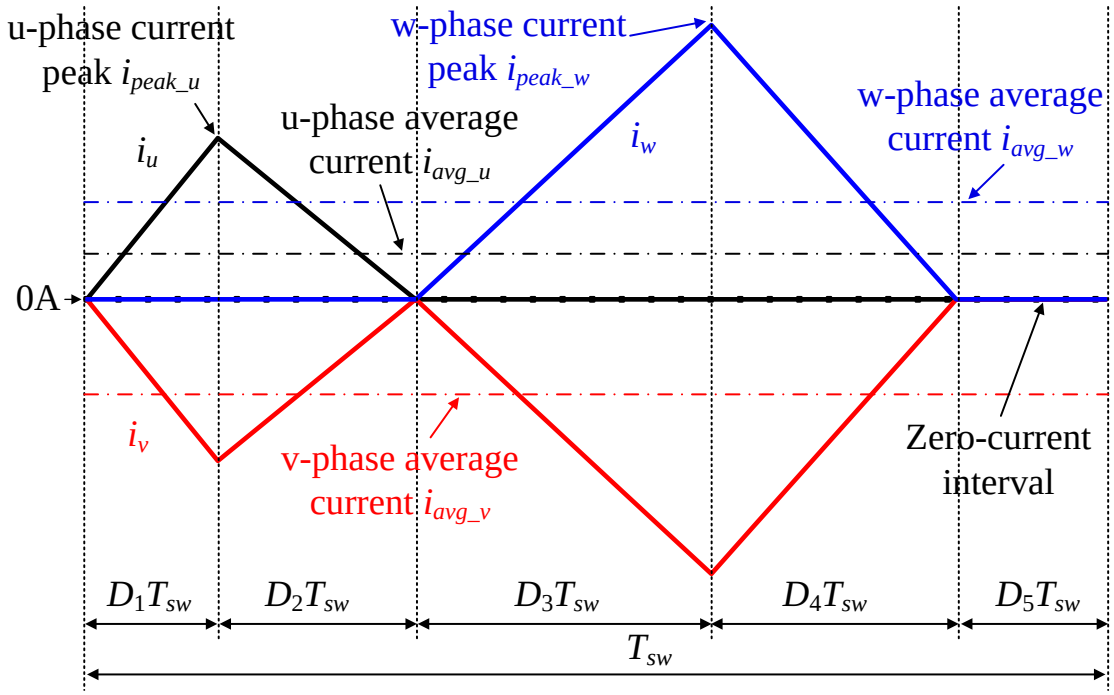
Fig. 5.2. Zero-current distortion phenomenon. The current distortion increases with the high current ripple due to the dead-time.

### 5.2.2 Circuit Model Derivation

Figure 5.3 indicates the phase clamping selection in six cycles of traditional discontinuous pulse width modulation (DPWM), and the inverter output current waveform in one switching period during $0^o$-$60^o$ region. In order to simplify the control of DCM, only two phase currents should be controlled, whereas the current of the third phase is the summation of the currents of the first two phases. Hence, DPWM is employed in order to satisfy this control condition. During each 60-degree time region in DPWM, one phase is clamped to P or N polarity of dc-link voltage as shown in Fig. 5.3(a), whereas the other two phases are modulated to control separately two inverter output currents as shown in Fig. 5.3(b). The separation of the controlled currents into each individual intervals result in the elimination of the interference decoupling, which is required many calculation efforts due to the nonlinearity in DCM [5-14]. Hence, the proposed DCM control method leads to a simple current control and can be applied into numerous application.




(5.3.a) Phase clamping selection in six cycles of DPWM




(5.3.b) Inverter output current waveform in one switching period during 0°-60° region

Fig. 5.3. Six 60-degree time regions of DPWM and inverter output current in DCM. In order to simplifying the DCM control, DPWM is employed, controlling only two phase currents at the same time.

The circuit model in DCM is derived in order to generate the duty ratios. Average small signal modeling technique is used to model the inverter for the current control loop design [4-14].

First, considering the u-phase current in Fig. 5.3(b), $D_1$ and $D_2$ indicate the duty ratios of the first and the second intervals of the u-phase current, whereas $D_3$ and $D_4$ indicate the duty ratios of the first and the second intervals of the w-phase current, and $D_5$ depicts the duty ratio of the zero-current intervals. The u-phase inductor voltage in $D_1T_{sw}$, $D_2T_{sw}$ and $(D_3+D_4+D_5)T_{sw}$ is given by (5.1)-(5.3), respectively,

$$v_{Lu_1} = V_{dc} - v_{uo} + v_{vo} \quad \text{.....} (5.1)$$

$$v_{Lu_2} = \left(-v_{uo} + v_{vo}\right) \quad \text{.....} (5.2)$$

$$v_{Lu_3} = 0 \quad \text{.....} (5.3)$$

where $V_{dc}$ is the dc-link voltage and $v_{uo}$ and $v_{vo}$ are the phase voltages. Then, the inductor voltage during a switching period is expressed by (5.4),

$$\begin{aligned} v_{Lu} &= D_1 v_{Lu_1} + D_2 v_{Lu_2} + D_0 v_{Lu_3} \\ &= D_1\left(V_{dc} - v_{vuo} + v_{vo}\right) + D_2\left(-v_{uo} + v_{vo}\right) \end{aligned} \quad \text{.....} (5.4)$$

where $D_0$ is the sum of $D_3$, $D_4$ and $D_5$. The average current $i_{avg_u}$ and the current peak $i_{peak_u}$ shown in Figure 5.3 is expressed as,

$$i_{avg_u} = \frac{i_{peak_u}}{2}\left(D_1 + D_2\right) \quad (5.5)$$

$$i_{peak_u} = \frac{V_{dc} - (v_{uo} - v_{vo})}{2L} D_1 T_{sw} \quad (5.6)$$

Substituting (5.6) into (5.5), and solving the equation for the duty ratios $D_2$, then the duty ratio $D_2$ is expressed by (5.7),

$$D_2 = \frac{4Li_{avg_u}}{D_1 T_{sw}(V_{dc} - v_{uo} + v_{vo})} - D_1 \quad (5.7)$$

Substituting (5.7) into (5.4) in order to remove the duty ratio $D_2$ and representing (5.4) as a function of only the duty ratio $D_1$, (5.8) is obtained.

$$L\frac{di_{avg_u}}{dt} = v_{Lu} = D_1 V_{dc} - v_{uv} + v_{uv}\left[1 - \frac{4Li_{avg_u}}{D_1 T_{sw}(V_{dc} - v_{uv})}\right] \quad (5.8)$$

Then, the circuit model in DCM is established based on (5.8) [5-14]-[5-15].

Fig. 5.4 illustrates the circuit model of the inverter operating in DCM. The dash line part does not exist when the inverter operates in CCM because the average current $i_{avg}$ equals to the half current peak $i_{peak}/2$; in other words, the CCM operation makes the zero-current interval $D_3T_{sw}$ shown in Fig. 5.3 disappear. Consequently, the zero-current interval $D_3T_{sw}$ induces the nonlinearity into the transfer functions when the inverter operates in DCM, which implies that the duty ratio in DCM is a function of

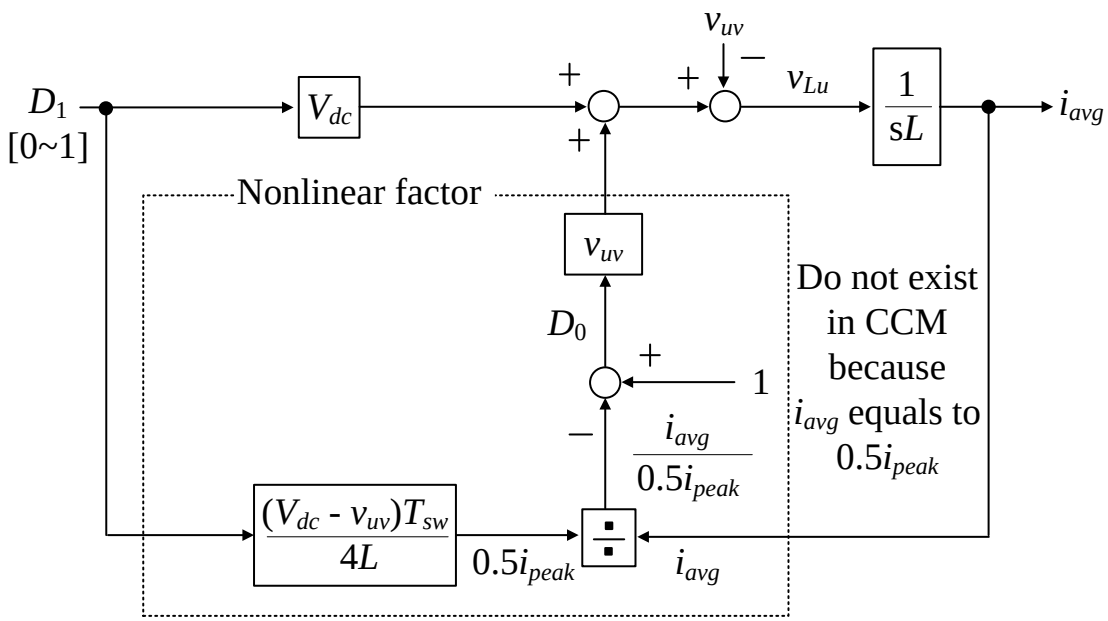



Fig. 5.4. Circuit model of inverter operating in DCM. The current control loop gain in DCM depends on the average current, i.e. the nonlinearities occurring in the duty-ratio-to-current transfer function.

the current at steady-state points. Substituting the u-phase inductor voltage $v_{Lu}$ in (5.8) as zero and the duty ratio $D_1$ is expressed as,

$$D_1 = 2\sqrt{\frac{i_{avg_u} L f_{sw}(v_{uo} - v_{vo})}{V_{dc}(V_{dc} - v_{uo} + v_{vo})}} \quad \text{.....(5.9)}$$

where $f_{sw}$ is the switching frequency. Then, substituting the u-phase inductor voltage $v_{Lu}$ in (5.4) as zero and the duty ratio $D_2$ is expressed as in (5.10),

$$D_2 = \frac{D_1(V_{dc} - v_{uo} + v_{vo})}{v_{uo} - v_{vo}} \quad \text{.....(5.10)}$$

Similarly, the duty ratios $D_3$ and $D_4$ of the w-phase current shown in Fig.

5.3(b) can be expressed as in (5.11)-(5.12),

$$D_3 = 2\sqrt{\frac{i_{avg_w} L f_{sw} (v_{wo} - v_{vo})}{V_{dc}(V_{dc} - v_{wo} + v_{vo})}} \quad \text{.....} (5.11)$$

$$D_4 = \frac{D_3 (V_{dc} - v_{wo} + v_{vo})}{v_{wo} - v_{vo}} \quad \text{.....} (5.12)$$

### 5.2.3 Discontinuous Current Mode Control System

Figure 5.5 shows the control system and the control operation flowchart of the three-phase grid-tied inverter operating completely in DCM, whereas Table 5.1 depicts the look-up table for the duty calculation and the switching signal output in each 60-degree time region. When the grid operates normally, the inverter only has to regulate the grid current following the sinusoidal waveform.

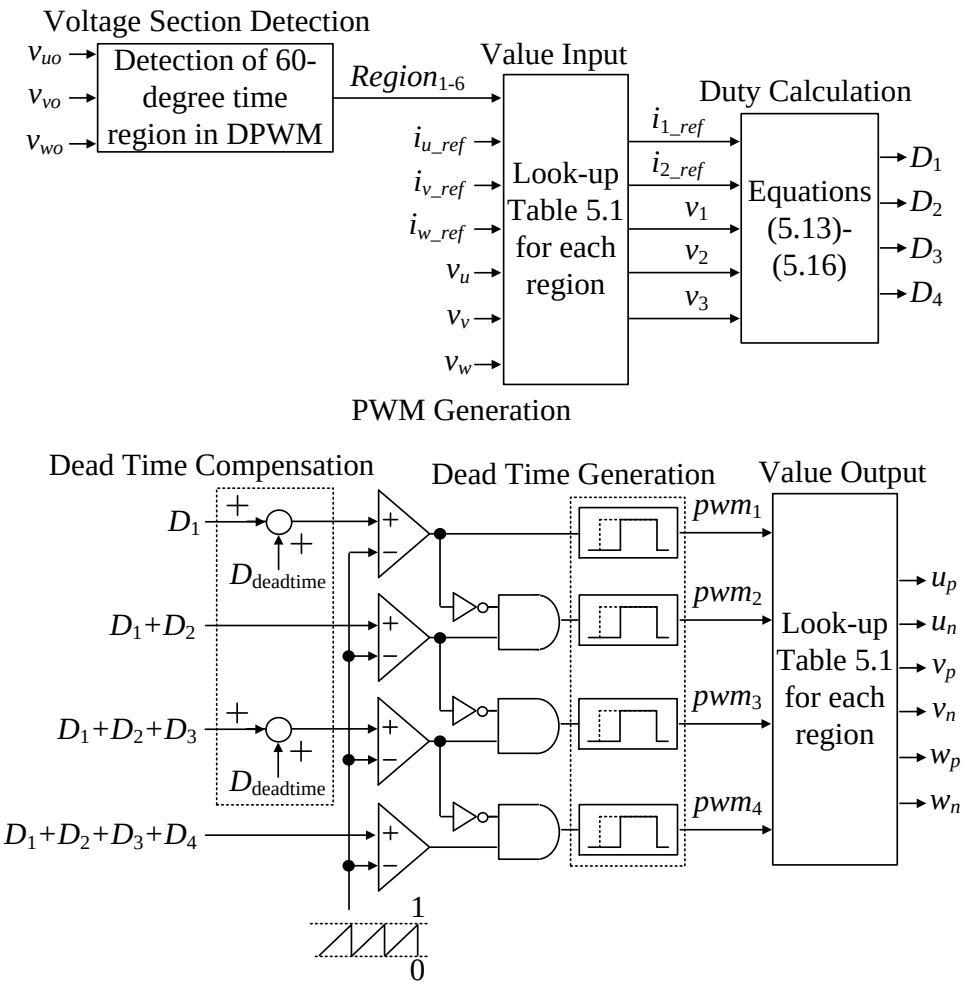
First, the new switching period is detected by using the carrier. In the start of new switching period, the 60-degree time section is detected by detected values of the grid phase voltage $v_{uo}$, $v_{vo}$, and $v_{wo}$. Then, the phase current references and the phase voltages are distributed to input values of a duty calculation based on the detected 60-degree time section as shown in Table 5.1. In the DCM operation, the duty ratio can be directly calculated from the current reference. Therefore, feed-forward control method is employed for the DCM operation in this paper. In the duty calculation step, the duty ratios $D_1$-$D_5$ are expressed as follows. Note that the calculation of the duty ratios $D_1$-$D_5$ is similar to that of the duty ratios $D_1$-$D_4$ shown in Figure 5.3.

$$D_1 = 2\sqrt{\left|\frac{i_{1_ref} L f_{sw}(v_1 - v_2)}{V_{dc}(V_{dc} - v_1 + v_2)}\right|} \quad \text{.....} (5.13)$$

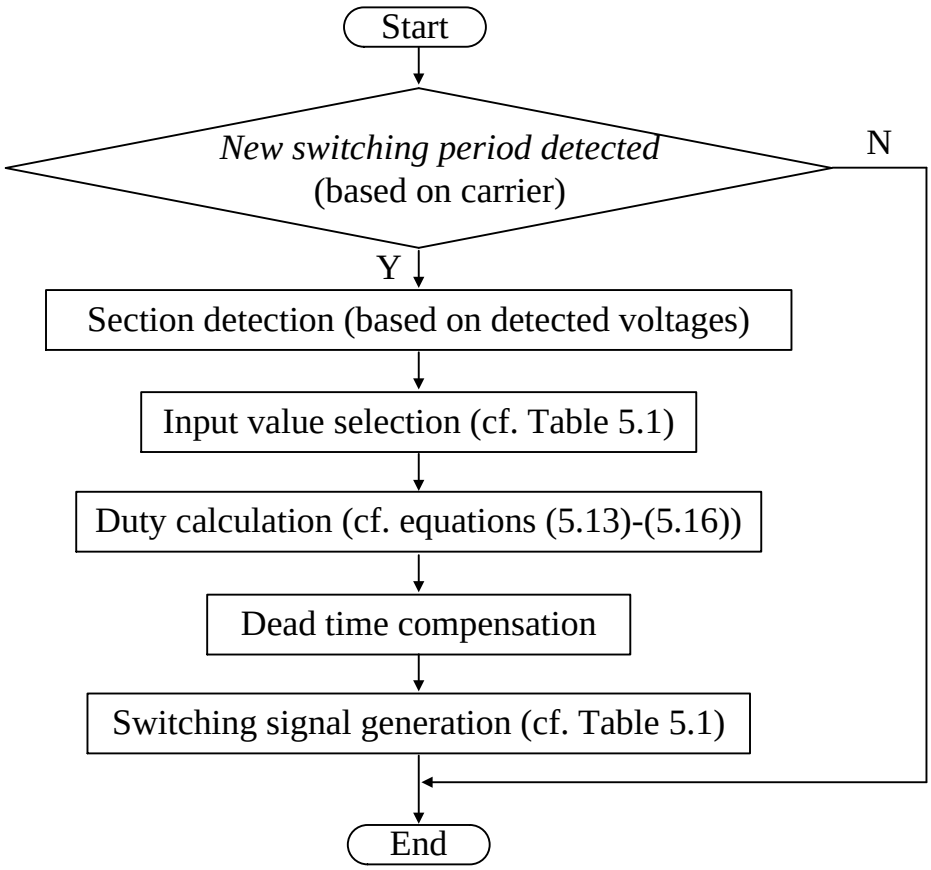
$$D_2 = \frac{D_1(V_{dc} - v_1 + v_2)}{v_1 - v_2} \quad \text{.....} (5.14)$$

$$D_3 = 2\sqrt{\left|\frac{i_{2_ref} L f_{sw}(v_3 - v_2)}{V_{dc}(V_{dc} - v_3 + v_2)}\right|} \quad \text{.....} (5.15)$$

$$D_4 = \frac{D_4(V_{dc} - v_3 + v_2)}{v_3 - v_2} \quad \text{.....} (5.16)$$




(5.5.a) Control system




(5.5.b) Control operation flowchart

Fig. 5.5. Control system of the three-phase grid-tied inverter operating completely in DCM. The dead-time-induced error voltage is compensated simply when the inverter is intentionally operated in DCM because the zero-current interval is controlled.

$$D_5 = 1 - D_1 - D_2 - D_3 - D_4 \quad (5.17)$$

where $i_{1_ref}$ and $i_{2_ref}$ are the first and second controlled currents in each 60-degree time region, and $v_1$, $v_2$ and $v_3$ are the voltages corresponding to the controlled currents. For instance, during the $0^o$-$60^o$ time region, the controlled currents are $i_u$ and $i_w$ as shown in Fig. 5.3. Therefore, the input values to $i_1$, $i_2$, $v_1$, $v_2$, and $v_3$ are $i_{u_ref}$, $i_{w_ref}$, $v_{uo}$, $v_{vo}$ and $v_{wo}$, respectively, as

TABLE 5.1.
LOOK-UP TABLE FOR DUTY CALCULATION AND PWM OUTPUT.

| Region / Variable | $0^o$-$60^o$ | $60^o$-$120^o$ | $120^o$-$180^o$ | $180^o$-$240^o$ | $240^o$-$300^o$ | $300^o$-$360^o$ |
|---|---|---|---|---|---|---|
| $i_{1_ref}$ | $i_{u_ref}$ | $i_{w_ref}$ | $i_{v_ref}$ | $i_{u_ref}$ | $i_{w_ref}$ | $i_{v_ref}$ |
| $i_{2_ref}$ | $i_{w_ref}$ | $i_{v_ref}$ | $i_{u_ref}$ | $i_{w_ref}$ | $i_{v_ref}$ | $i_{u_ref}$ |
| $v_1$ | $v_u$ | $-v_w$ | $v_v$ | $-v_u$ | $v_w$ | $-v_v$ |
| $v_2$ | $v_v$ | $-v_u$ | $v_w$ | $-v_v$ | $v_u$ | $-v_w$ |
| $v_3$ | $v_w$ | $-v_v$ | $v_u$ | $-v_w$ | $v_v$ | $-v_u$ |
| $u_p$ | $pwm_1$ | 1 | $pwm_3$ | $pwm_2$ | 0 | $pwm_4$ |
| $u_n$ | $pwm_2$ | 0 | $pwm_4$ | $pwm_1$ | 1 | $pwm_3$ |
| $v_p$ | 0 | $pwm_4$ | $pwm_1$ | 1 | $pwm_3$ | $pwm_2$ |
| $v_n$ | 1 | $pwm_3$ | $pwm_2$ | 0 | $pwm_4$ | $pwm_1$ |
| $w_p$ | $pwm_3$ | $pwm_2$ | 0 | $pwm_4$ | $pwm_1$ | 1 |
| $w_n$ | $pwm_4$ | $pwm_1$ | 1 | $pwm_3$ | $pwm_2$ | 0 |

shown in Table 5.1.

Next, the dead-time compensation is introduced at the first step of PWM generation. The duty ratio which compensates for the dead-time-induced error voltage, is expressed as follow,

$$D_{deadtime} = f_{sw} T_{deadtime} \quad (5.18)$$

where $T_{deadtime}$ is the dead-time. The dead-time-induced error voltage is simply compensated as shown in Fig. 5.4 because when the inverter is intentionally operated in DCM, the zero-current interval is under control. The compensated duty ratios are then compared with the sawtooth waveform to generate the PWM signals. In order to avoid the simultaneous

turn-on of both switching devices in one leg, the typical dead-time generation is used to delay the turn on. Finally, the PWM signals are distributed to the switching devices corresponding to each 60-degree time region of DPWM based on Table 5.1. Note that if the outputs $pwm_2$ and $pwm_4$ are utilized as shown in Table 5.1, the inverter is operated under synchronous switching; otherwise, if the outputs $pwm_2$ and $pwm_4$ are set to zero, the inverter is operated under asynchronous switching.

## 5.3 Simulation Results

Table 5.2 shows the circuit parameters to evaluate the operation of the inverters, whereas Figure 5.6 depicts the inductor volume against the inductor impedance. The inverter-side inductors $L$ in Fig. 5.1 occupy a majority of the inverter volume. Therefore, the minimization of $L$ is mainly focused in this paper. Generally, the inductor value is expressed as a grid filter impedance scaled to the inverter total impedance $\%Z_L$ [5-16]. In particular, three designs of the grid filter impedance are evaluated. As shown in Fig. 5.6, the inverter-side inductor $L$ volume is minimized by 70% when the inductor impedance $\%Z_L$ is reduced from 2.5% to 0.075%.

Figure 5.7 shows the inverter output currents and the average currents of the conventional CCM current control and the proposed DCM current control at rated load with three inductor designs from Fig. 5.6. As the current ripple increases, i.e. the decrease in the inductor impedance, the current with the conventional CCM current control distorts notably around the zero-crossing points. Consequently, the current THD increases from 1.5% to 9.8% when the inductor impedance $\%Z_L$ is reduced from 2.5% to 0.075%. On the other hand, when the inverter is operated in DCM, the

TABLE 5.2.
SIMULATION PARAMETERS.

| Circuit Parameter | | |
|---|---|---|
| $V_{DC}$ | DC link Voltage | 500 V |
| $v_g$ | Line-to-line Voltage | 200 Vrms |
| $P_n$ | Nominal Power | 3 kW |
| $f_g$ | Grid Frequency | 50 Hz |
| $Z_b$ | Total Impedance | 13.3 Ω |
| $f_{sw}$ | Switching Frequency | 40 kHz |
| $T_{deadtime}$ | Dead-time | 500 ns |
| $L_1$ | 1st Inductor Value | 1061 μH (2.5%) |
| $L_2$ | 2nd Inductor Value | 254.6 μH (0.6%) |
| $L_3$ | 3rd Inductor Value | 31.8 μH (0.075%) |
| **Current Controller Parameter** | | |
| $\zeta$ | Damping Factor | 0.7 |
| $f_c$ | Cutoff Frequency | 1 kHz |

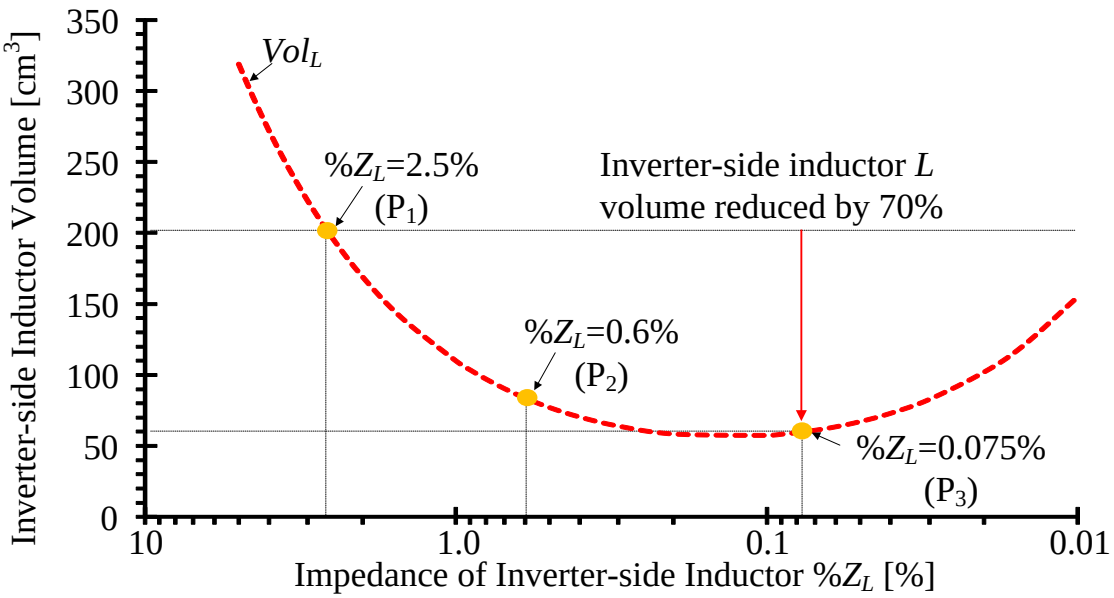
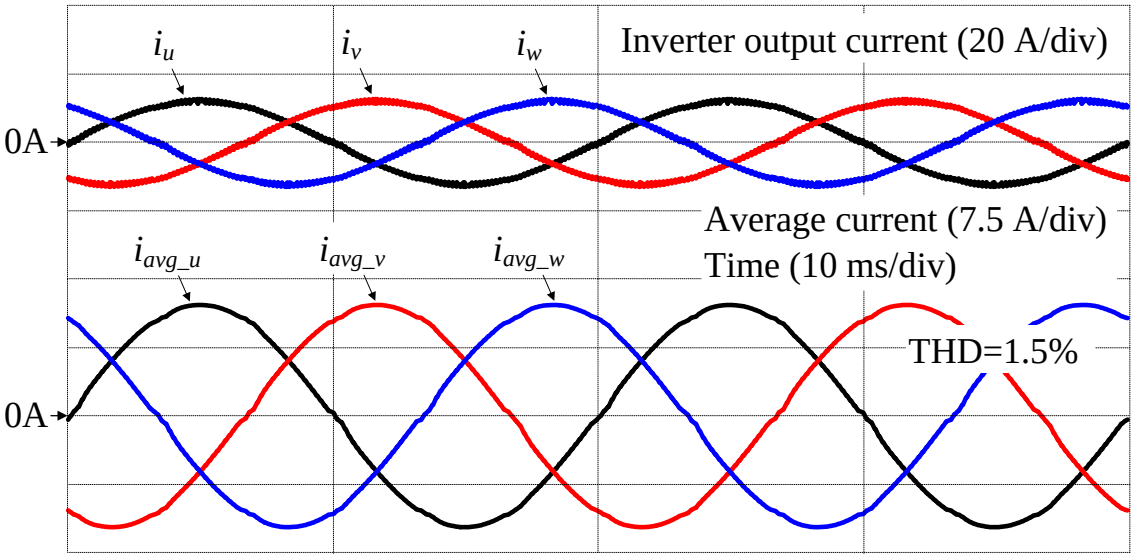
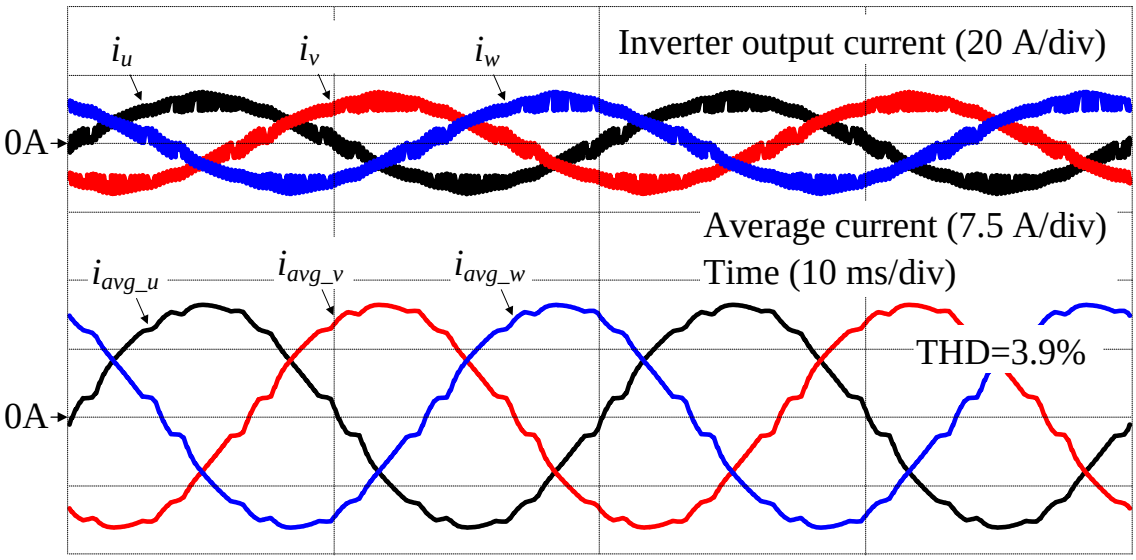



Fig. 5.6. Relationship between filter volume and inductor impedance at switching frequency of 40 kHz. The inductor volume can be minimized greatly when reducing the inductor impedance.

zero-current interval can be controlled and the dead-time-induced error



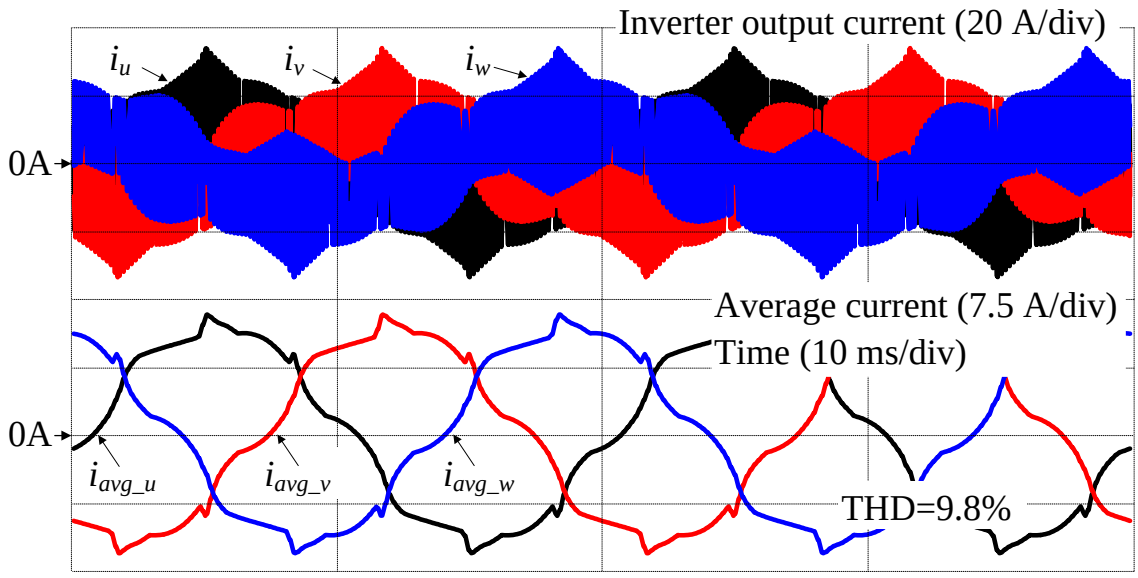

(5.7.a) Conventional CCM control with %$Z_L$ = 2.5% at rated load



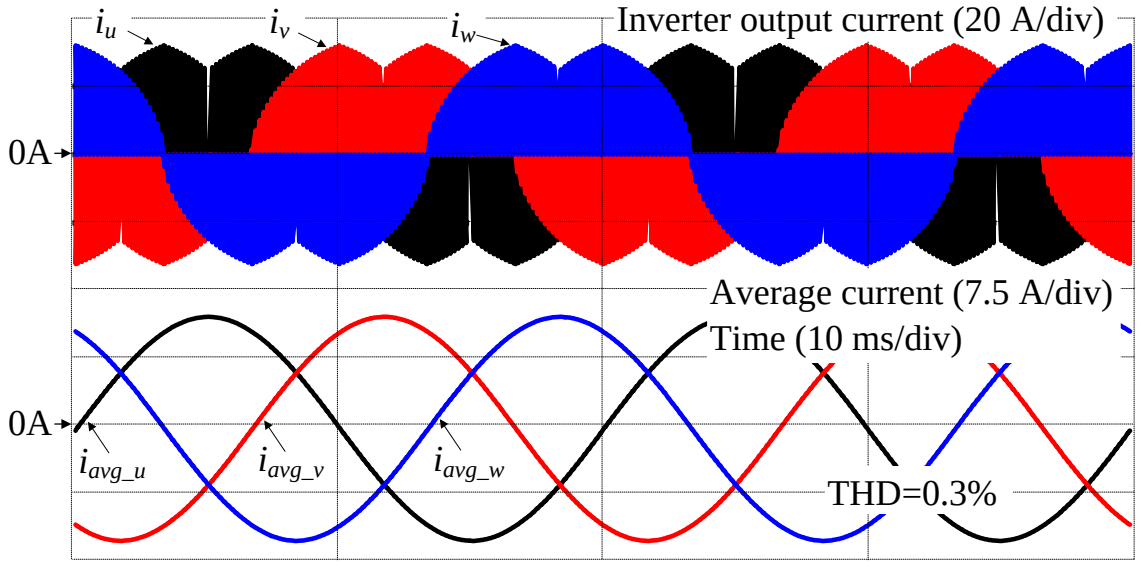

(5.7.b) Conventional CCM control with %$Z_L$ = 0.6% at rated load

voltage can be compensated simply as shown in Fig. 5.5. Therefore, even with the minimized inductor impedance of 0.075%, the low current THD of 0.3% is achieved with the proposed DCM current control.

Figure 5.8 depicts the load step response of the proposed DCM current




(5.7.c) Conventional CCM control with %$Z_L$ = 0.075% at rated load




(5.7.d) Proposed DCM control with %$Z_L$ = 0.075% at rated load

Fig. 5.7. Inverter output currents and average currents of conventional CCM current control and proposed DCM current control at rated load. The current THD of the conventional CCM current control increases with the reduction of the grid filter impedance, whereas the current THD of the proposed current control is still low.

control. Even under the sudden load step between the load of 0.1 p.u. and

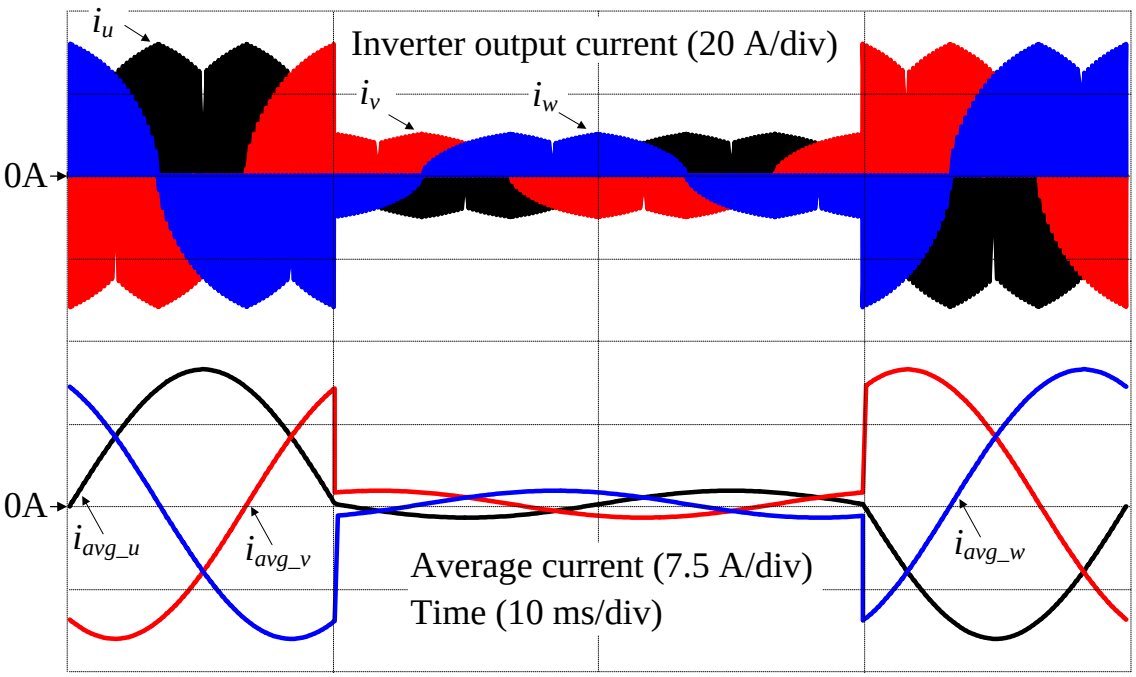



Fig. 5.8. Load step response between load of 0.1 p.u. and load of 1.0 p.u.. The stable inverter operation is confirmed even at load step change. Moreover, the balanced phase currents are also confirmed.

the load of 1.0 p.u., the stable inverter operation and the balanced three-phase currents are still achieved with the proposed control.

Figure 5.9 shows the current THD characteristics of the conventional CCM current control and the proposed DCM current control with three inductor designs from Fig. 5.6. At rated load with the inductor impedance of 0.075%, the current distortion of the proposed DCM current control is reduced by 97.6% compared to the conventional CCM current control. Note that the current THD of the conventional CCM current control with the inductor impedance of 0.075% or 0.6% has a tendency to decrease at

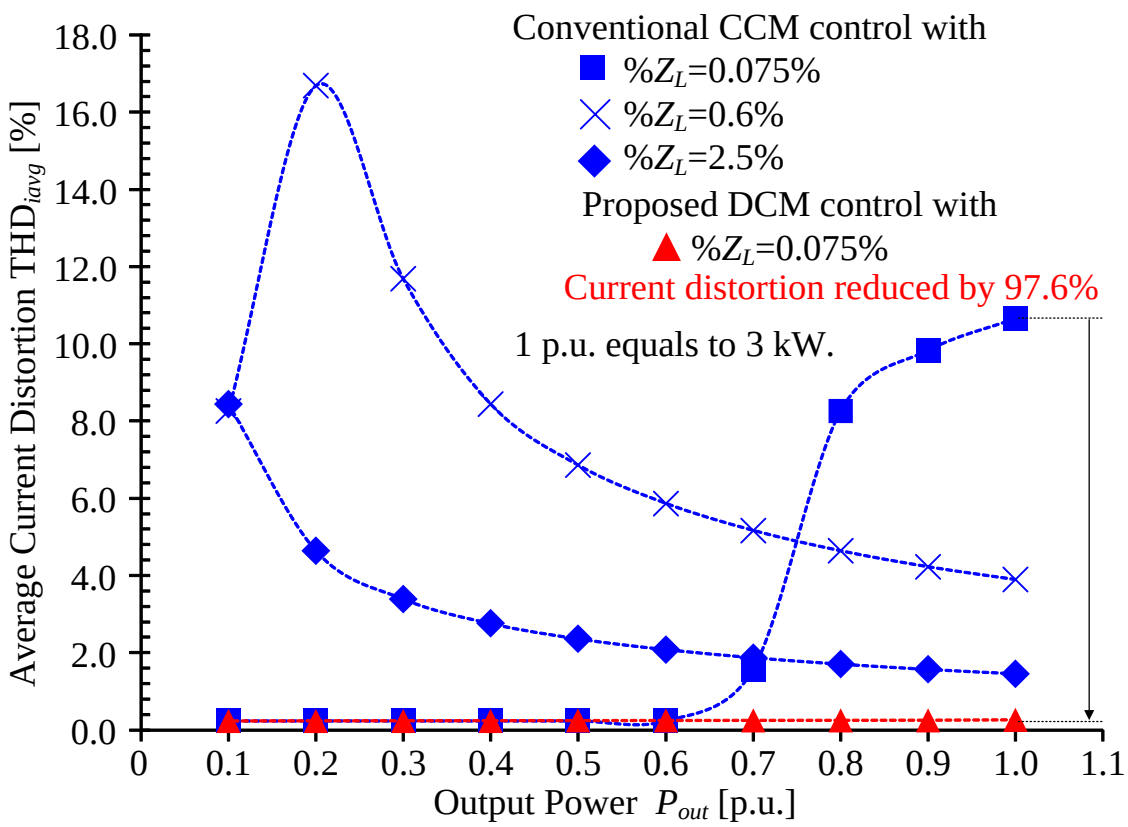



Fig. 5.9. Current THD characteristics of conventional CCM current control and proposed DCM current control with three different inductor designs. With the proposed DCM current control, the current THD is maintained below 5% over entire load range from 0.1 p.u. to 1.0 p.u..

light load. The reason is when the average current is significantly smaller than the current ripple, the current mode is no longer CCM but triangular current mode (TCM) [17]. In TCM, all the turn on of the switching devices is zero voltage switching. On other words, the dead-time-induced error voltage does not occur in TCM. Hence, the current distortion due to the zero-clamping phenomenon disappears at light load.

## 5.4 Experimental Results

Table 5.3 shows the experimental parameters, whereas figure 5.10 depicts the prototype of the miniature three-phase grid-tied inverter. In order to operate the inverter under DCM over entire load range with the switching frequency of 20 kHz, the inverter-side inductor value is designed at 80 μH, whose impedance is 0.5% of the total inverter impedance.

TABLE 5.3.
EXPERIMENTAL PARAMETERS.

| **Circuit Parameter** | | |
|---|---|---|
| $V_{DC}$ | DC link Voltage | 300 V |
| $v_g$ | Line-to-line Voltage | 100 Vrms |
| $P_n$ | Nominal Power | 700 W |
| $f_g$ | Grid Frequency | 50 Hz |
| $Z_b$ | Total Impedance | 4.8 Ω |
| $f_{sw}$ | Switching Frequency | 20 kHz |
| $T_{deadtime}$ | Dead-time | 500 ns |
| $L$ | Inductor Value | 80 μH (0.5%) |

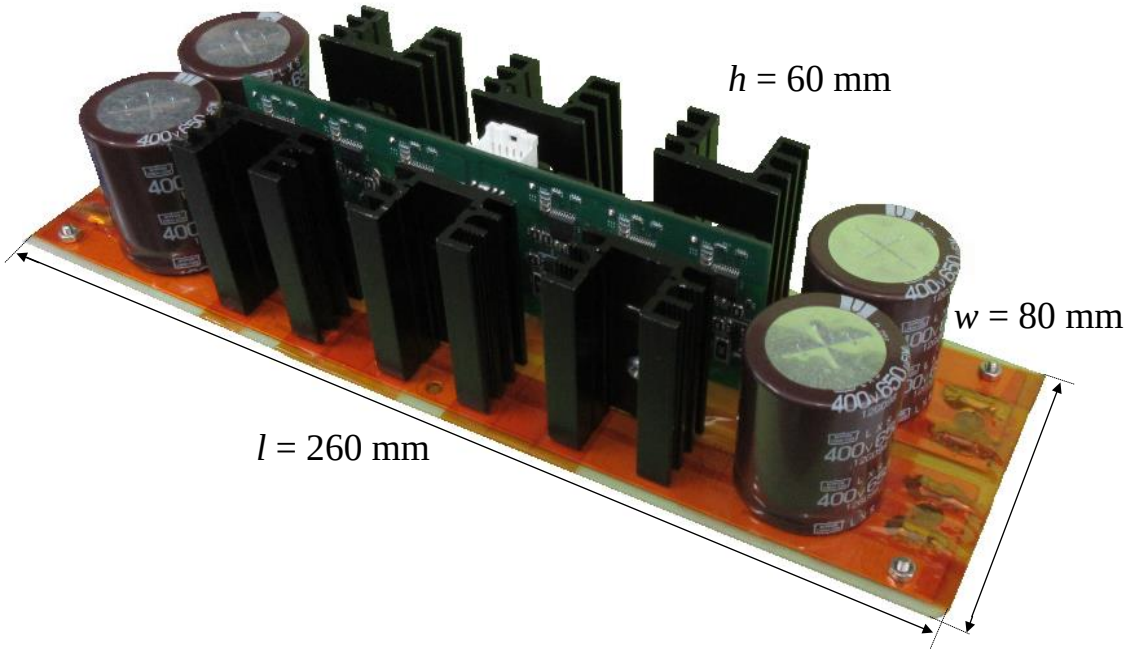
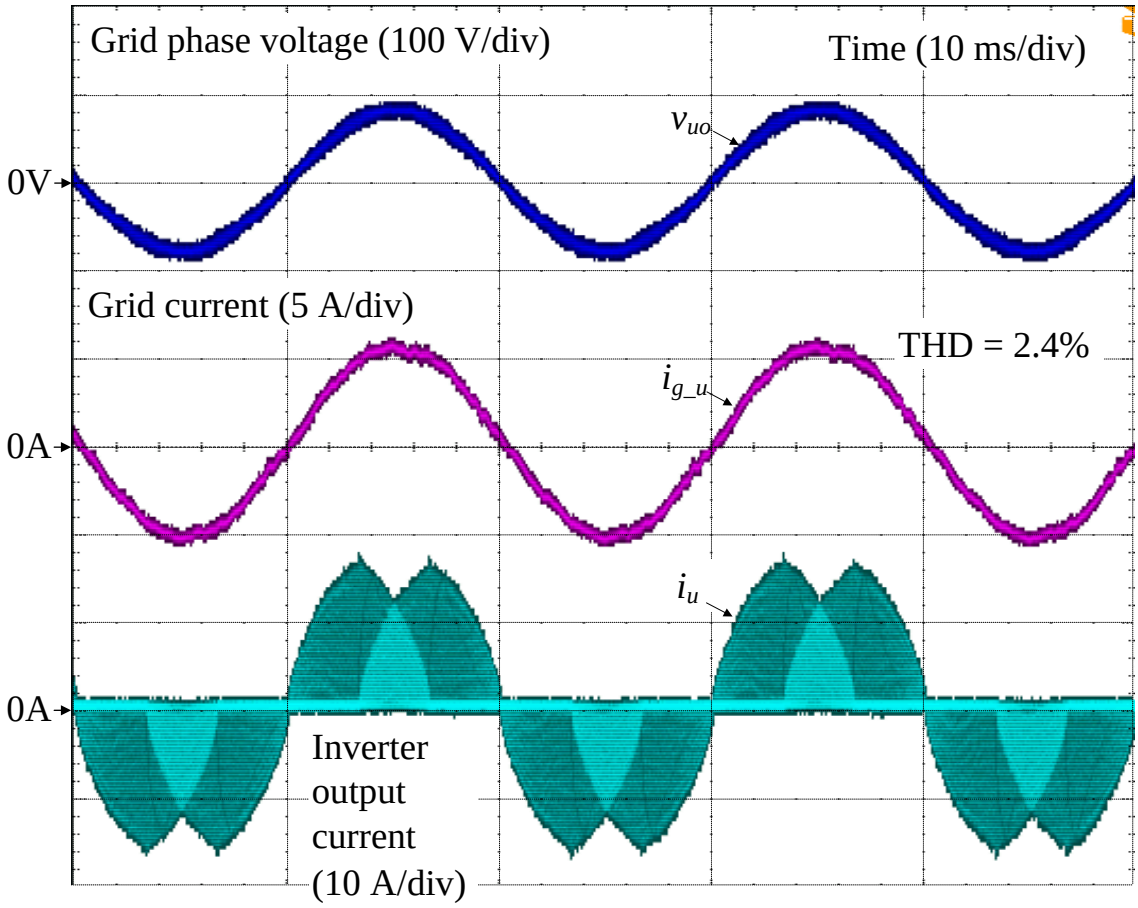



Fig. 5.10. Prototype of miniature three-phase grid-tied inverter.

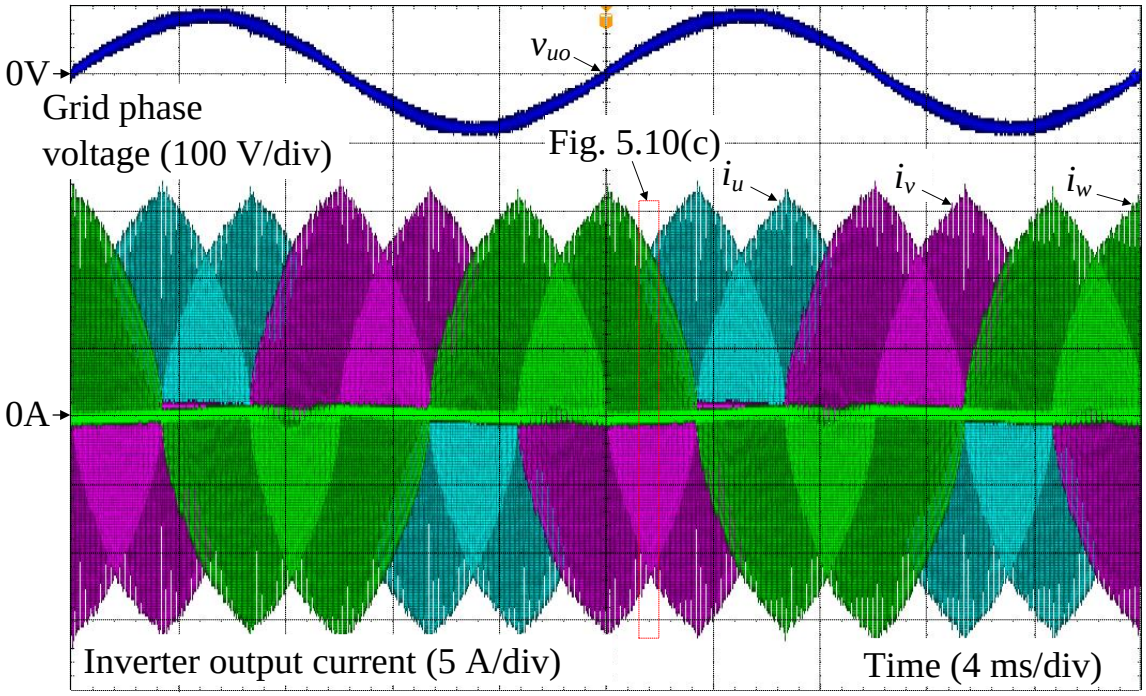
### 5.4.1 Operation Verification

Figure 5.11 depicts the three-phase grid-tied inverter DCM operation waveform at rated load. In Figure 5.11(a), the phase difference between the grid current of u phase and the grid u-phase voltage is almost zero, i.e. the unity-power-factor operation. Furthermore, even with the small inverter-side inductor impedance of 0.5%, the low current THD of 2.4% is still achieved. As shown in Figure 5.11(b)-(c), the three-phase inverter output currents are similar to those shown in Figure 5.7(c), i.e. the operation of the proposed DCM control is confirmed.

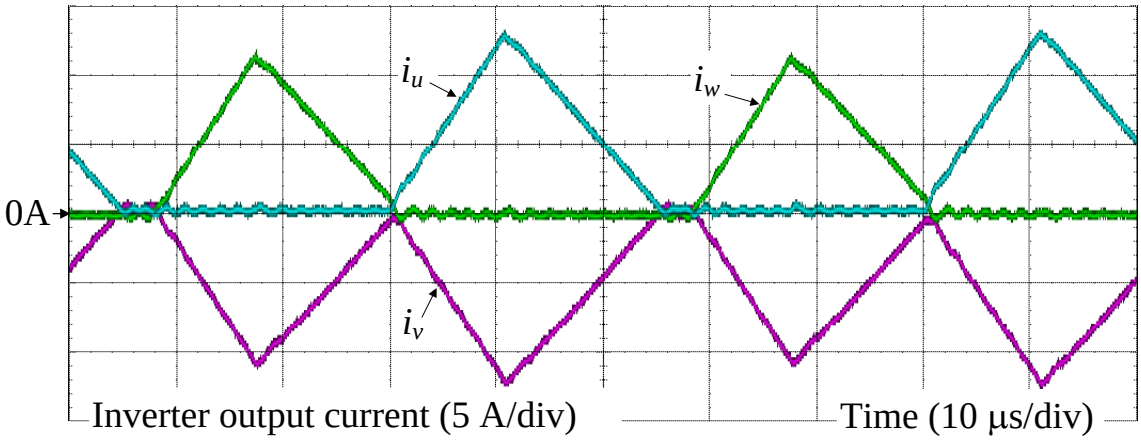
Figure 5.12 shows the grid phase voltages and the grid currents of u phase and w phase at the normal operation and at step-up load change. At the normal operation, the three-phase grid current is well balance and the low current THD of 2.4% is achieved for all three-phase grid current. At the step-up load change from 0.1 p.u. to 1.0 p.u., the stable current response is confirmed. Note that the three-phase grid currents are still balance both




(5.11.a) Grid phase voltage, grid current, and inverter output current of u phase




(5.11.b) Grid phase voltage of u phase, and three-phase inverter output currents

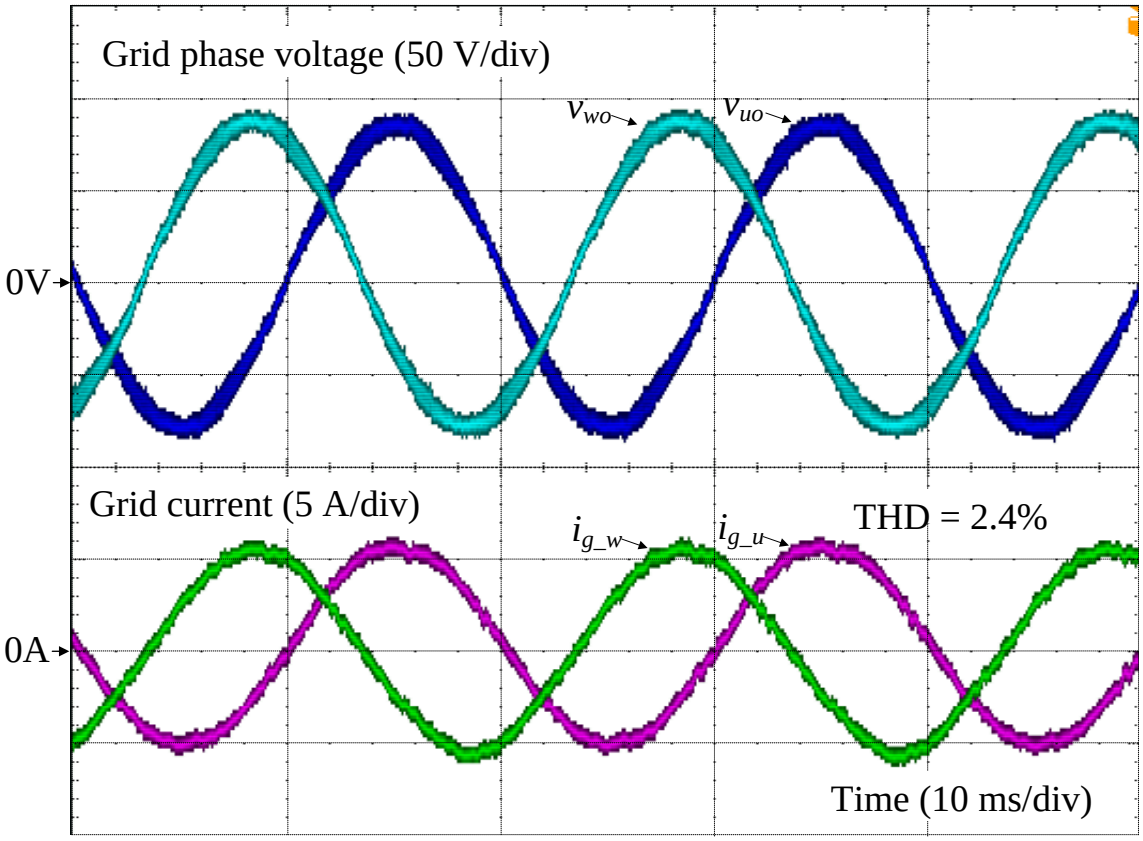



(5.11.c) Zoom-in three-phase grid current from Fig. 5.10(b)

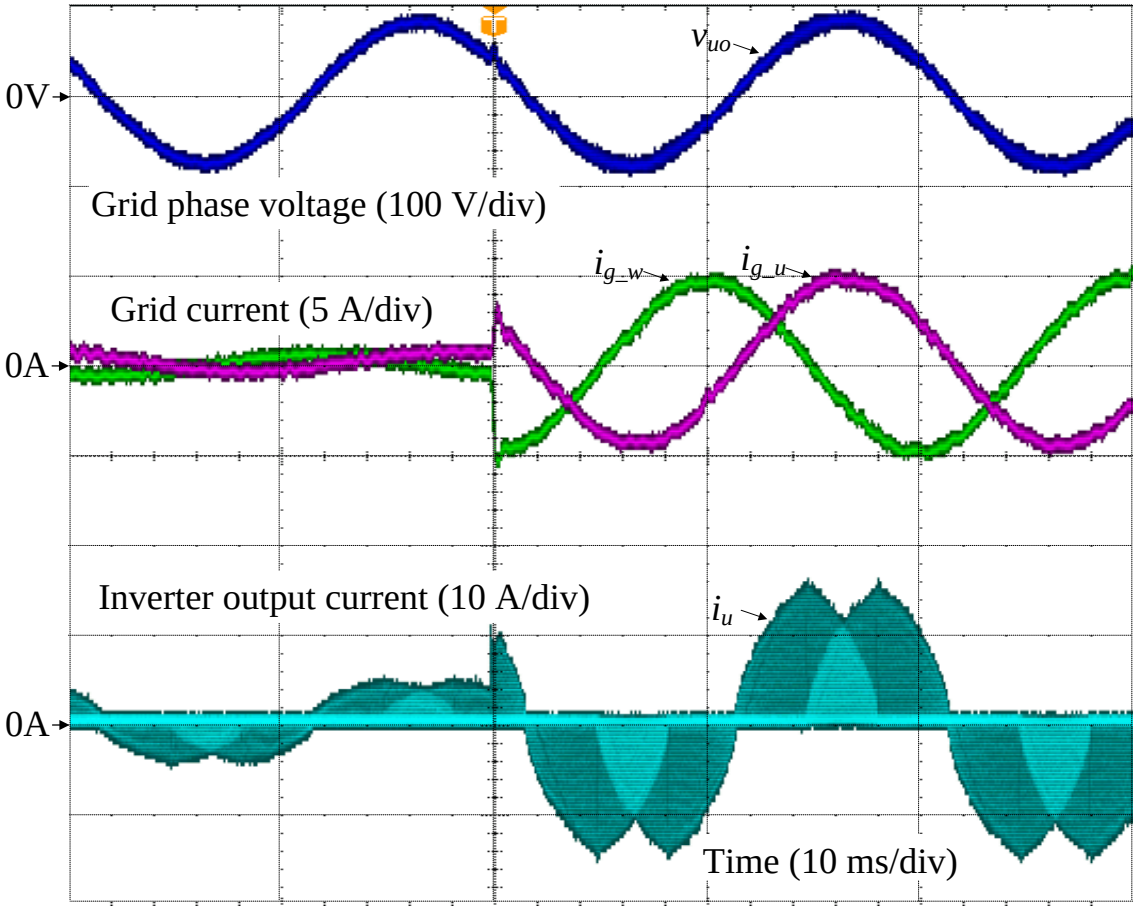
Fig. 5.11. Three-phase grid-tied inverter DCM operation waveform at rated load. The three-phase inverter output currents shown in Fig. 5.10(b) are similar to those shown in Fig. 5.6(c). This confirms the operation of the proposed DCM control.

before and after the step-up load change.

Figure 5.13 depicts the current THD characteristics of the proposed DCM current control. The current THD is maintained below 5% over load range from 0.3 p.u. to 1.0 p.u., which satisfies the current THD constraint in IEEE-1547, even when the inductance impedance is reduced to 0.5% of the inverter impedance. The increase of the current THD at light load can be explained due to the high occupation of the reactive current flowing through the filter capacitor. Therefore, in order to reduce the current THD




(5.12.a) Grid phase voltages and grid currents of u phase and w phase at normal operation




(5.12.b) Current response of step-up load change

Fig. 5.12. Grid phase voltages and grid currents of u phase and w phase at normal operation and at step-up load change.

at light load, the DCM control should also consider the effect of the reactive current in the filter capacitor.

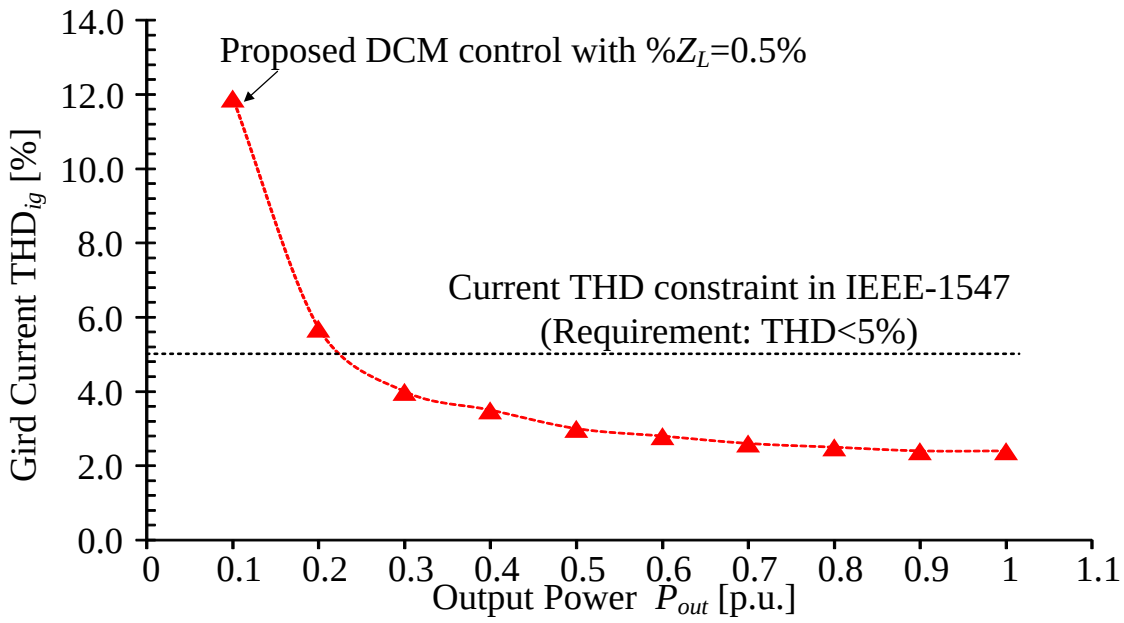
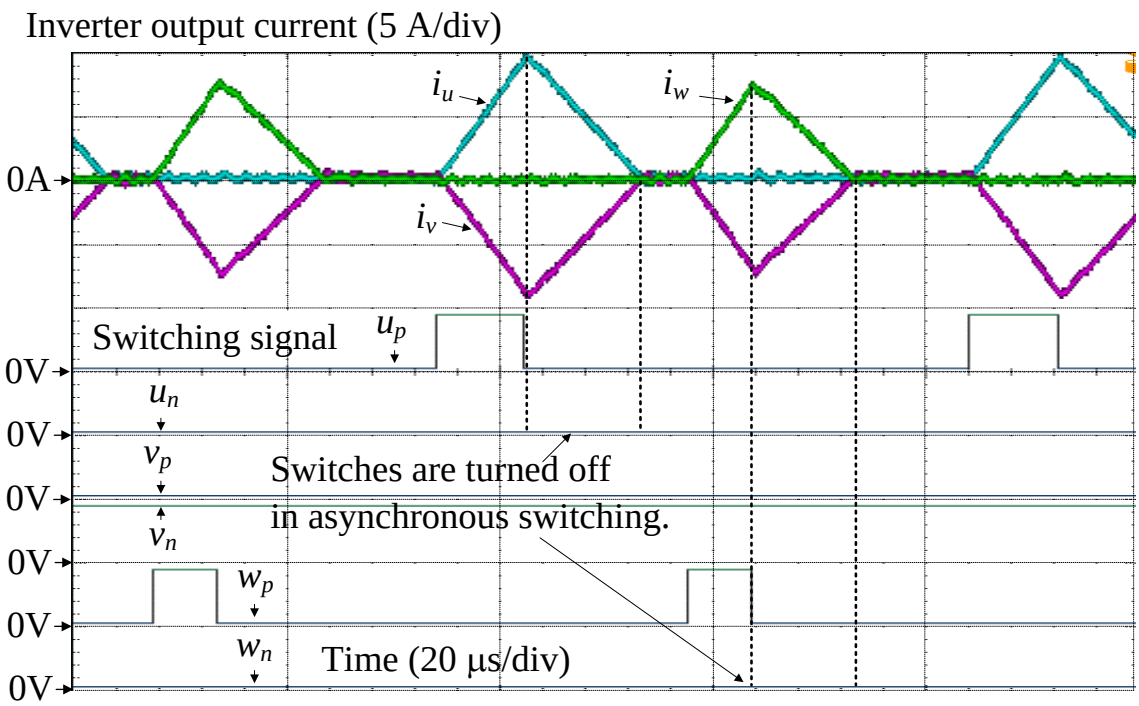



Fig. 5.13. Current THD characteristics of proposed DCM current control. The current THD is maintained below 5% over load range from 0.3 p.u. to 1.0 p.u., which satisfies the current THD constraint in IEEE-1547, even when the inductance impedance is reduced to 0.5% of the inverter impedance.

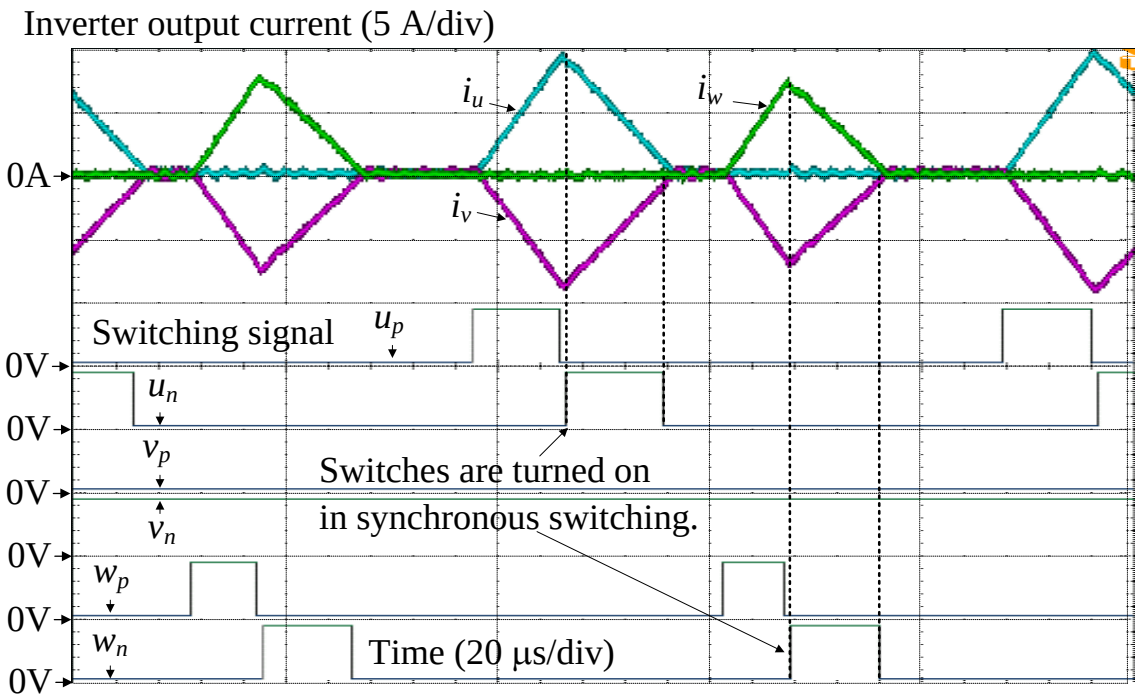
### 5.4.2 Efficiency Comparison between Asynchronous and Synchronous Switching

Figure 5.14 shows the asynchronous switching and synchronous switching in DCM. In the asynchronous switching, the corresponding switches are turned after the period $D_1T_{sw}$ and $D_3T_{sw}$ finish. Therefore, the current has to flow through the diode. In the next generation switching devices such as SiC or GaN, the forward voltage of the inverse diode in such devices is generally higher than that of the conventional MOS-FET devices. Consequently, the conduction loss with the asynchronous switching is higher that of the synchronous switching, where the current flows through the FET part. As shown in Figure 5.14, the synchronous switching can also be applied into DCM in the same manner as the conventional CCM. Consequently, the conduction loss of the switching device is reduced.

Figure 5.15 depicts the efficiency comparison between asynchronous switching and synchronous switching in DCM. The application of the DCM synchronous switching reduces the conversion loss by 33% compared to the DCM asynchronous switching at rated load. Furthermore,




(5.14.a) Asynchronous switching in DCM




(5.14.b) Synchronous switching in DCM

Fig. 5.14. Asynchronous switching and synchronous switching in DCM.

the maximum efficiency of 97.8% is achieved at rated load.

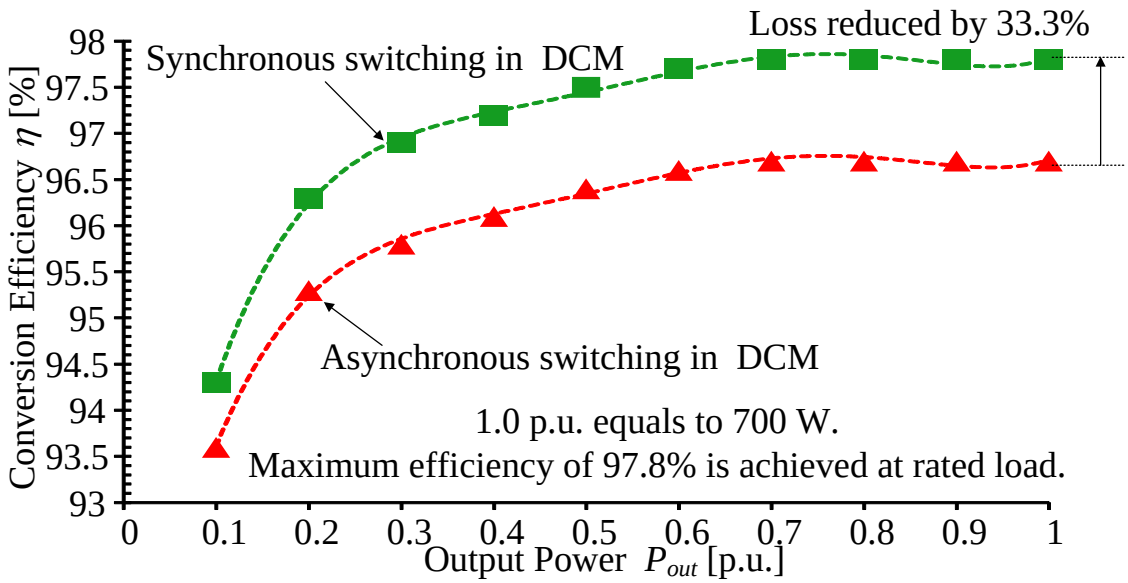



Fig. 5.15. Efficiency comparison between asynchronous switching and synchronous switching in DCM.

## 5.5 Conclusion

In this chapter, the DCM current control was proposed to the grid-tied three-phase inverter in order to minimize the grid filter volume without worsening the current THD. The DCM control separated the control of each current in individual intervals in order to avoid the control interference of current into each other. Therefore, the interference decoupling control for DCM operation was not required for the proposed control, leading to the simple control system. The effectiveness of the proposed DCM control method was confirmed by both simulations and experiments. In particular, the low current THD of 2.4% was achieved even when the inductance impedance was reduced to 0.5% of the inverter total impedance.

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# Chapter 6

# Hybrid Discontinuous Current Mode

## 6.1 Introduction

This chapter presents a novel concept of a hybrid current mode between triangular current mode (TCM) and discontinuous current mode (DCM), which is entitled hybrid discontinuous current mode (HDCM). The proposed current mode can achieve a high efficiency over a wide load range for a high-frequency SiC-based boost converter. In HDCM, TCM is applied during zero-current interval of DCM in order to satisfy the conditions for ZVS. Consequently, the switching frequency can be increased by HDCM in order to minimize the converter. Meanwhile, the current ripple is also reduced at light load, which results in the

wide-load-range high efficiency. The chapter is organized as follows; in section 6.2, HDCM is proposed in order to solve the problems of the conventional current modes, then in section 6.3 the design and the control of the boost converter operated in HDCM are explained. After that, experimental HDCM operations are presented in section 6.4. In particular, a comparison of the efficiencies among four current modes, i.e. TCM, DCM, continuous current mode (CCM) and HDCM, over a wide load range is carried out. Furthermore, the advantages of HDCM over other current modes are clarified based on these results. Finally, in section 6.5, the conclusion of this chapter will be presented.

## 6.2 Hybrid Current Mode between Discontinuous Current Mode and Triangular Current Mode

Over the past decades, the increase of the power density has been one of the most important design criteria in power electronics due to limited space requirements or weight reductions [6-1]-[6-3]. A typical boost DC-DC converter is widely applied in many power conversion systems, e.g. power conditioning system in photovoltaic systems. Magnetic component, i.e. a boost inductor in the boost converter, accounts for the major volume of the converter [6-4]. By increasing the switching frequency, the volume of the boost inductor can be reduced. However, higher switching frequency leads to an increase of switching loss, which requires larger cooling system. Therefore, a reduction of the switching loss is crucial to high power density design.

In recent years, SiC devices have emerged as promising devices for high efficiency and high density power conversion. The switching frequency of SiC devices has been push up to several hundreds of kHz in order to reduce the size of the magnetic component. The following important switching characteristic occurs in the SiC devices; turn-on

switching loss is dominant due to reverse recovery charge or junction capacitor charge of free-wheeling device at hard-switching condition. Soft switching techniques can greatly reduce the turn-on switching loss, in which resonance between a inductor and a capacitor is utilized in order to achieve zero-voltage switching (ZVS) [6-5]-[6-7]. However, in order to satisfy conditions for ZVS, these methods suffer many drawbacks such as, e.g. a requirement of additional components, or a restriction of controllable duty ratio. The additional components not only restricts the minimization of the converter but also complicates the control method, whereas the limitation of the duty ratio restricts the applicable range of ZVS. Therefore, the achievement of ZVS without additional components or the limited controllable duty ratio is desired.

On the other hand, TCM operation is the most simple and effective way to achieve ZVS, and is recently introduced in the “Little Box Challenge”, i.e. a worldwide competition in order to push the forefront of power density in today’s converter systems further [6-8]-[6-11]. In TCM, turn-off switching loss can be decreased greatly by connecting a snubber capacitor in parallel with the switching devices, whereas the turn-on switching loss is

eliminated by ZVS. Consequently, the switching frequency can be pushed to hundreds of kHz or several MHz. One of the main drawbacks in TCM applied with pulse-width modulation (PWM) is that the high current ripple is constant over entire load range. Consequently, it is difficult to achieve high efficiency at light load when the load current is relatively low. Therefore, it is desired to reduce the current ripple at light load in order to avoid a sharp decrease in the efficiency [6-8].

Figure 6.1 depicts a typical non-isolated boost converter, where the junction capacitor of the semiconductor devices are shown as $C_{ds1}$ and $C_{ds2}$. In order to minimize the magnetic component, i.e. the boost inductor $L$, the

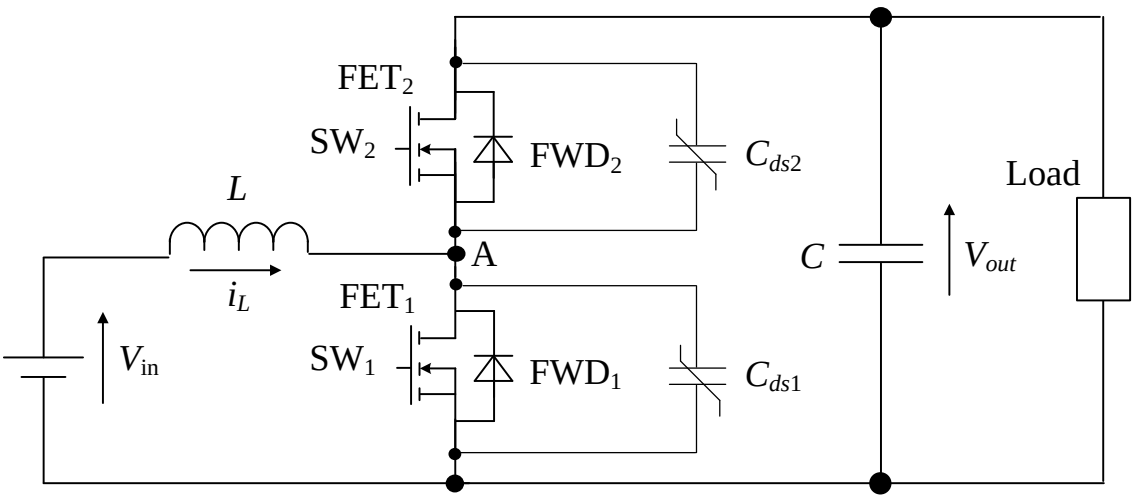


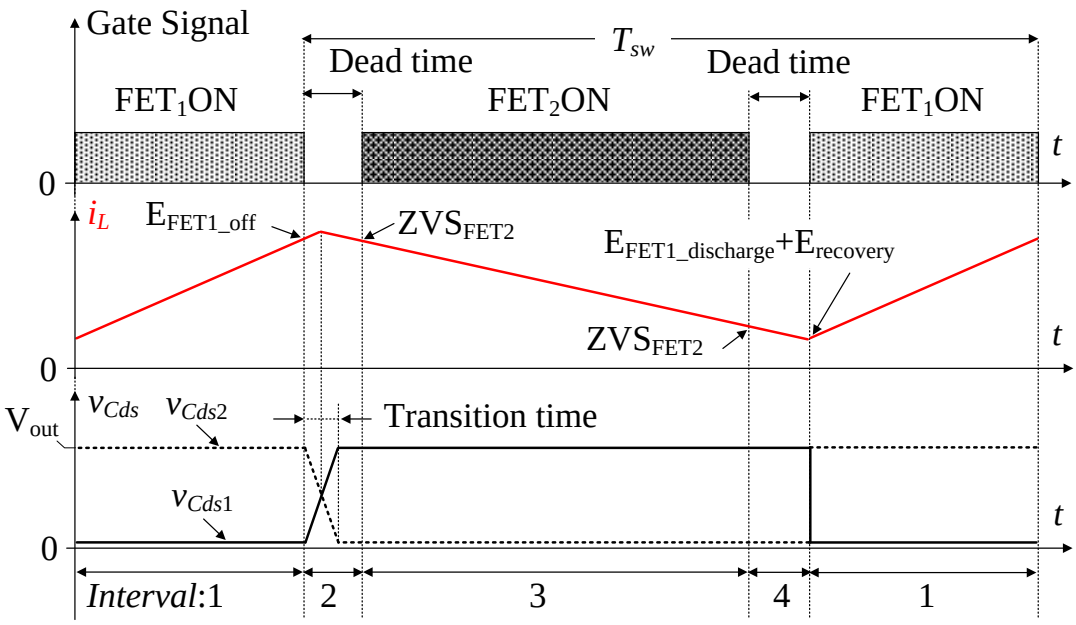

Fig. 6.1. Typical non-isolated boost DC-DC converter. The switching loss reduction is crucial to the high frequency design. In general, there are three current modes to operate the converter: CCM, DCM and TCM.

switching frequency is required to be pushed to hundreds of kHz or even several MHz. Hence, the switching loss reduction is crucial to the high power density design. There are three conventional current modes to operate the boost converter: CCM, DCM and TCM. Note that critical current mode (CRM) can be analyzed as same as DCM without the occurrence of the zero-current interval.

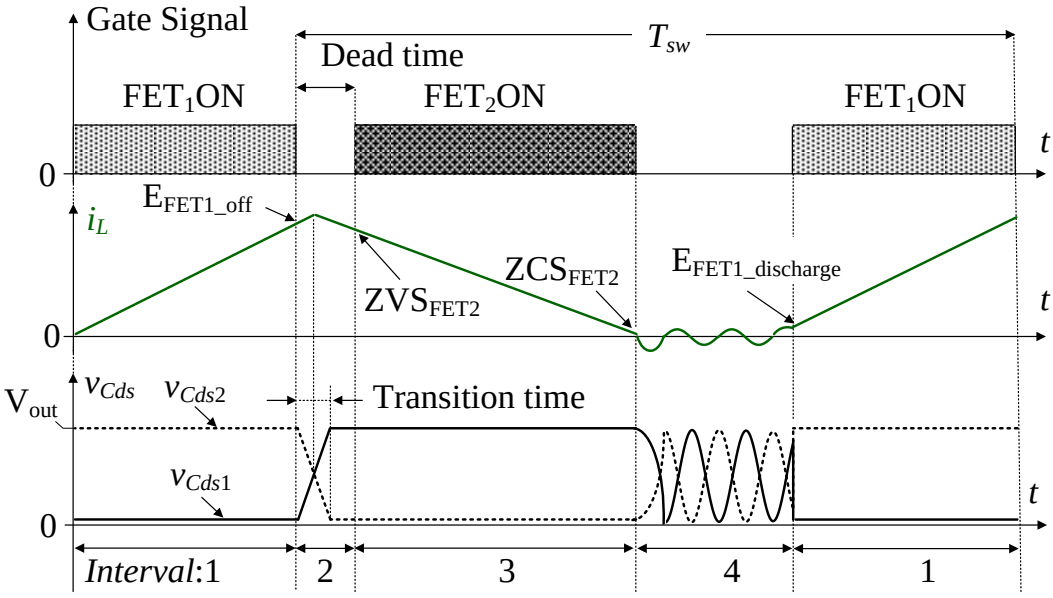
Figure 6.2 depicts the pattern of the switching losses in each current mode. The switching period in CCM as depicted in Fig. 6.2(a) is split into two main intervals and two short resonant transitions.

*Interval* 1 (CCM): During interval 1, the switch $SW_1$ is closed, the input voltage $V_{in}$ is applied to the inductor $L$, and the inductor current $i_L$ increases linearly. At the end of the interval 1, $SW_1$ is turned off. Consequently, the turn-off loss occurs on $SW_1$.

*Interval* 2 (CCM): During interval 2, a switching transition takes place where the junction capacitor $C_{ds1}$ is charged and $C_{ds2}$ is discharged. When $C_{ds1}$ is fully charged to the output voltage $V_{out}$, $FWD_2$ starts to conduct the inductor current $i_L$. At the end of the interval 2, $SW_2$ is turned on at the forward voltage of $FWD_2$, which is considered as ZVS.

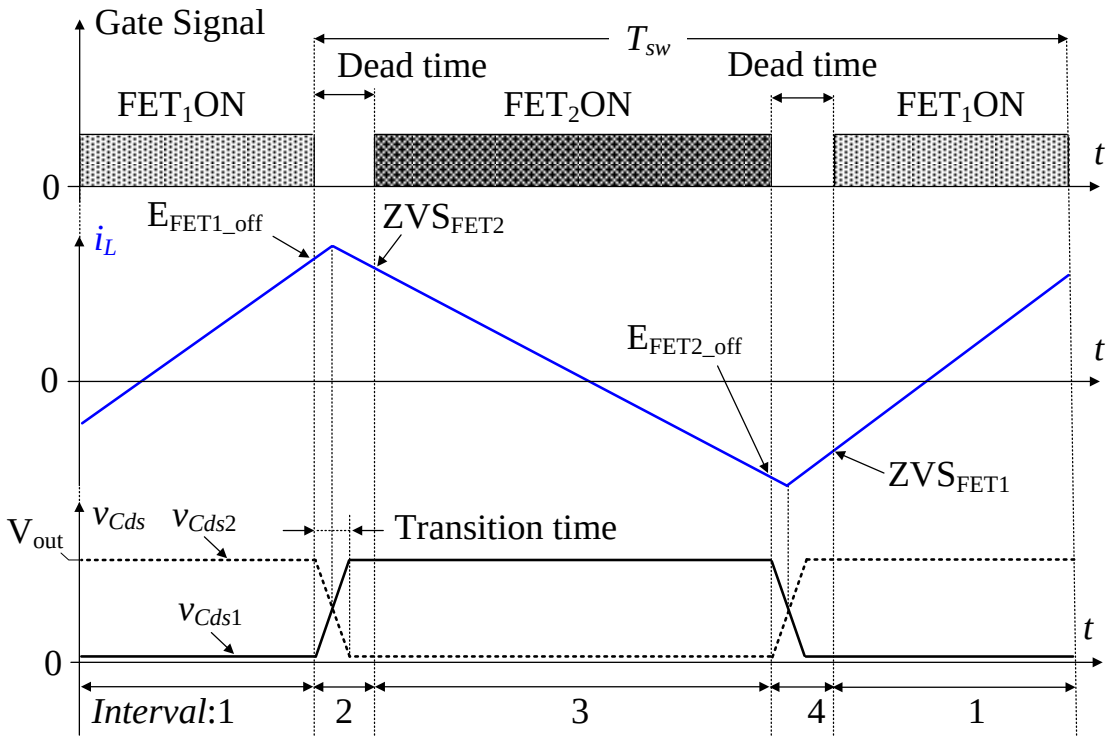



(6.2.a) Switching losses in CCM. In CCM, the free-wheeling diode suffers from the significant reverse recovery loss.




(6.2.b) Switching losses in DCM. The reverse recovery issues can be alleviated by DCM. Nevertheless, in DCM, two kinds of switching loss still occur; the high turn-off loss because the switching devices is turned off at least twice of the average current, and the turn-on loss due to the junction capacitor charge.

*Interval* 3 (CCM): During interval 3, the voltage applied to $L$ is negative




(6.2.c) Switching losses in TCM

Fig. 6.2. Switching losses in CCM, DCM and TCM. In TCM, the turn-off loss can be reduced simply by connecting a snubber capacitor in parallel with the switching devices, whereas the turn-on loss is eliminated by using the boost inductor to resonate out the junction capacitor charge before the turn-on, i.e. ZVS. However, the high current ripple is constant over entire load range with the application of PWM, which decreases the efficiency at light load.

and $i_L$ decreases linearly. At the end of the interval 2, $SW_2$ is turned off and the inductor current commutates from $FET_2$ to $FWD_2$. This current commutation clamps the voltage of $SW_2$ to the forward voltage of $FWD_2$. As a result, the turn-off of $SW_2$ is considered as ZVS.

*Interval* 4 (CCM): During interval 4, $i_L$ continues to decrease. As soon as

the dead time has passed, $SW_1$ is turned on. The inductor current $i_L$ commutates from $FWD_2$ to $FET_1$ which leads to the forceful turn-off of $FWD_2$. This results in the high reverse recovery current and the high reverse recovery loss [6-12]. Note that $FET_1$ is turned on when $C_{ds1}$ is fully charged at the output voltage $V_{out}$. Consequently, additional loss coming from the discharge of $C_{ds1}$ occurs.

On the other hand, the switching period in DCM as depicted in Fig. 6.2(b) is split into two main intervals and two resonant transitions.

*Interval* 1 and *Interval* 2 (DCM): these intervals are similar to the intervals in CCM.

*Interval* 3 (DCM): At the end of interval 3, $i_L$ reaches zero and $SW_2$ is turned off. Therefore, zero-current switching (ZCS) is achieved.

*Interval* 4 (DCM): During interval 4, $L$, $C_{ds1}$, and $C_{ds2}$ form a resonant circuit which starts to oscillate. The behavior of the oscillation depends on the input to output voltage ratio $V_{in}/V_{out}$ [6-9]. Due to this oscillation, at the moment when $SW_1$ is turned on at the end of interval 4, the voltage of $C_{ds1}$ varies from 0V to $V_{out}$ depending on the circuit condition. On the other words, $SW_1$ can still be turned on under the condition that $C_{ds1}$ is charged

and the loss coming from the discharge of $C_{ds1}$ still occurs. Hence, the hard switching still occurs in DCM.

In order to allow for ZVS over entire period, TCM has been proposed [6-8]-[6-11]. The switching period in TCM as depicted in Fig. 6.2(c) is split into two main intervals and two resonant transitions.

*Interval* 1 and *Interval* 2 (TCM): these intervals are similar to the intervals in CCM.

*Interval* 3 (TCM): Different from DCM, instead of turning off $SW_2$ when $i_L$ reaches zero, $SW_2$ is still kept on in order to let $i_L$ become negative. At the end of interval 3, $SW_2$ is finally turned off. Consequently, the turn-off loss occurs on $SW_2$.

*Interval* 4 (TCM): During interval 4, a switching transition takes place in which $C_{ds2}$ is charged and $C_{ds1}$ is discharged. When $C_{ds2}$ is fully charged, $FWD_1$ starts to conduct $i_L$. At the end of the interval 4, $SW_1$ is turned on at the forward voltage of $FWD_1$, which is considered as ZVS. Note that TCM is basically similar to CCM but the current ripple in TCM is intentionally designed high enough to let the current become negative in one switching period (cf., Section 6.3) [6-11].

To conclude, the principle of the ZVS achievement in TCM is to flow a current through the free-wheeling diode before the turn-on of the switches in order to discharge the junction capacitor. Besides, it should be noted that the turn-off loss can be reduced simply by connecting a snubber capacitor in parallel with the switches. A drawback of TCM, however, is a large current ripple which decreases notably the efficiency at light load [6-8]. Therefore, the current ripple reduction of TCM at light load is desired. In order to reduce the current ripple, one of the conventional methods is to increase the switching frequency at light load, i.e. the Pulse Frequency Modulation (PFM) [6-9]-[6-10]. However, PFM is undesirable in many power electronic systems because it is difficult to design a filter circuit for the operation across a wide range of frequencies [6-13]-[6-14]. On the other hand, in DCM, because the current ripple becomes smaller at light load, the high efficiency can be maintained [6-15]. As mentioned above, because DCM still suffers the high turn-on loss, the method to achieve ZVS in DCM is desired. Therefore, this paper proposes the novel concept where TCM and DCM are combined in order to utilize the advantages of these current modes, i.e. ZVS in TCM and the current ripple reduction at light

load in DCM.

Figure 6.3 illustrates the concept of the hybrid discontinuous current mode (HDCM) between DCM and TCM. During the zero-current interval in DCM, i.e. the interval 4 as depicted in Fig. 6.2(b), instead of letting the current return to zero, the switches are modulated in order to flow the TCM current. Consequently, the condition in order to achieve ZVS in DCM can be satisfied by the TCM current during the interval 4 as shown in Fig. 6.3. Note that the switching losses during the TCM interval are negligibly small as explained above. Furthermore, because the total charge during the TCM

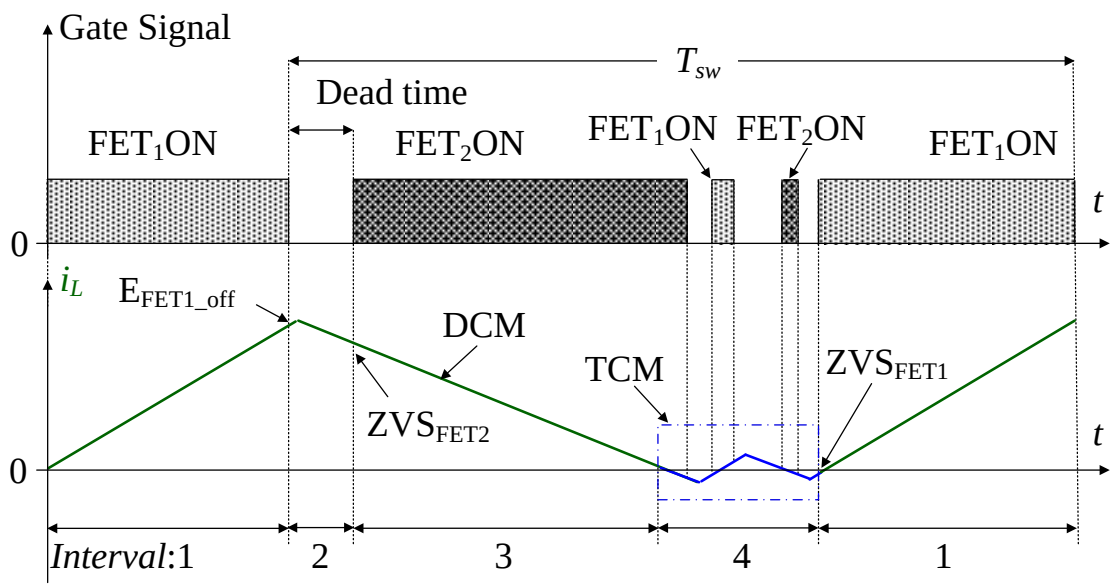



Fig. 6.3. Hybrid discontinuous current mode between DCM and TCM. By applying TCM during the zero-current interval of DCM, the condition for ZVS is achieved, whereas the current ripple can still be reduced at light load.

interval can be controlled to become negligibly small, the TCM interval has no effects on the average current which is generated by the DCM interval. On the other words, the current ripple at light load can still be reduced by the DCM operation. As a result, both ZVS and the current ripple reduction at light load are achieved without additional components or the limitation of the duty ratio.

## 6.3 Operation of Hybrid Discontinuous Current Mode

Based on the mechanism of the switching loss occurrence discussed in Section 6.2, the design and control of the boost converter for HDCM is described in this section. The derivation of the ZVS condition has to be carried out for two cases: $V_{in}>V_{out}/2$ and $V_{in}<V_{out}/2$. However, for the sake of brevity, only the case of $V_{in}>V_{out}/2$ is discussed in the following, whereas the case of $V_{in}<V_{out}/2$ is derived analogously [6-9].

### 6.3.1 Converter Design

Figure 6.4 depicts the HDCM operation waveforms of the gate signal, the junction capacitor voltage and the inductor current at rated load in case of $V_{in}>V_{out}/2$. HDCM is utilized in order to reduce the current ripple at light load and to allow for ZVS during the complete period. Hence, HDCM basically becomes TCM at rated load.

During the positive-current interval $T_{main}$, when $SW_1$ is turned off at $t_1$, due to the high current peak at rated load, the current is higher than the required positive current $I_{R_p}$ which is the current value satisfying the condition for the ZVS achievement of $SW_2$. Similarly, the required negative current $I_{R_n}$ stands for the current value which discharges completely $C_{ds1}$,

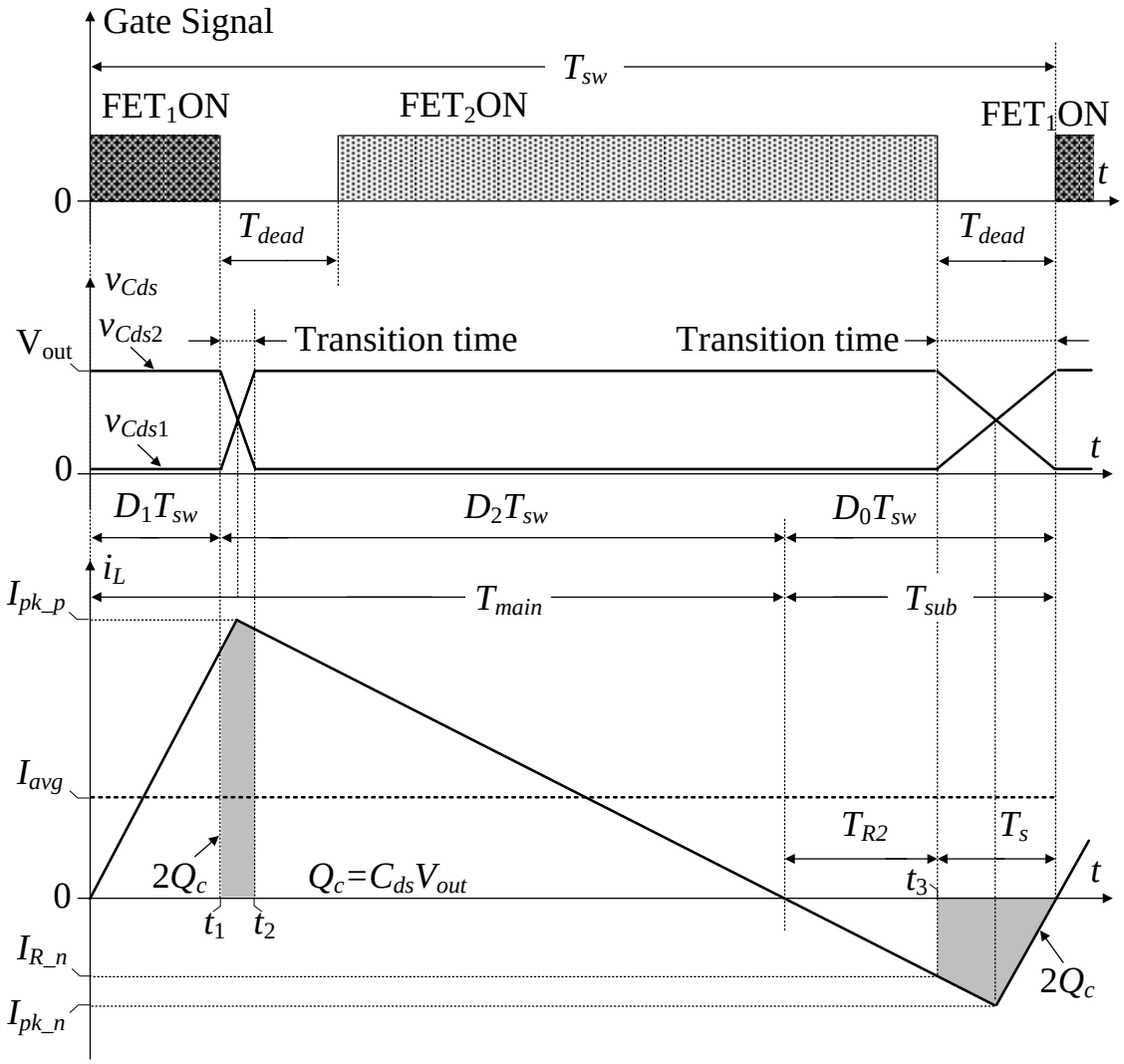



Fig. 6.4. HDCM operation waveforms of gate signal, junction capacitor voltage and inductor current at rated load in case of $V_{in}>V_{out}/2$. The design of the boost inductance $L$ and the dead time $T_{dead}$ is carried out in TCM which allows for ZVS at rated load.

i.e. one of the conditions for the ZVS achievement of SW$_1$. Considering the negative-current interval $T_{sub}$, as soon as FET$_2$ is turned off at $t_3$, $C_{ds1}$ and $C_{ds2}$ are connected in parallel. In order to discharge $C_{ds1}$, the charge $Q_c$ has to be removed and, assuming identical switches, the same charge $Q_c$ is

required to charge $C_{ds2}$ to $V_{out}$. The larger the negative inductor current is, the shorter the transition time becomes. However, this negative current should be minimized in order not to increase the current ripple, which causes excessive conduction loss and decreases the efficiency at rated load. The required negative current $I_{R_n}$ is independent of the output power but only depends on $V_{in}$, $V_{out}$, $L$ and the selected switch which defines $C_{ds}$ [6-9]-[6-10],

$$I_{R_n} = \sqrt{\frac{2C_{ds}V_{out}(2V_{in} - V_{out})}{L}} \quad \text{.....} (6.1)$$

When $FET_2$ is precisely turned off at the moment $i_L$ reaches $I_{R_n}$, the resonance between $L$ and $C_{ds}$ continues to flow $i_L$ until it reaches the negative current peak $I_{pk_n}$,

$$I_{pk_n} = \sqrt{\frac{2C_{ds}V_{out}V_{in}}{L}} \quad \text{.....} (6.2)$$

Assuming that at rated load, the boost converter transmits the average current $I_{avg}$ to the load over a switching period $T_{sw}$ and also generates the negative current $I_{pk_n}$ for the ZVS achievement, the boost inductance $L$ *and* the dead time $T_{dead}$ which achieve the minimum current ripple are derived as following. First, the positive-curent interval $T_{main}$ and the

negative-current interval $T_{sub}$ are geometrically derived from the corresponding peak current $I_{pk_p}$ and $I_{pk_n}$,

$$T_{main} = I_{pk_p} L \left( \frac{1}{V_{out} - V_{in}} + \frac{1}{V_{in}} \right) \quad \text{.....(6.3)}$$

$$T_{sub} = I_{pk_n} L \left( \frac{1}{V_{out} - V_{in}} + \frac{1}{V_{in}} \right) \quad \text{.....(6.4)}$$

In the boost converter applied with PWM, $T_{sw}$ is constant, whereas $I_{avg}$ is the total charge over $T_{sw}$,

$$T_{sw} = T_{main} + T_{sub} \quad \text{.....(6.5)}$$

$$I_{avg} = f_{sw} \left( \frac{1}{2} I_{pk_p} T_{main} - \frac{1}{2} I_{pk_n} T_{sub} \right) \quad \text{.....(6.6)}$$

Substituting (6.3) and (6.4) into (6.5) and (6.6) and solving for the boost inductance $L$, (6.7) is obtained.

$$L = \frac{1}{f_{sw}^2 \left( \frac{1}{V_{out} - V_{in}} + \frac{1}{V_{in}} \right)^2} \cdot$$

$$\frac{1}{\left[ \sqrt{2C_{ds} V_{out} V_{in}} + \sqrt{2C_{ds} V_{out} V_{in} + \frac{2I_{avg}}{f_{sw} \left( \frac{1}{V_{out} - V_{in}} + \frac{1}{V_{in}} \right)}} \right]^2} \quad \text{.....(6.7)}$$

Then, the dead time $T_{dead}$ is designed longer than the transition time $T_s$

in order to resonate out completely the charge in the junction capacitor before the switches are turned on,

$$T_s = L\left(\frac{I_{pk_n} - I_{R_n}}{V_{out} - V_{in}} + \frac{I_{R_n}}{V_{in}}\right) \quad (6.8)$$

To conclude, when the boost converter transmits $I_{avg}$ to the load over $T_{sw}$ at rated load, the condition to achieve ZVS is that $L$ and $T_{dead}$ have to satisfy (6.7) and (6.8), respectively.

## 6.3.2 Control System

Figure 6.5 depicts the control system of the boost converter operating in HDCM. The voltage and current regulators and the calculation for the duty ratios are implemented into a digital signal processor (DSP), whereas the switching signals are generated by a field-programmable gate array (FPGA) based on the duty ratios received from the DSP. In order to regulate the output voltage $V_{out}$ in response to the line, the load, and the parameter variations, a PI controller is employed into the voltage regulator

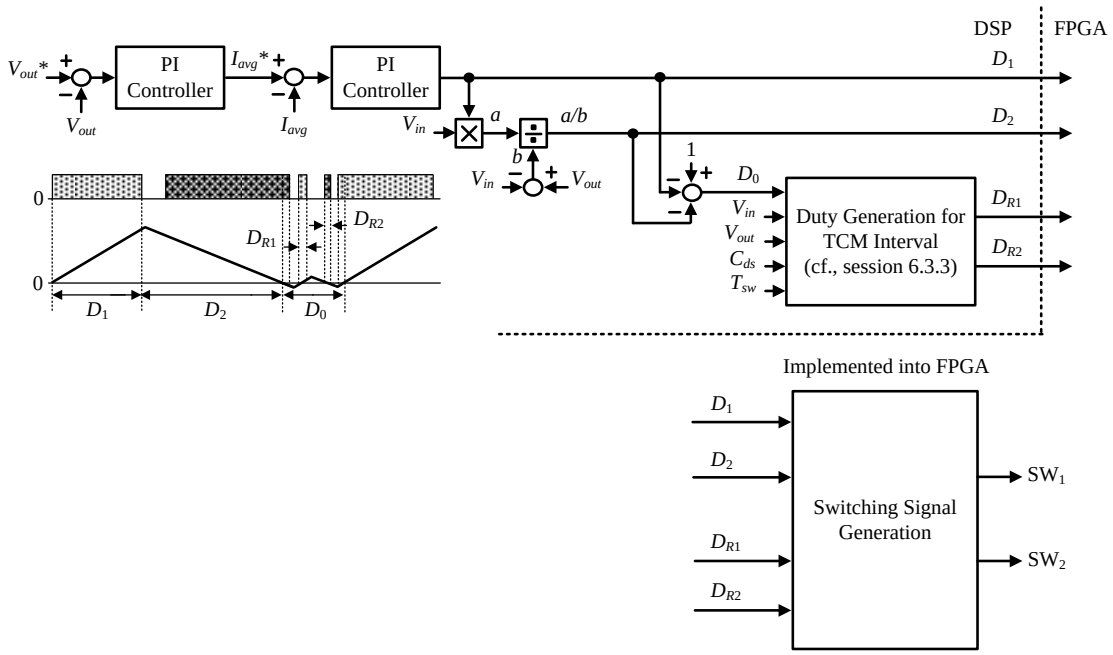



Fig. 6.5. Control system of boost converter operating in HDCM. A FPG6-based DSP is employed in order to control the boost converter operating in HDCM. Owing to the online calculation of the duty ratios, a real-time closed-loop control of HDCM can be realized.

as a major control loop. The output of the voltage regulator, i.e. the average inductor current $I_{avg}$*, is then used as a command for the current regulator. Note that the current regulator which is designed in order to deal with the nonlinearity in DCM has been researched thoroughly in [6-16]-[6-19]. The current regulator outputs the duty ratio $D_1$ of the positive-current interval $T_{main}$ as shown in Fig. 6.4. Based on the relationship between the current slopes during $T_{main}$ [6-16], the duty ratio $D_2$ of $SW_2$ and the duty ratio $D_0$ of the zero-current interval, i.e. the TCM interval, are estimated as follows,

$$D_2 = D_1 \frac{V_{in}}{V_{out} - V_{in}} \quad \text{.....} (6.9)$$

$$D_0 = 1 - D_1 - D_2 \quad \text{.....} (6.10)$$

Then, the following parameters are used to generate the duty ratios $D_{R1}$ and $D_{R2}$ for the TCM interval (cf., Section 6.3.3): the duty ratio $D_0$, the input voltage $V_{in}$, the output voltage $V_{out}$, the junction capacitor value $C_{ds}$, and the switching period $T_{sw}$. Finally, the switching signals are generated in the FPGA by comparing the duty ratios $D_1$, $D_2$, $D_{R1}$ and $D_{R2}$ with multiple counters. Owing to the online calculation of the duty ratios, a real-time closed-loop control of the proposed current mode (HDCM) can be realized.

### 6.3.3 Duty Generation for Triangular Current Mode Interval

At light load, the negative current in TCM increases due to the constant switching frequency, which increases the ratio between the current ripple and the average current. Consequently, the efficiency at light load decreases sharply [6-8], [6-15]. Therefore, HDCM is applied at light load in order to reduce the current ripple load and to achieve ZVS.

Figure 6.6 depicts the flowchart of the switching signal generation during the TCM interval in HDCM. It is necessary to control the turn-on period of the switches during the TCM interval as depicted in Fig. 6.3 so that the following conditions are satisfied;

(i) the TCM interval has no influence on the DCM operation, which implies that the total charge during the TCM interval is required to be negligibly small,

(ii) the ZVS condition for the next DCM period is satisfied, which implies that the current value at the end of the TCM interval is required to be adjusted according to the zero-current interval of DCM by controlling the TCM current peak and the TCM period,

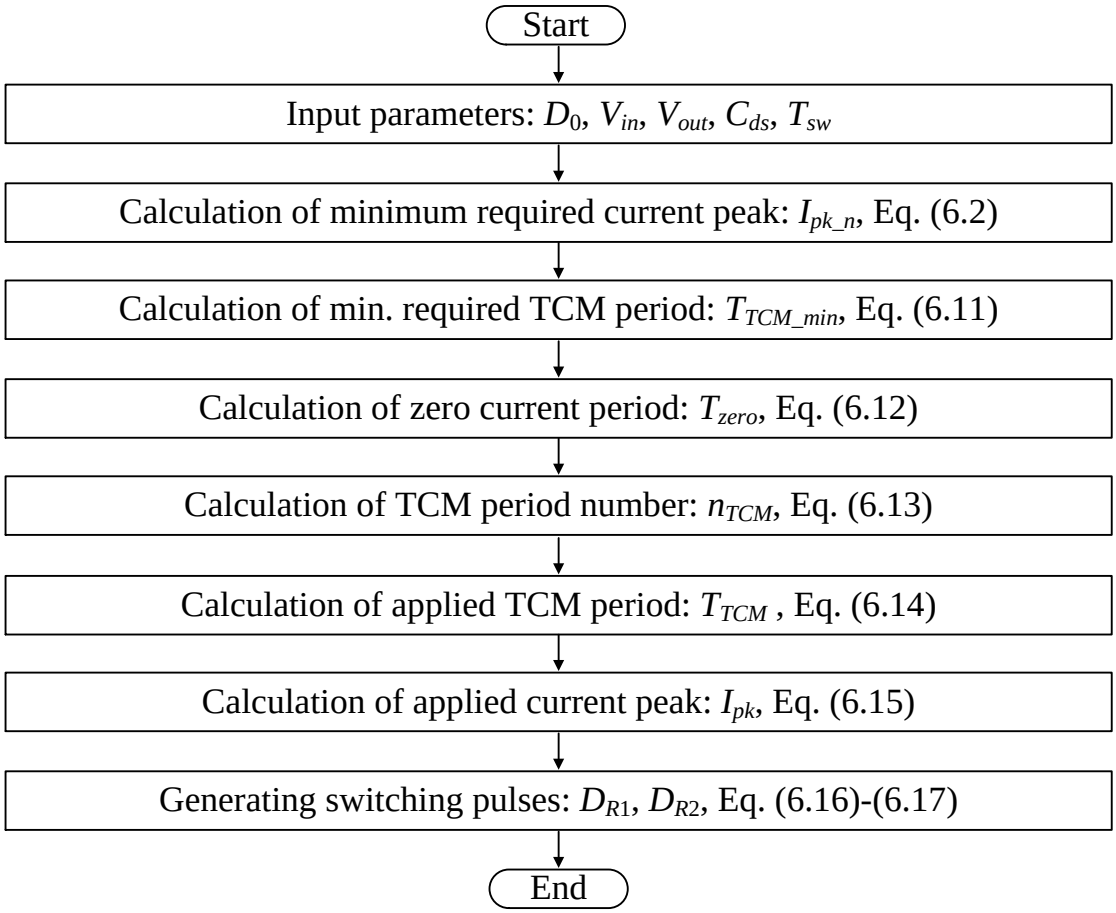



Fig. 6.6. Flowchart of switching signal generation during TCM interval. Because the TCM current is flown in order to achieve the ZVS condition for DCM, the losses and the charge from the additional TCM current is required to be minimized. Furthermore, it is also necessary to achieve ZVS during the TCM interval.

(iii) the losses from the TCM interval such as the conduction loss are minimized, which implies that the TCM current peak is large just enough to achieve ZVS over the TCM interval.

Figure 6.7 depicts the HDCM operation waveforms of the gate signal, the junction capacitor voltage and the inductor current at light load. Note

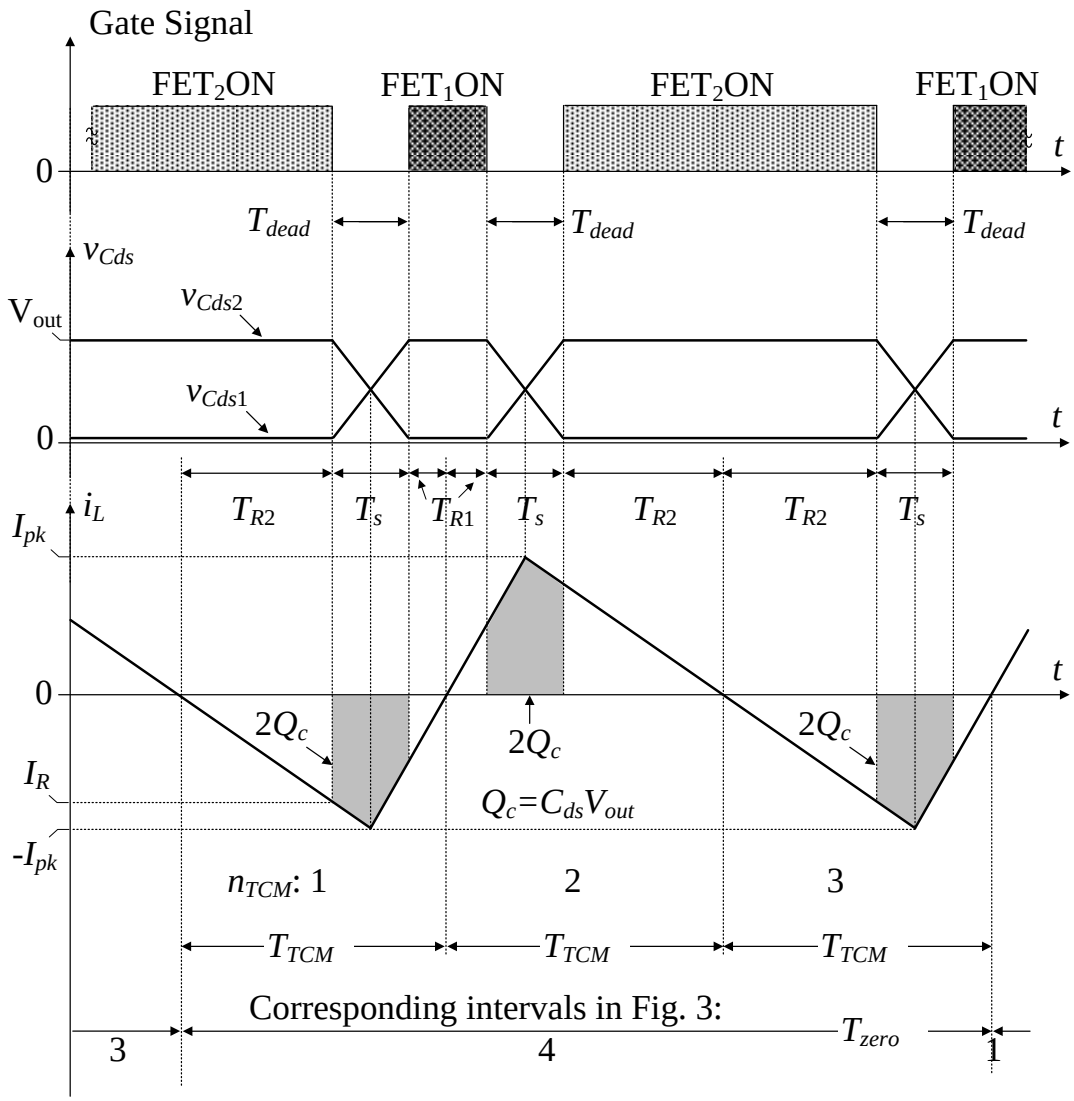



Fig. 6.7. HDCM operation waveforms of gate signal, junction capacitor voltage and inductor current at light load. In order to achieve ZVS for the DCM operation, the TCM period $T_{TCM}$ is adjusted according to the zero-current period $T_{zero}$. Furthermore, in order to minimize the losses from the additional TCM current, the current peak $I_{pk}$ is designed to be just large enough to achieve ZVS for both switches $SW_1$ and $SW_2$ during the TCM interval. Finally, in order to make the TCM interval has no influence on the DCM operation, which implies the total charge from the additional TCM current is negligibly small, the positive and negative values of the current peak $I_{pk}$ are controlled to become equal.

that only the zero-current interval in which TCM is applied is shown. First,

the minimum current peak $I_{pk_n}$ which achieves the condition of ZVS for $SW_1$ is calculated from the total charge stored $Q_c$ in the junction capacitor $C_{ds}$ as in (6.2). In order to let the inductor current reach the peak $I_{pk_n}$, the required TCM period $T_{TCM_min}$ is calculated by (6.11),

$$T_{TCM_\min} = I_{pk_n} L \left( \frac{1}{V_{out} - V_{in}} + \frac{1}{V_{in}} \right) \quad \text{.....} (6.11)$$

Next, the number of the TCM period $n_{TCM}$ is calculated from the zero-current period $T_{zero}$ as shown in Fig. 6.6. The zero-current period $T_{zero}$ is calculated from the duty ratio $D_0$ [16],

$$T_{zero} = D_0 T_{sw} \quad \text{.....} (6.12)$$

In order to minimize the losses from the TCM interval, the current peak $I_{pk}$ of the TCM current is required to be minimal. Consequently, it is necessary to choose the number of the TCM period $n_{TCM}$ as a maximum odd number,

$$n_{TCM} \le \frac{T_{zero}}{T_{TCM_\min}}; n_{TCM} \text{ is an odd number.} \quad \text{.....} (6.13)$$

Next, the applied TCM period $T_{TCM}$ is calculated from the zero-current period $T_{zero}$ and the number of the TCM period $n_{TCM}$,

$$T_{TCM} = \frac{T_{zero}}{n_{TCM}} \quad \text{.....} (6.14)$$

Then, the applied current peak $I_{pk}$ of the TCM current is calculated as in (6.15),

$$I_{pk} = \frac{T_{TCM}}{L\left(\frac{1}{V_{out} - V_{in}} + \frac{1}{V_{in}}\right)} \quad \text{.....} (6.15)$$

Finally, the duty ratios $D_{R1}$ and $D_{R2}$ of $SW_1$ and $SW_2$ in order to achieve the TCM current peak $I_{pk}$ is calculated as in (6.16) and (6.17), respectively [6-9],

$$D_{R1} = \frac{L}{f_{sw} V_{in}} \sqrt{I_{pk}^2 - \frac{2C_{ds} V_{out} V_{in}}{L}} \quad \text{.....} (6.16)$$

$$D_{R2} = \frac{L}{f_{sw}(V_{out} - V_{in})} \sqrt{I_{pk}^2 - \frac{2C_{ds} V_{out}(V_{out} - V_{in})}{L}} \quad \text{.....} (6.17)$$

As depicted in Fig. 6.6, the positive and negative values of the current peak $I_{pk}$ are controlled to be the same, which makes the total charge from the additional TCM current negligibly small. Consequently, the TCM interval has almost no influence on the DCM operation, which implies that the current ripple can be reduced at light load by DCM. Hence, by controlling the TCM current peak during the TCM interval, HDCM both reduces the current ripple load and achieves ZVS.

## 6.4 Experimental Results

Table 6.1 shows the experimental parameters of the circuit and the controllers. A 1-kW prototype is realized with the SiC devices and ferrite core N87. At rated load of 1 kW and the switching frequency of 100 kHz, the inductor value is designed by (6.7) in order to operate the boost converter in TCM. Consequently, three current modes TCM, DCM, and HDCM share the same operation at rated load. On the other hand, in order to operate the boost converter by CCM under the same condition of the boost inductor, the switching frequency is increased to 200 kHz. As a result, the inductor current ripple of CCM at rated load is reduced by half compared to HDCM. On the other words, in order to achieve the same size of the boost inductor by using CCM with the small inductor current ripple compared to HDCM with the high inductor current ripple, the switching frequency has to be increased.

### 6.4.1 Operation Verification

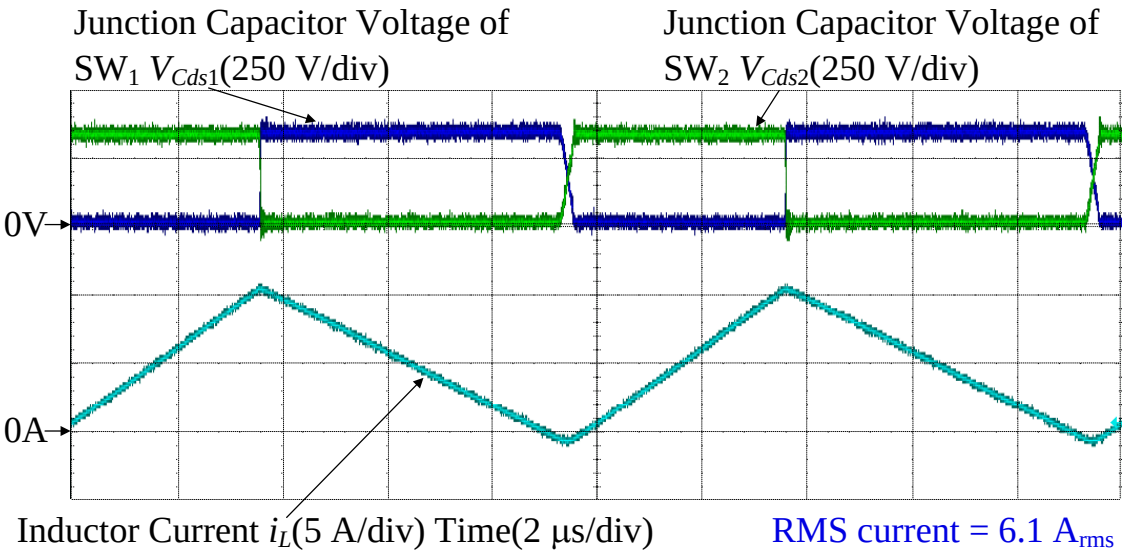
Figures 6.8-6.10 depict the waveforms of the TCM, DCM, HDCM and CCM currents, and the junction capacitor voltages under different

TABLE 6.1.
PARAMETERS OF CIRCUIT AND CONTROLLERS IN EXPERIMENTS.

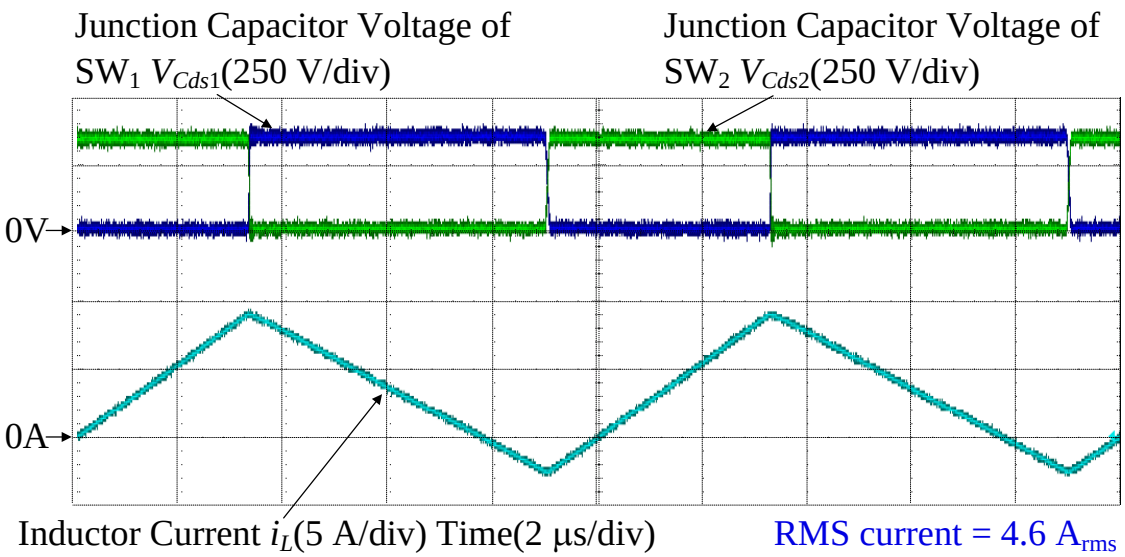
| Symbol | Quantity | Value |
|---|---|---|
| $V_{in}$ | Input Voltage | 200 V |
| $V_{out}$ | Output Voltage | 350 V |
| $P$ | Rated Output Power | 1 kW |
| | Experiments for Efficiency Comparison | |
| | Switching Device | SCH2080KE(ROHM) |
| $L$ | Boost Inductor Value | 70 μH |
| $\Delta i_H$ | Current Ripple at Rated Load in TCM, DCM and HDCM | 100% |
| $f_{sw1}$ | Switching Freq. at Rated Load in TCM, DCM and HDCM | 100 kHz |
| $f_{sw2}$ | Maximum Switching Freq. at Light Load in HDCM | 300 kHz |
| $\Delta i_L$ | Current Ripple at Rated Load in CCM | 50% |
| $f_{sw3}$ | Switching Freq. in CCM | 200 kHz |
| | Experiment for Load Step Response | |
| $C$ | Output Capacitor Value | 360 μF |
| $f_{samp}$ | Sampling Frequency | 25 kHz |
| $f_c$ | Cutoff frequency (Current Regulator) | 500 Hz |
| $\zeta_c$ | Damping factor (Current Regulator) | 0.707 |
| $f_v$ | Cutoff frequency (Voltage Regulator) | 10 Hz |
| $\zeta_v$ | Damping factor (Voltage Regulator) | 0.707 |

conditions of load. At rated load, the current waveforms are same for TCM, DCM and HDCM. The current ripple of TCM in Fig. 6.8 is constant against load. On the other hand, at light load, compared to TCM, the current ripple is greatly reduced by DCM or HDCM. In particular, at light load of 0.2 p.u.,

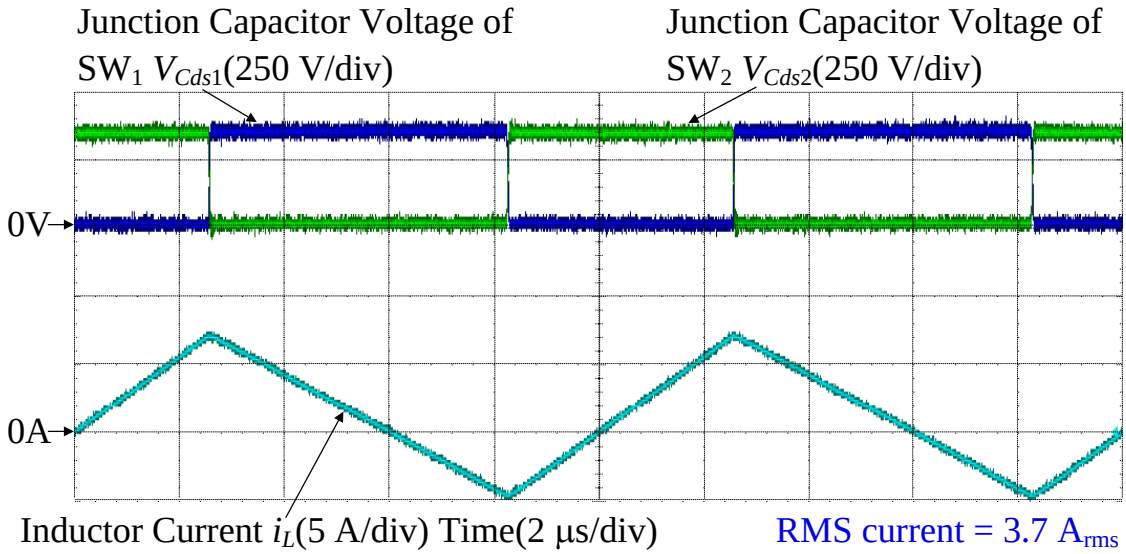
the root-mean-square (RMS) current is reduced from 3.7 $A_{rms}$ (TCM) to 1.8 $A_{rms}$ (DCM) or to 2.1 $A_{rms}$ (HDCM). The RMS current of HDCM is slightly higher than that of DCM due to the employment of the TCM current during the zero-current interval. Furthermore, as shown in Fig. 6.9(c)-(d), the positive and negative values of the TCM current are controlled to be almost the same. Consequently, the addition TCM current has no effects on the DCM operation. This allows the conventional DCM current control to be applied simply to HDCM [6-16]-[6-19]. As shown in Fig. 6.10, by increasing the switching frequency from 100 kHz to 200 kHz, the boost converter is operated in CCM at rated load. Compared to TCM, the smaller RMS current is achieved in CCM due to the increase in the switching frequency.




(6.8.a) TCM current and junction capacitor voltages at rated load

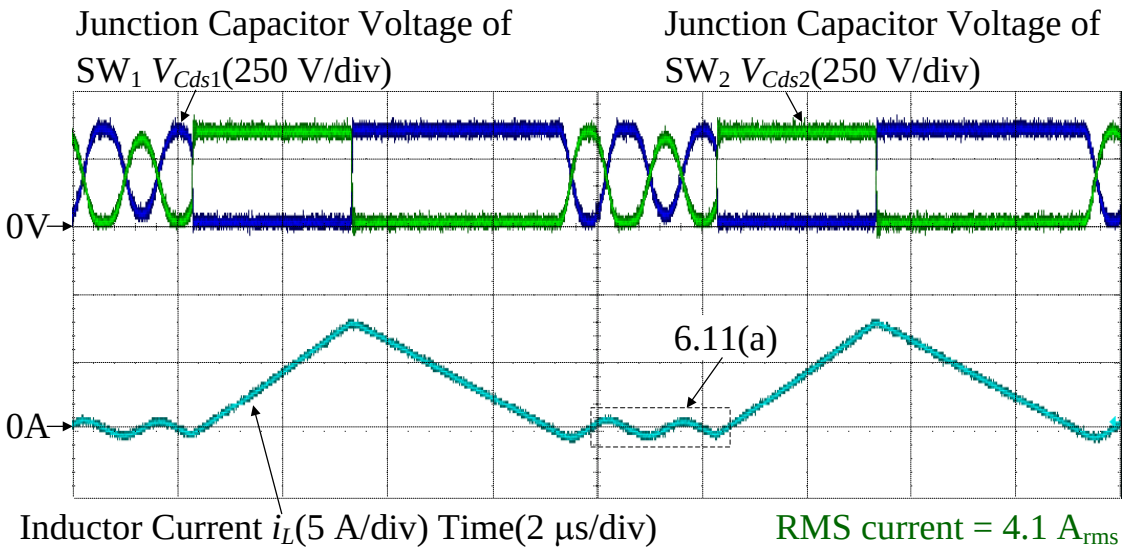



(6.8.b) TCM current and junction capacitor voltages at light load of 0.6 p.u.

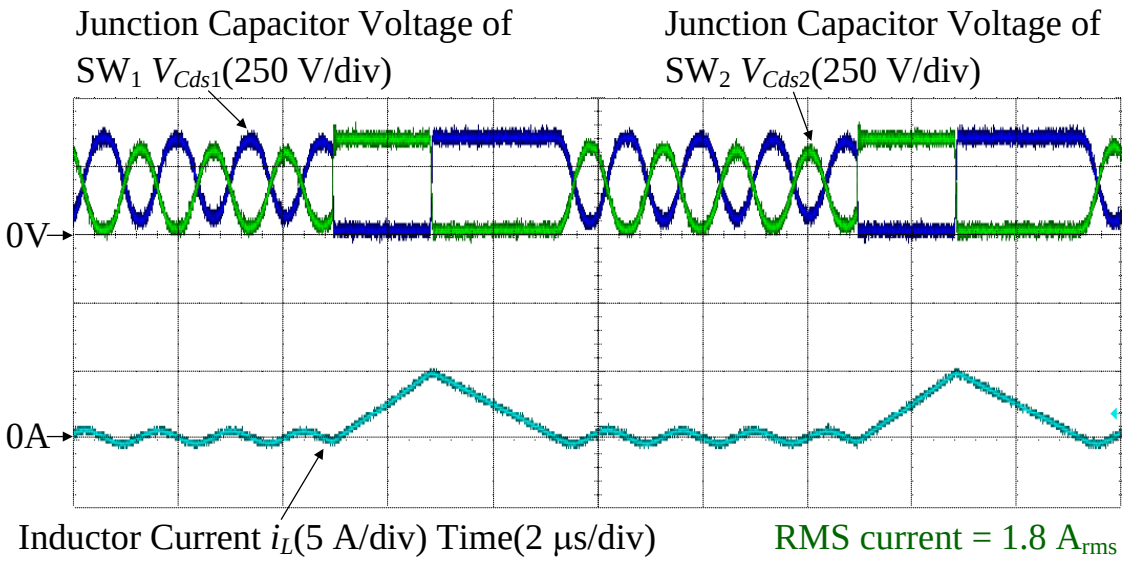



(6.8.c) TCM current and junction capacitor voltages at light load of 0.2 p.u.

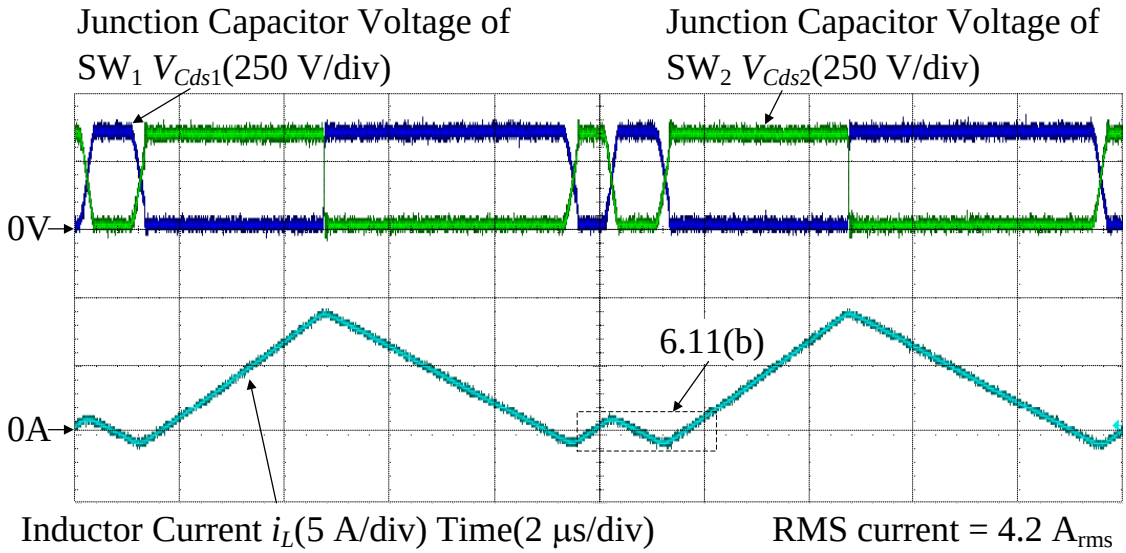
Fig. 6.8. Waveforms of TCM current and junction capacitor voltages under different conditions of load.



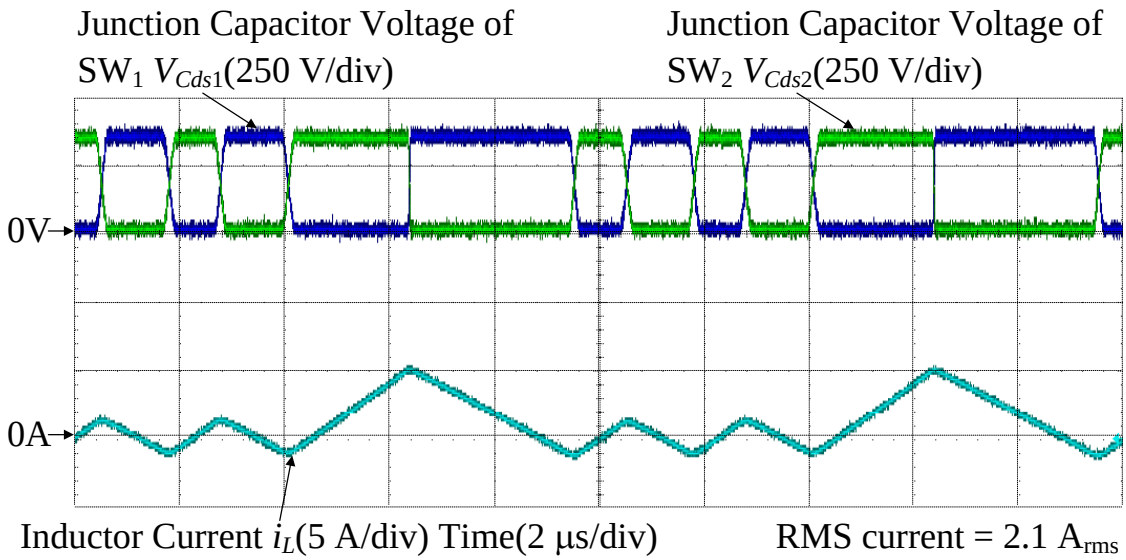

(6.9.a) DCM current and junction capacitor voltages at light load of 0.6 p.u.




(6.9.b) DCM current and junction capacitor voltages at light load of 0.2 p.u.

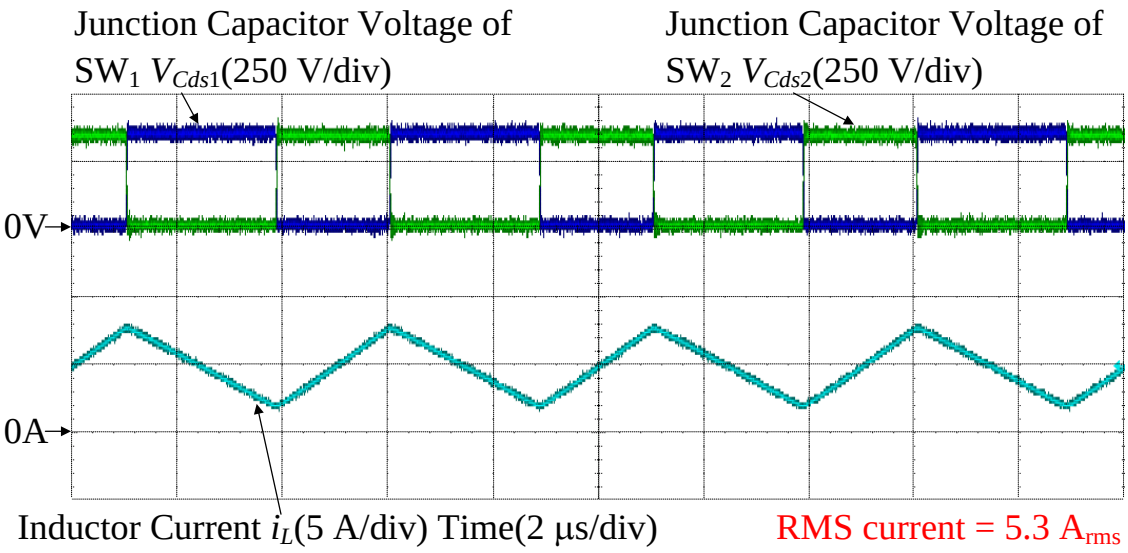



(6.9.c) HDCM current and junction capacitor voltages at light load of 0.6 p.u.

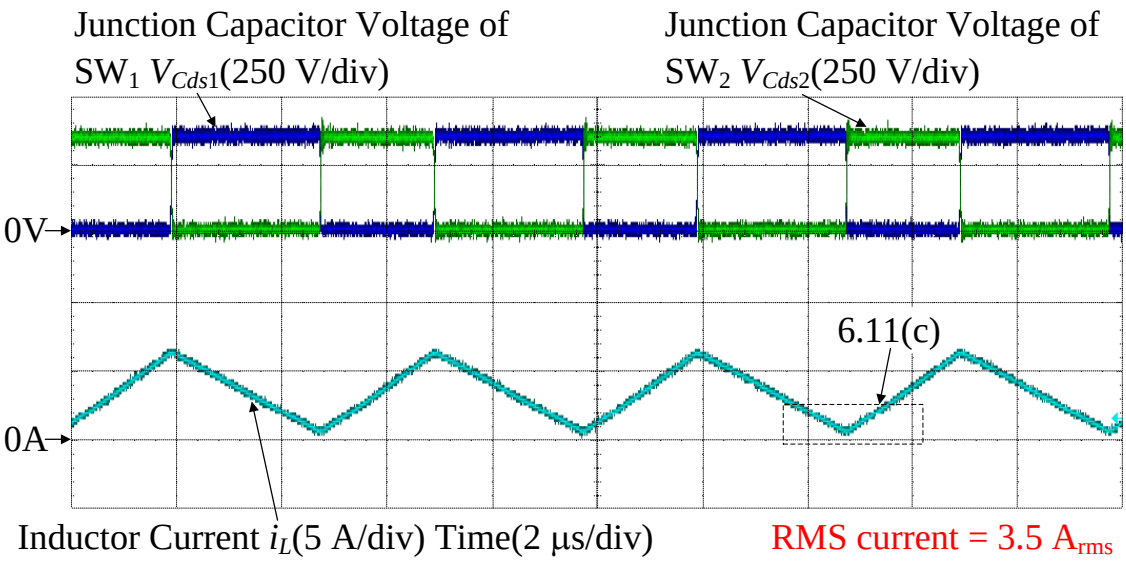



(6.9.d) HDCM current and junction capacitor voltages at light load of 0.2 p.u.

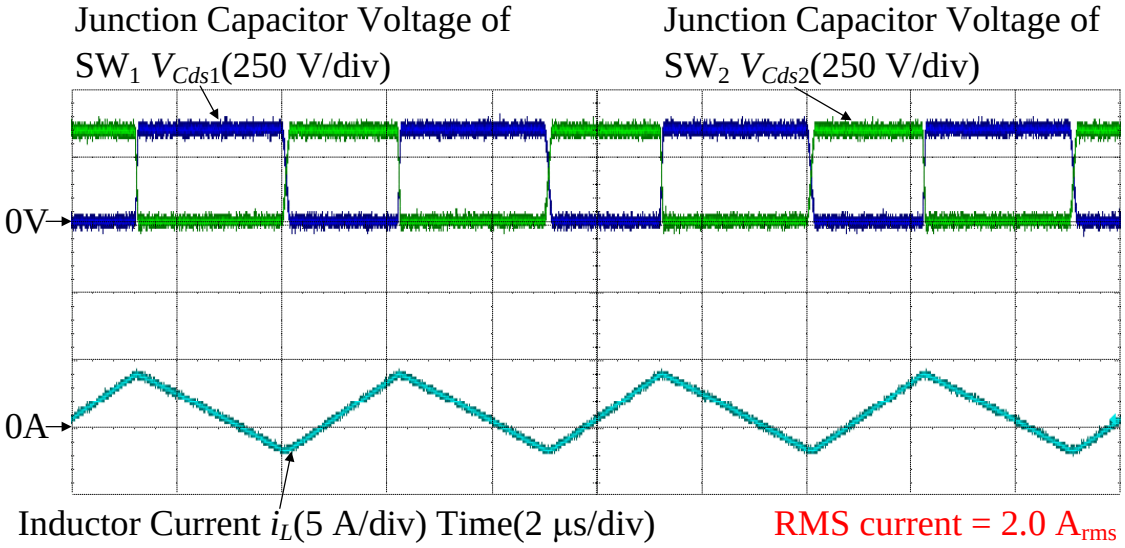
Fig. 6.9. Waveforms of DCM and HDCM currents, and junction capacitor voltages under different conditions of load.




(6.10.a) CCM current and junction capacitor voltages at rated load




(6.10.b) CCM current and junction capacitor voltages at light load of 0.6 p.u.

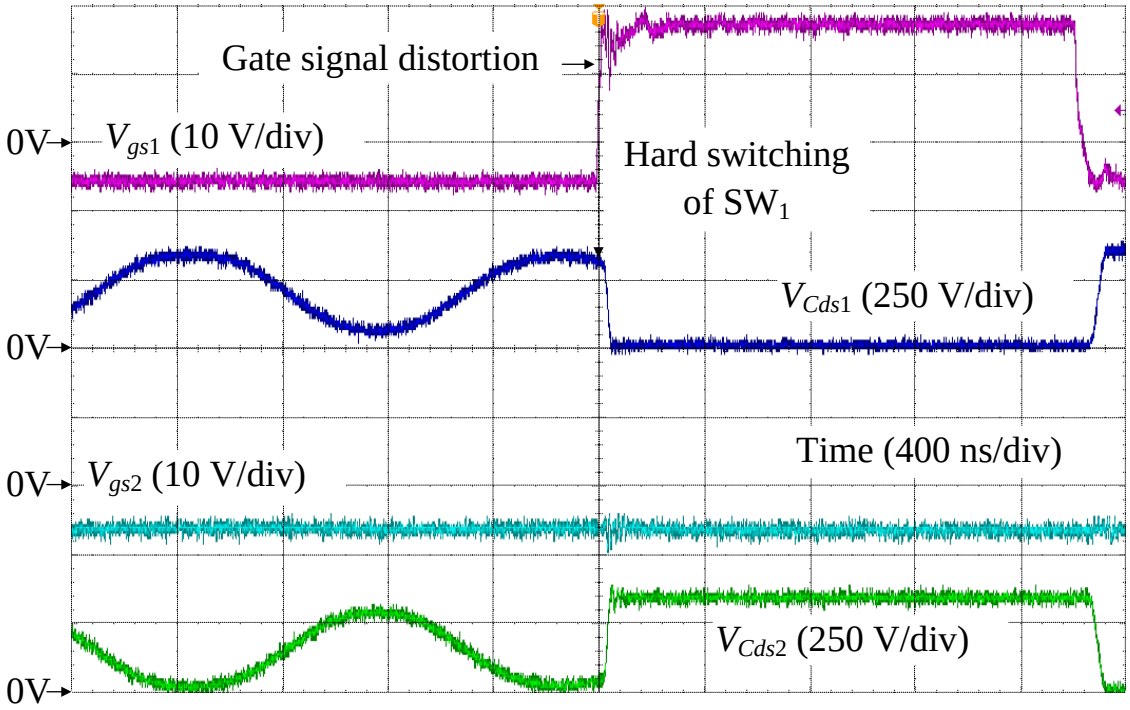



(6.10.c) CCM current and junction capacitor voltages at light load of 0.2 p.u.

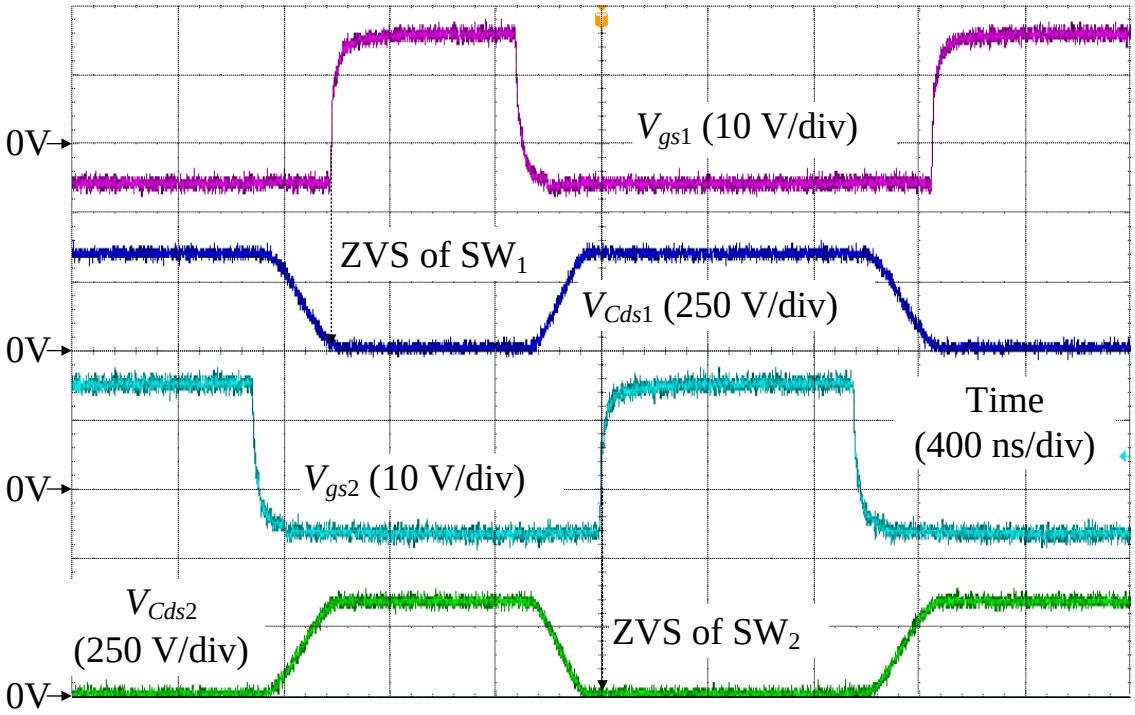
Fig. 6.10. Waveforms of CCM current and junction capacitor voltages under different conditions of load.

Figure 6.11 illustrates the waveforms of the gate signal and the junction capacitor voltage, which is the magnified waveforms from Fig. 6.9(a), 6.9(c), and 6.10(b). As explained in Fig. 6.2(b), the hard switching can still occur in DCM. The switching behavior and the switching loss of DCM depends on the resonance between the boost inductor and the junction capacitors during the zero-current interval. On the other hand, it is confirmed in Fig. 6.11(b) that both the switches $SW_1$ and $SW_2$ are turned on at the zero voltage, i.e. ZVS. Furthermore, the turn-off losses can be simply reduced by connecting a snubber capacitor parallel to the switch in order to delay the rise of the junction voltage. Consequently, low switching

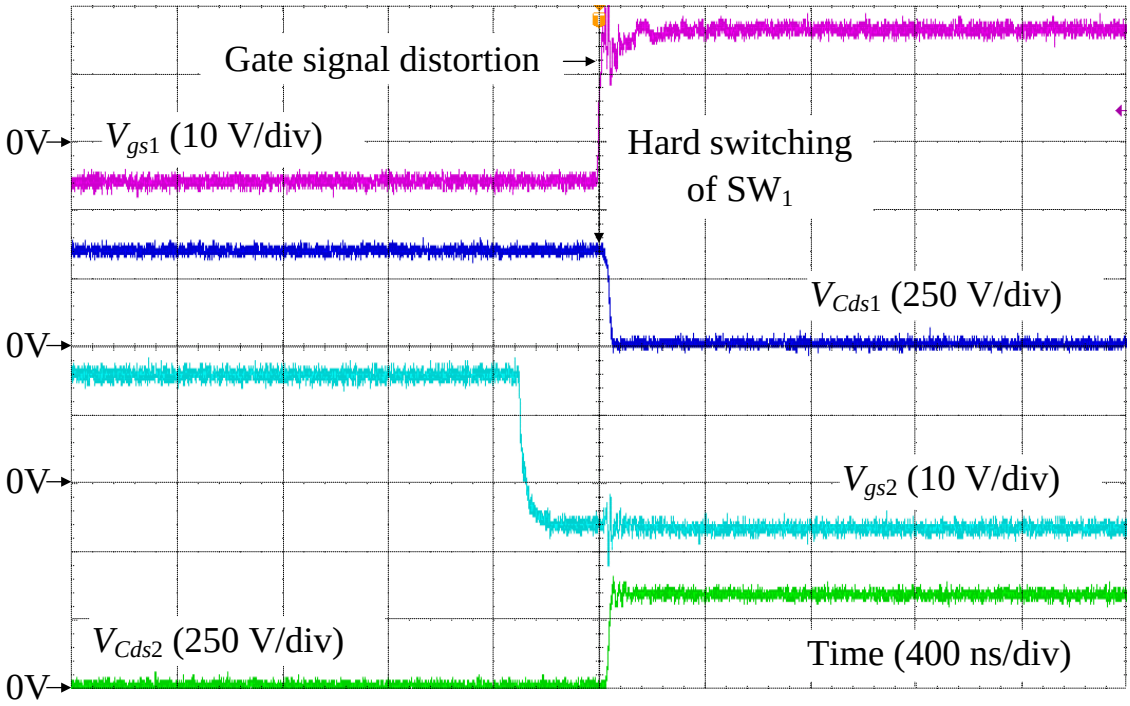
loss can be accomplished in order to further increase the switching frequency and to achieve the high power density. In Fig. 6.11(c), the occurrence of the hard switching is confirmed in CCM similarly to DCM. The hard switching in DCM and CCM not only generates high switching loss but also distorts the gate signal due to the high di/dt of the discharge current from the junction capacitor. The gate signal distortion can lead to the occurrence of the false triggering in CCM and DCM. In order to avoid the occurrence of the false triggering during hard switching in CCM and DCM, the main circuit and the gate driver circuit are required to be customized for the high di/dt of the current, which is undesirable due to the increase in cost. On the other words, the soft switching in HDCM not only reduces the switching loss but also benefits the design cost of the main circuit and the gate driver circuit.




(6.11.a) Hard switching in DCM




(6.11.b) Soft switching in HDCM

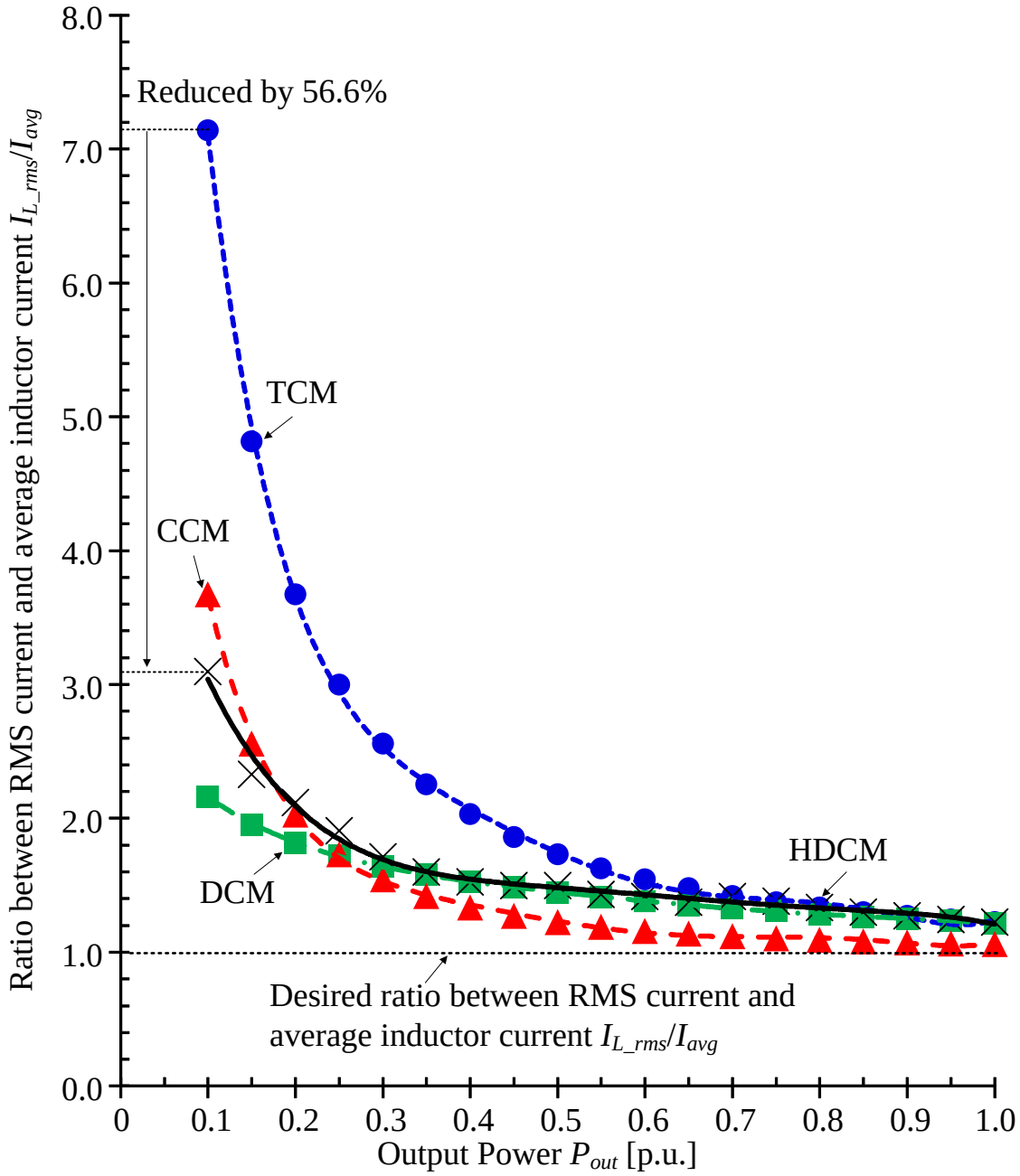



(6.11.c) Hard switching in CCM

Fig. 6.11. Waveforms of gate signal and junction capacitor voltage in DCM, HDCM and CCM which is the magnified waveforms from Fig. 6.9(a), 6.9(c), and 6.10(b).

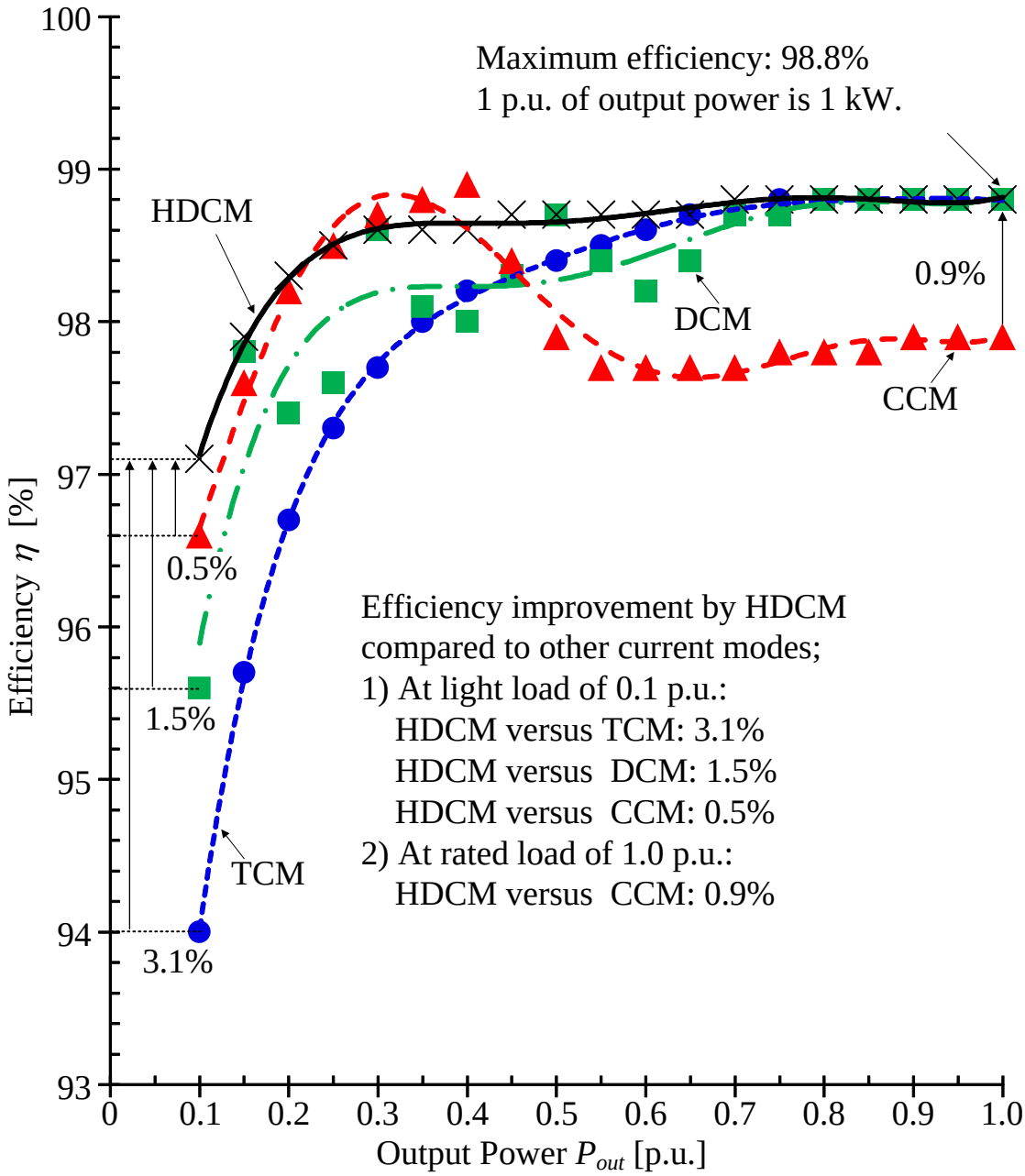
### 6.4.2 Comparisons of Root-Mean-Square Current and Efficiency

Figure 6.12 shows the comparisons of RMS current and efficiency among TCM, DCM, HDCM and CCM. Note that the same boost inductor is used to conduct the experiments of the efficiency comparison. First, as shown in the results of the ratio between the RMS current $I_{L_rms}$ and the average current $I_{avg}$, by utilizing the variable current-ripple characteristic of DCM, the RMS current in HDCM is reduced greatly compared to TCM. In particular, at light load of 0.1 p.u., the RMS current of HDCM is reduced by 56.6%. Besides, the RMS current of HDCM at rated load is as same as that in TCM, because the converter is designed to be operated with TCM at rated load. This design minimizes the required current ripple in order to achieve ZVS at rated load. Consequently, the efficiency of HDCM at rated load is as same as that in TCM, whereas at light load, the efficiency is improved up to 3.1% with HDCM. On the other hand, the RMS current of HDCM is slightly higher than that of DCM due to the employment of the TCM current during the zero-current interval. However, the efficiency of HDCM is higher than that of DCM over entire load range because the hard




(6.12.a) Ratio between RMS current and average current

switching still occurs in DCM. Note that the variation of the DCM efficiency is quite large because the turn-on loss of the hard switching in




(6.12.b) Efficiency characteristic

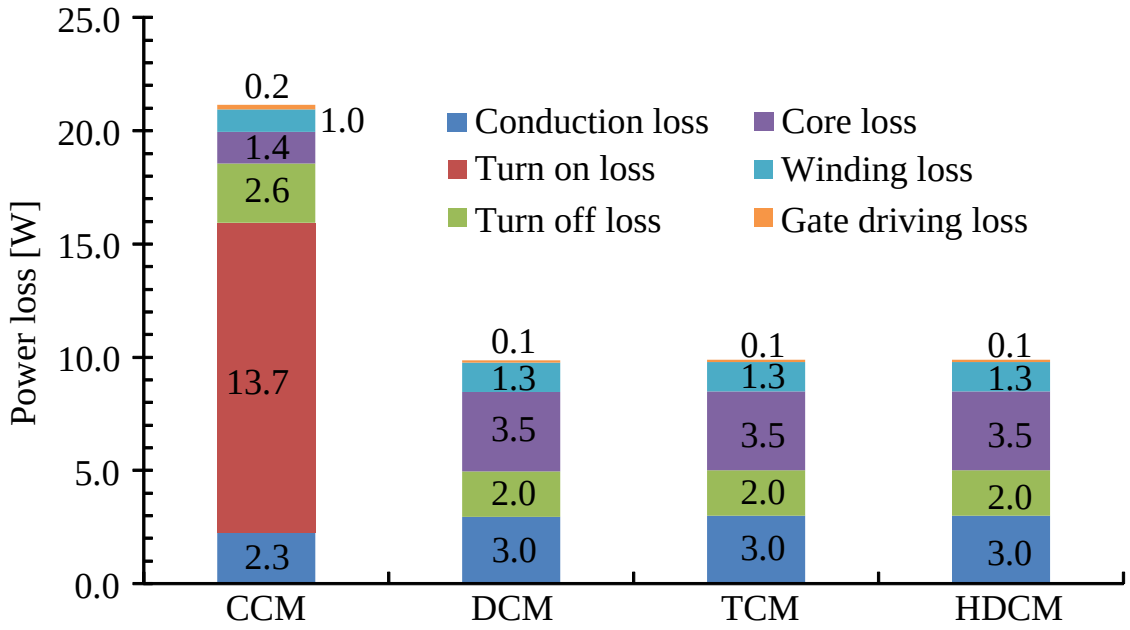
Fig. 6.12. Comparison of RMS current and efficiency among TCM, DCM, HDCM and CCM.

DCM depends on the zero-current interval which changes according to load.

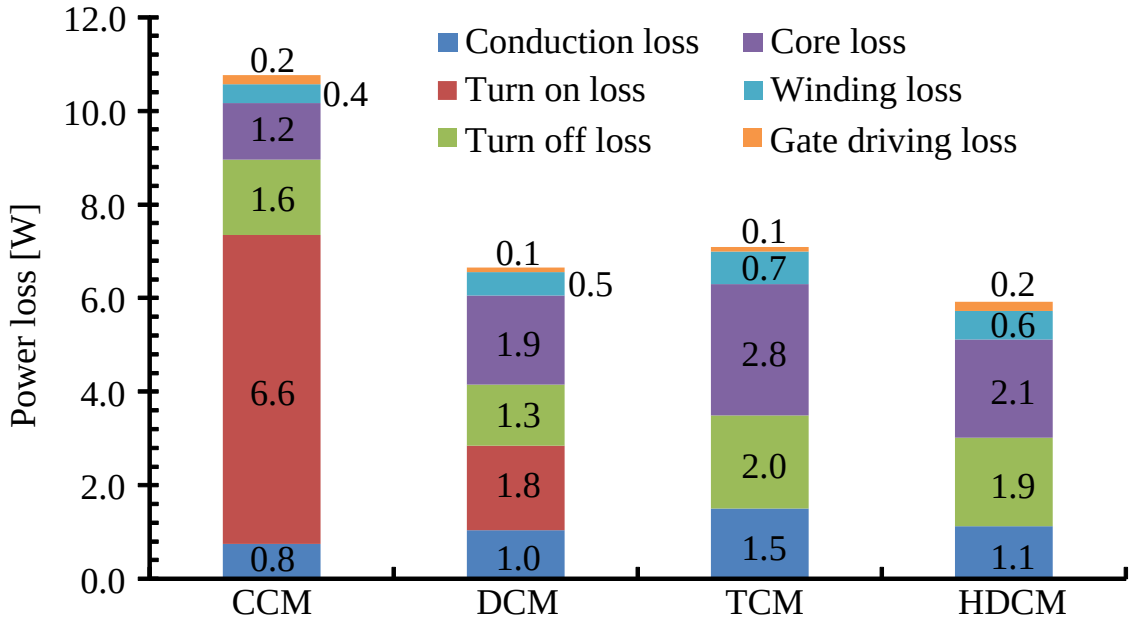
Finally, the efficiency of CCM shows a sharp decline around load of 0.5 p.u.

because the boost converter changes the current mode from TCM to CCM as shown in Fig. 6.10 (b)-(c). By applying HDCM, the efficiency at rated load is improved by 0.9% compared to CCM.

Figure 6.13 shows the loss distribution of four current modes under different conditions of load. The conduction losses and the switching losses are obtained from the simulator, i.e. PLECS, whereas the core losses and the winding losses are obtained from the inductor modeling software entitled GeckoMAGNETICS. As shown in Fig. 6.13(a), the turn-on loss in CCM is dominant and this greatly reduces the efficiency at rated load. The turn-on loss in DCM varies largely depending on the zero-current interval which changes according to load and the other conditions of the circuit such as the input and output voltage. On the other hand, as shown in Fig. 6.13 (c), the high conduction loss and inductor loss still occur in TCM even at light load due to the constant current ripple. The losses from the high current ripple in TCM at light load can be reduced by applying HDCM. This efficiency improvement at light load is specially desired in the photovoltaic system, where the most frequent operating range locates at light load. Note that the increase in the gate driving loss when applying

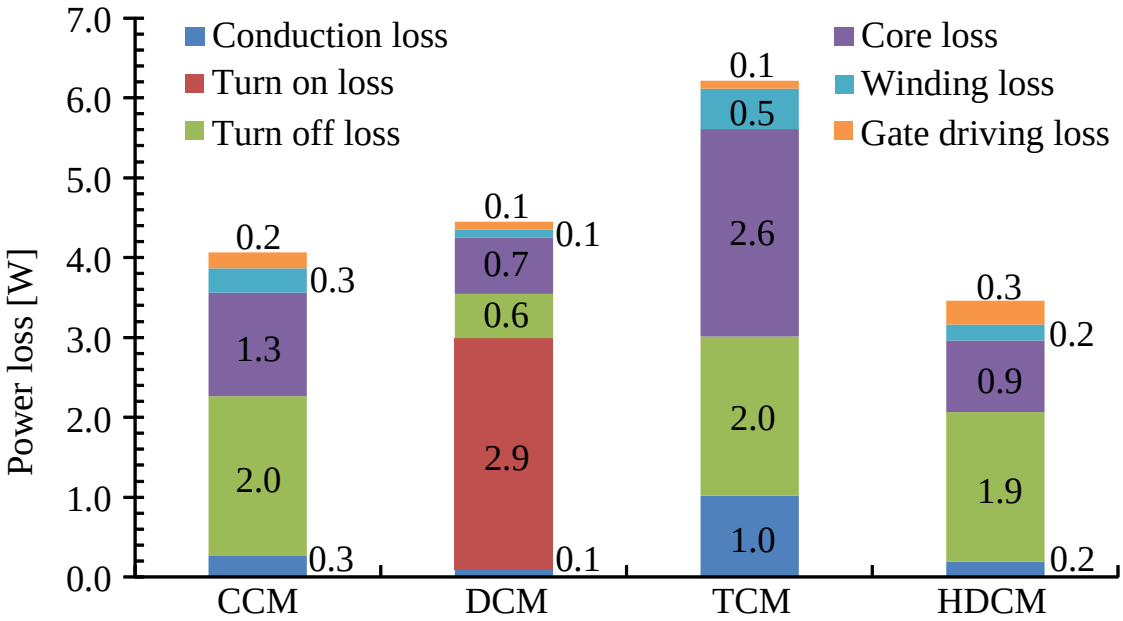



(6.13.a) Loss distribution at rated load




(6.13.b) Loss distribution at load of 0.5 p.u.

HDCM is negligibly small compared to the reduction of the other losses.




(6.13.c) Loss distribution at load of 0.1 p.u.

Fig. 6.13. Loss distribution of four current modes under different conditions of load. In the SiC device, the turn-on switching loss is dominant due to the reverse recovery charge or the junction capacitor charge of the free-wheeling device at hard-switching condition. Therefore, it is crucial to eliminate the turn-on switching loss in order to increase the switching frequency and still maintain the high efficiency.

### 6.4.3 Average Current Ripple Reduction and Output Voltage Regulation

Figure 6.14 describes the theoretical and actual DCM currents. At $t_1$, when both the switches $SW_1$ and $SW_2$ are turned off, the theoretical DCM current remains zero until $t_2$. However, due to the resonance between the boost inductor and the junction capacitors, a current flows during the interval from $t_1$ to $t_2$. At $t_2$, the theoretical DCM current starts to rise from 0A and reaches the current peak $I_{pk1}$ after the turn-on interval $D_1T_{sw}$ of $SW_1$, whereas the actual DCM current reaches the current peak $I_{pk2}$. The difference between $I_{pk1}$ and $I_{pk2}$ results in the average-current ripple $\Delta I_{avg}$. On the other words, the current flowing during $t_1$ and $t_2$ acts as a disturbance to the current regulator. Furthermore, the amplitude of the current flowing during $t_1$ and $t_2$ is inversely proportional to the boost inductor value. This relationship has been researched thoroughly in [6-20]. Consequently, the minimization of the boost inductor in DCM suffers the high average-current ripple. On the other hand, the TCM current in HDCM is controlled in order to let the current return to zero before the next switching period (cf., Section 6.3). Therefore, the average-current ripple

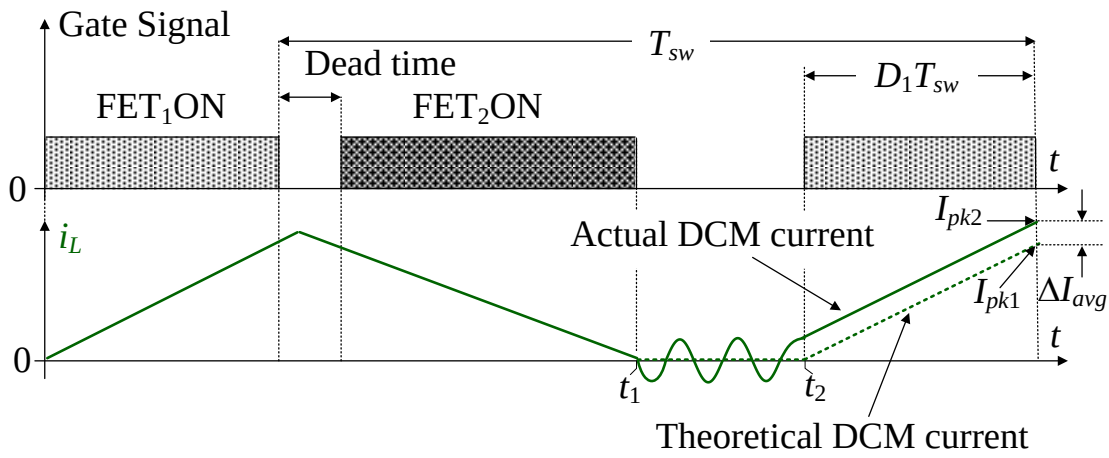
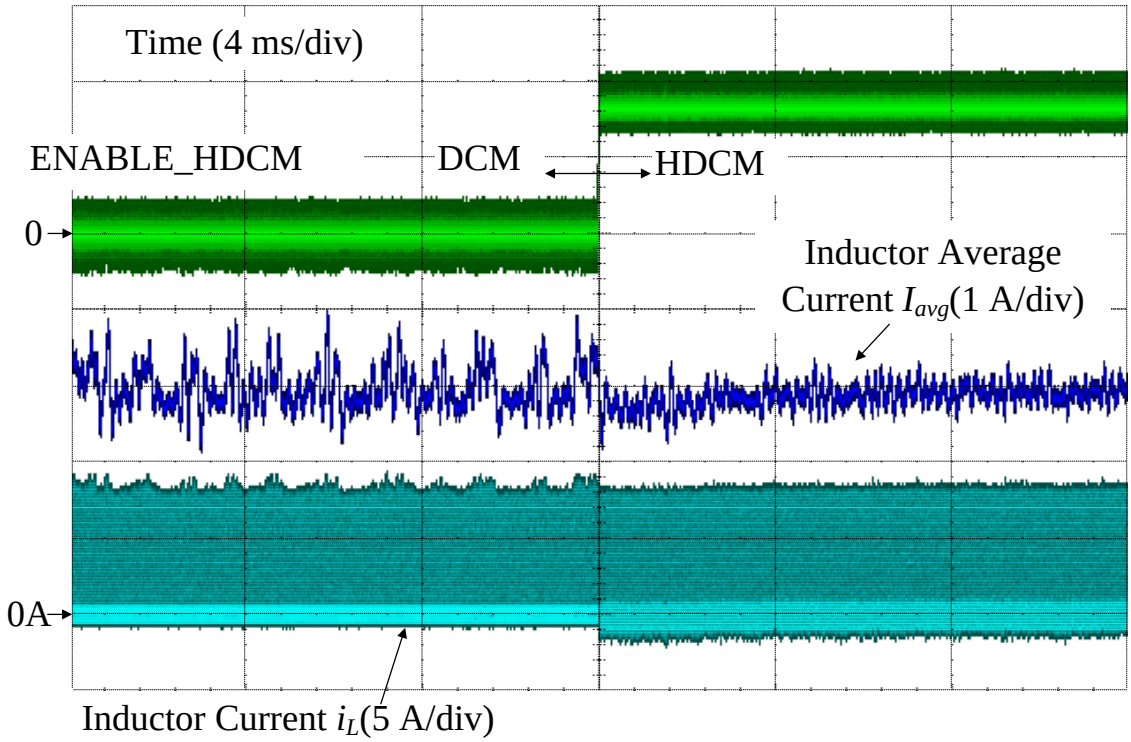



Fig. 6.14. Theoretical and actual DCM currents. Due to the resonance between the boost inductor and the junction capacitors, the high average-current ripple occurs in DCM. Consequently, the minimization of the boost inductor in DCM suffers this high average-current ripple.

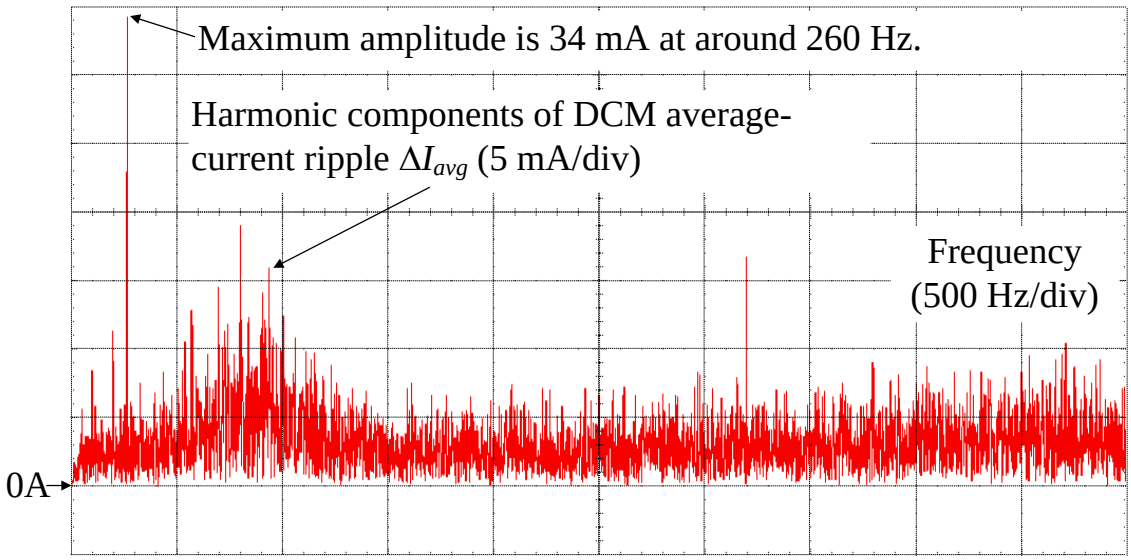
can be reduced by the employment of HDCM.

Figure 6.15 depicts the experimental results of the average-current ripple reduction by applying HDCM. When the signal of ENABLE_HDCM becomes high, the current mode changes from DCM to HDCM. The reduction of the average-current ripple by applying HDCM can be observed from Fig. 6.15(a). Then, the harmonic analysis of the average-current ripple in DCM and HDCM is conducted and the results are shown in Fig. 6.15(b)-(c), respectively. As observed from Fig. 6.15(b), the average-current ripple in DCM consists of many low-frequency harmonic components, one of which has the maximum amplitude of 34 mA around 260 Hz. The average-current ripple in DCM decreases the efficiency of the

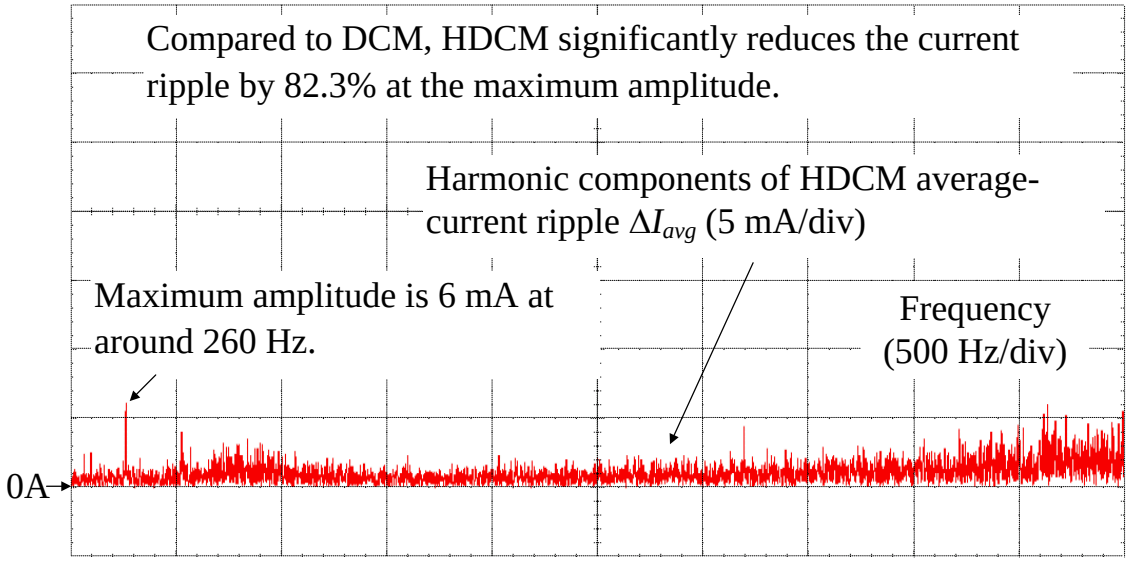
photovoltaic system, because the maximum power point tracking is decayed with this average-current ripple. Furthermore, a large input filter which has a low cut-off frequency is required if the average-current ripple in DCM has to be filtered out, because the harmonic components of the average current ripple in DCM occur in the low frequencies. This problem restricts the minimization of the boost inductor by DCM. The average-current ripple in DCM can also be reduced by damping the resonance between the boost inductor and the junction capacitors. This can




(6.15.a) Average current when the current mode is changed from DCM to HDCM at load of 0.6 p.u.




(6.15.b) Harmonic analysis results of DCM average-current ripple



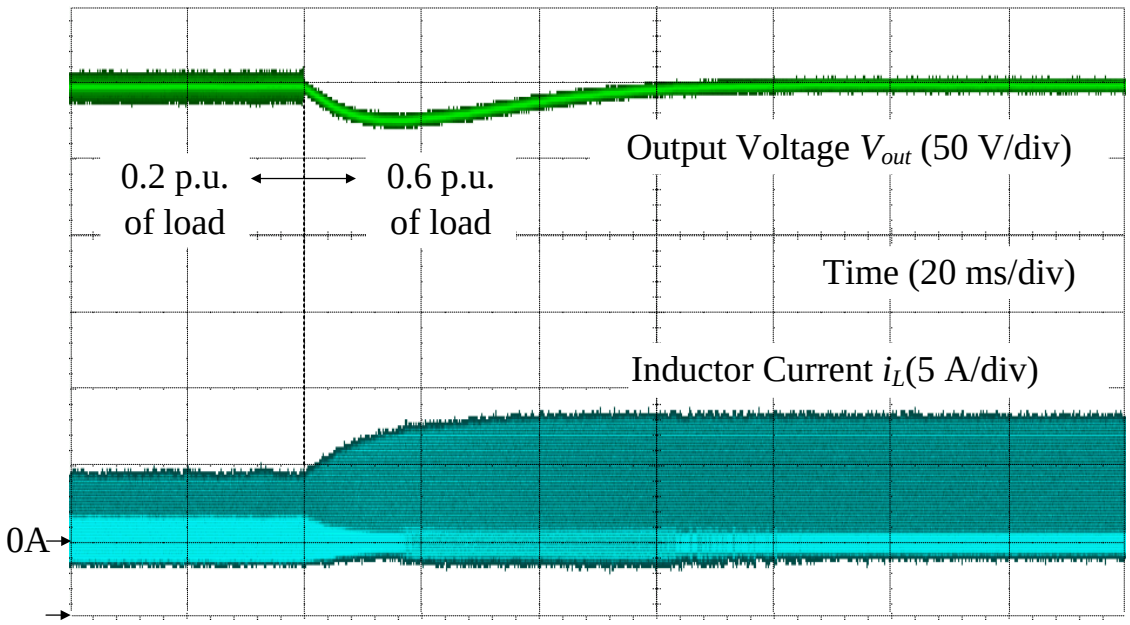

(6.15.c) Harmonic analysis results of HDCM average-current ripple

Fig. 6.15. Average-current ripple reduction by applying HDCM. The high average-current ripple occurring in DCM worsens the maximum power point tracking in the photovoltaic system. By applying HDCM, the average-current ripple can be reduced greatly. This enables the minimization of the boost inductor.

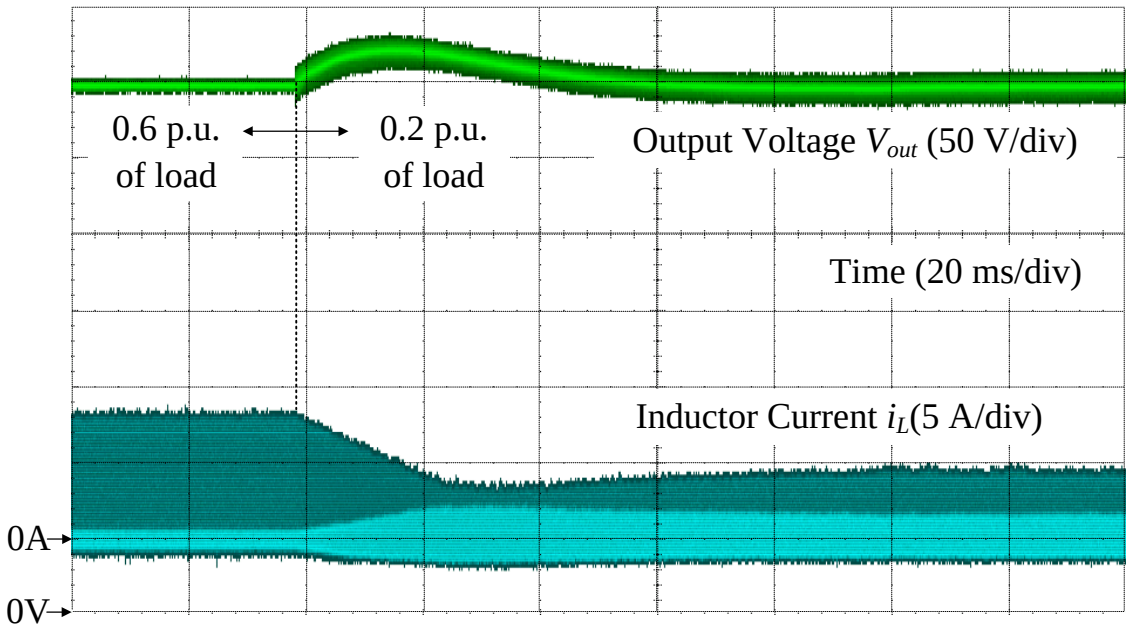
be accomplished by employing a snubber circuit connected parallel to the switching devices. However, the snubber circuit not only increases the

switching loss as shown in Table 6.1 in [6-20], but also restricts the minimization of the boost converter. On the other hand, as observed from Fig. 6.15(c), the harmonic components of the average-current ripple are greatly reduced by applying HDCM. In particular, compared to DCM, the maximum amplitude of the harmonic components is reduced by 82.3%. Note that the small average-current ripple still occurs in HDCM due to the limited resolution of the counter in the FPGA which is generated by a clock frequency of 200 MHz. This causes the TCM current cannot exactly return to zero before the next switching period. This problem can be alleviated by increasing the clock frequency of the FPG6.

Figure 6.16 shows the load transient response obtained in experiment by the output voltage control with 10-Hz cutoff frequency. The test is conducted with a load current step from 0.2 p.u. to 0.6 p.u. and vice vers6. The overshoot voltage and the settling time are 28 V and 56 ms, the errors of which compared to the designed values are 3.6% and 1.8%, respectively. The stability of the voltage control in HDCM is similar to that in DCM because the online calculation of the duty ratios is employed and the TCM current is controlled to have no influence on the DCM operation.




(6.16.a) Load step change: 0.2 p.u. to 0.6 p.u.




(6.16.b) Load step change: 0.6 p.u. to 0.2 p.u.

Fig. 6.16. Load transient response by output voltage control with 10 Hz cutoff frequency. The overshoot voltage and the settling time are 28 V and 56 ms, the errors of which compared to the designed values are 3.6% and 1.8%, respectively [18].

Consequently, this confirms that the real-time closed-loop control of

HDCM can be realized as same as DCM. Furthermore, the duty generation for the TCM interval can be carried out with a margin considering the element tolerances, whereas the feedback control ensures the stable operation of HDCM.

## 6.5 Conclusion

This chapter presented a hybrid current mode between TCM and DCM in order to improve the wide-load-range efficiency for the high-frequency SiC-based boost converter. In the proposed current mode entitled HDCM, ZVS was achieved without any additional components as same as the conventional TCM. Consequently, the high power density design was accomplished by using the SiC devices at high switching frequency. The advantages of HDCM were compared to the other current modes; i.e. TCM, CCM, DCM.

First, in TCM, the constant current ripple decreased significantly the efficiency at light load. Therefore, HDCM in which TCM was applied during the zero-current interval of DCM, was introduced in order to reduce the current ripple and to allow for ZVS over entire switching period. As a result, under the condition of the same boost inductor, the efficiency of HDCM at light load of 0.1 p.u. was improved by 3.1% compared to TCM.

Second, in order to operate the boost converter by CCM under the same condition of the boost inductor, the switching frequency was increased from 100 kHz to 200 kHz. As a result, the inductor current ripple of CCM

at rated load was reduced by half compared to HDCM. In CCM, the hard switching occurred due to the discharge of the reverse recovery charge and the junction capacitor charge. Therefore, the efficiency of CCM at rated load was lower by 0.9% compared to HDCM. Furthermore, the hard switching in CCM not only generated high switching loss but also distorted the gate signal due to the high di/dt of the discharge current from the junction capacitor. The gate signal distortion can lead to the occurrence of the false triggering in CCM. In order to avoid the occurrence of the false triggering during hard switching in CCM, the main circuit and the gate driver circuit are required to be customized for the high di/dt of the current, which is undesirable due to the increase in cost. On the other words, the soft switching in HDCM not only reduced the switching loss but also benefitted the design cost of the main circuit and the gate driver circuit.

Finally, the hard switching in DCM can still occur depending on load. Therefore, the efficiency of HDCM was improved by 1.5% at most compared to DCM. Furthermore, due to the resonance between the boost inductor and the junction capacitors, a current flew during the interval when both the switches are turned off. This current was the reason of the

difference between the theoretical and actual DCM currents, which generated the average-current ripple. The average-current ripple in DCM decreased the efficiency of the photovoltaic system, because the maximum power point tracking was decayed with this average-current ripple. On the other hand, the TCM current in HDCM was controlled in order to let the current return to zero before the next switching period. Therefore, the average-current ripple could be reduced by the employment of HDCM. As a result, compared to DCM, the maximum amplitude of the harmonic components in the HDCM average-current ripple was reduced up to 82.3%.

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# Chapter 7

# Conclusion

## 7.1 Discussion

The power converters play an important role in the sustainable energy systems such as, e.g. wind turbine systems or solar power systems, acting as an interface between the power source to the energy storage system, or the grid. These are important technologies to effectively slow down the growth of $CO_2$ emission and reduce the climate change effects.

The motivation of this thesis is to develop power converters features high power density and high efficiency, for the applications of the solar power systems. Chapter 2 reviews the state of arts of the current control for CCM and DCM, and propose the novel control method. The DCM operation inevitable occurs at light load in the unidirectional power

converter, or in the vicinity of the zero-current-crossing points in the bidirectional power converter. In order to control the DCM operation, numerous studies have been focused on the zero-current-interval detection and the DCM nonlinearity compensation. However, these studies show that the zero-current-interval detection is difficult to implement in practical applications, requiring many efforts to accurately tune the thresh-hold value of the zero-current-interval detection, because the resonance between the inductor and the parasitic capacitance occurs during the zero-current interval. Therefore, the current mode determination based on the relationship of the CCM and DCM duties has received great amount of attentions. This method can avoid the use of the zero-current-interval detection; nevertheless, the DCM duty generation becomes dependent on the inductance. The inductance-dependent characteristic is undesired in the power converter used in the solar power systems, where the accurate inductance is difficult to obtain.

Chapter 3 describes the proposed DCM control for the boost converter as an example for DC-DC converters. The proposed DCM control is constructed based on the CCM control with the PI controller. In order to

employ the same PI controller designed in the CCM control, the DCM nonlinearity compensation is the duty value. In the conventional DCM nonlinearity compensation, the duty value is calculated with the use of the inductance, resulting the inductance-dependent DCM duty generation. On the other hand, in the proposed DCM nonlinearity compensation, the duty value is estimated with the use of the duty value at the previous calculation period, eliminating the inductance-dependence characteristic in the DCM duty generation. Chapter 3 demonstrates the comparison of the step current response between the CCM control and the proposed DCM control under conditions of the same PI controller. The experimental results have confirmed the validity of the proposed DCM control, including (i) showing the same DCM current response as in CCM, and (ii) employing the DCM synchronous switching as in CCM. Furthermore, the efficiency comparison also demonstrates that the employment of the DCM operation can reduce the converter loss at light load compared to the CCM operation.

Chapter 4 describes the proposed CCM/DCM control for the single-phase grid-tied inverter as an example for single phase DC-AC or AC-DC converters. The proposed CCM/DCM control uses the similar

DCM nonlinearity compensation in Chapter 3, with the addition of the CCM/DCM current mode determination. In the conventional CCM/DCM current mode determination, the difficult-to-reproduce tuning for the zero-current interval detection is employed; otherwise, the inductance is involved in the current mode determination. The proposed CCM/DCM current mode determination avoids the above problems by using the relationship between the CCM and DCM duties to determine the current mode. In the proposed CCM/DCM control, both the CCM and DCM duty generations are independent from the inductance, resulting in the inductance-independent CCM/DCM current mode determination. Chapter 4 demonstrates the comparison of the grid-tied mode operation between the CCM control and the proposed CCM/DCM control under conditions of the same PI controller. The experimental results have confirmed the validity of the proposed CCM/DCM control by showing the current THD improvement compared to the CCM control.

Chapter 5 discuss the proposed DCM control for the three-phase grid-tied inverter as an example for three-phase DC-AC or AC-DC converters. In the conventional DCM control for the three-phase DC-AC

converters, the currents in each phase interfere the current control in the other phases, resulting in the complicated DCM control. In the proposed DCM control, the generation of each current phase is split into 2 different intervals, avoiding the current interference. Therefore, the current control becomes simple and the DCM control in Chapter 3 can be applied. The experimental results confirm the operation of the proposed DCM control for the three-phase grid-tied inverter, including (i) the individual current generation in each intervals, and (ii) the sinusoidal current forming.

Chapter 6 demonstrates the implementation of the hybrid DCM. In the previous chapters, the DCM operation with the hard switching at the turn-on is employed. Note that the DCM operation starts at the zero current, resulting in the zero current switching (ZCS); nevertheless, the discharge of the parasitic capacitance still causes a high switching loss at the turn-on. This high turn-on switching loss prevents the increase in the switching frequency, i.e. the minimization of the inductor. Therefore, the hybrid current mode between DCM and TCM is proposed to achieve ZVS. This chapter has confirmed the effectiveness of the proposed hybrid DCM by comparing the efficiencies among CCM, DCM, TCM and hybrid DCM.

Overall, this thesis proposes the inductance-independent CCM&DCM control in order to achieve both the high power density and high efficiency for the boost converter and grid-tied inverter used in the solar power system. Due to the employment of the proposed control method, the minimization of the inductors which cause the large size and low efficiency of the system is achieved without any new controller design. In the experiments with the boost converter, the highest efficiency of 98.7% is achieved, whereas the loss at the light load is reduced by 60.9% at most. In the experiments with the grid-tied inverter, the grid current THD is maintained below 5% even when the inductor impendence is just 0.5% of the total inverter impendence. Moreover, the interconnecting inductor volume is reduced by 51% compared to that in the conventional CCM control. Consequently, the effectiveness of the proposed control method on the improvement of the power density and efficiency is confirmed through these experimental results.

## 7.2 Future Works

This thesis has demonstrated that the proposed CCM/DCM control is capable of achieving the high power density for the DC-DC, DC-AC and AC-DC converters, and still maintaining the high efficiency and the high current control performance. However, the proposed CCM/DCM control is still required further research to achieve high-volume practical production.

### 7.2.1 Island Mode Operation

The proposed CCM/DCM control is capable to achieve the sinusoidal current forming with low current THD for both the single-phase and three-phase grid-tied inverter. However, the island mode operation is also a requirement for such inverters. In the island mode operation, the grid-tied inverter needs to regulate the load voltage regardless of the load characteristic, i.e. the achievement of the sinusoidal voltage regulation even with the nonlinear or low-power-factor load. Especially with the nonlinear load such as, e.g. the rectifier load with high crest factor, the current becomes non-sinusoidal. Due to the above reasons, one of the future work is to analyze the island mode operation of the proposed CCM/DCM control. Then, the results are compared with the conventional CCM control that has

the similar controller to evaluate the effectiveness of the proposed CCM/DCM control in island mode operation. In particular, the comparison of the load voltage THD should be addressed.

### 7.2.2 CCM/DCM Feedback Current Control for Three-phase Converters

The issues of the proposed DCM control for the three-phase grid-tied inverters have been mention in Chapter 5. One of the issue is the control performance in the DCM feedforward current control. The inductance-dependence characteristic still occurs in the feedforward current control, preventing the high-volume practical production. In order to solve this problem, the CCM/DCM feedback current control needs to apply to control the three-phase converters. The basic idea might be similar to the proposed CCM/DCM feedback current control in Chapter 2; in particular, the duty value at the previous calculation period might be utilized to compensate for the DCM nonlinear factors of the DCM operation in the three-phase converters.

# List of Achievements

## Publication Journals

[1] Hoai Nam Le, Koji Orikawa and Jun-ichi Itoh, "Circuit-Parameter-Independent Nonlinearity Compensation for Boost Converter Operated in Discontinuous Current Mode," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 2, pp. 1157-1166, Feb. 2017.

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