The PWM Strategy based on Load Current Sector for DC-link Capacitor Current Stress Reduction in Three-phase AC Motor Drive System

by

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Table of Contents

List of Figures

Chapter 3

Chapter 4

Chapter 5

Chapter 6

List of Tables

Chapter 5

Chapter 6

Chapter 7

Chapter 1

Introduction

1.1 Background

Thanks to the progress of power electronics technologies, variable speed alternate current (AC) motor drive system has been developed. This system provides a lot of engineering benefits as follows compared to the other systems to obtain the mechanical force such as the internal combustion engines and the hydraulic actuators [1-1]:

- More downsizing and more packaging,
- More precise control for the torque and the speed,
- Higher availability and higher maintenability,
- Energy saving,
- Load leveling with the energy storage systems.

Fig. 1.1 shows the global electricity consumption ratio by end-use in 2014 based on the International Energy Agency (IEA) estimation [1-2]. The IEA estimated that 53% of global electricity, or 10700 TWh per year, was consumed by electric motor systems. This fact indicates that the AC motor drive systems play big role as an essential component in the emerging applications to save the energy. Moreover, for more practical use, not only its energy-efficient but also its reliability and size should be improved.

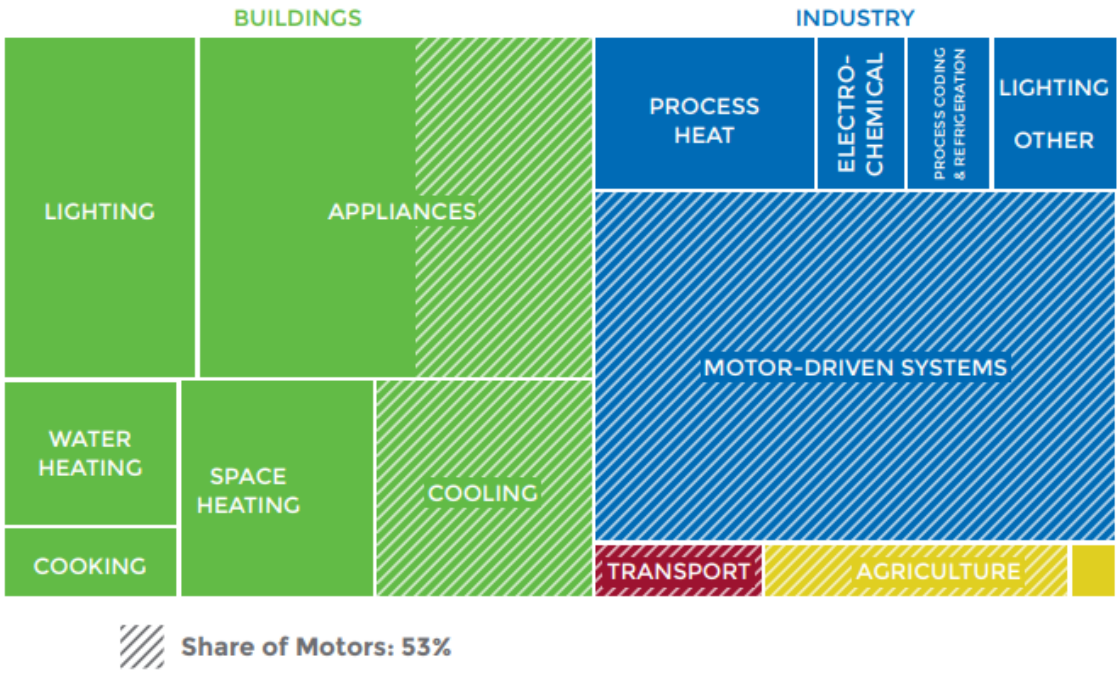
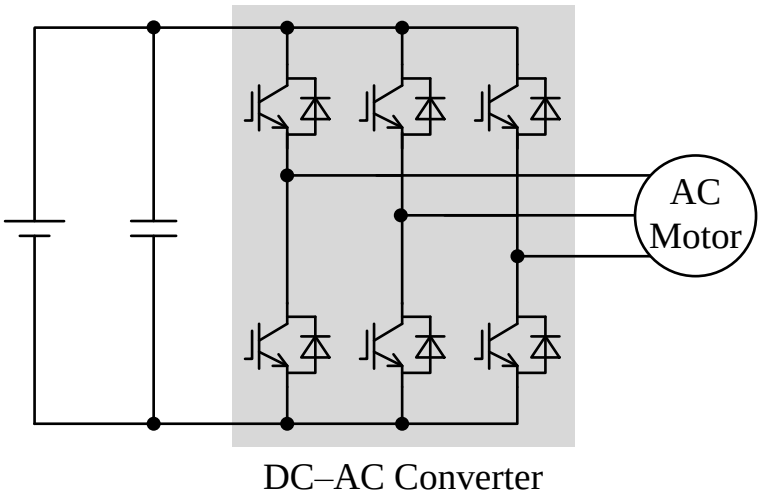
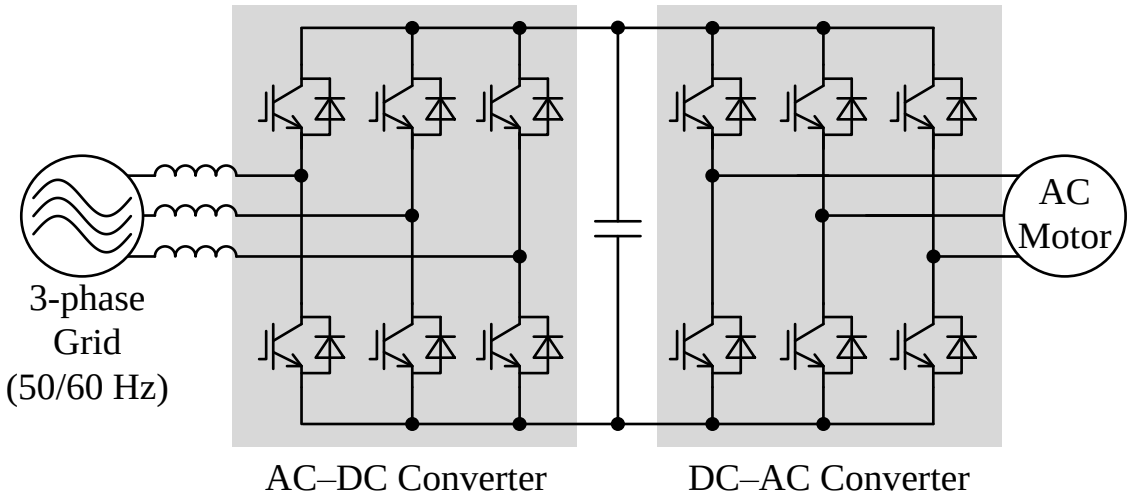


Fig. 1.1. Global electricity consumption ratio by end-use in 2014.
(Adapted from [1-2] United Nations Environment Programme, *Accelerating the Global Adoption of Energy-Efficient Electric Motors and Motor Systems–U4E Policy Guide Series*. 2017.)

Fig. 1.2 shows the classic configurations of the variable speed AC motor drive systems. Of all the modern power electronics converters, the two-level voltage source inverter (VSI), shown in Fig. 1.2, is one of the most widely used converter with power ratings ranging from several hundred watts to megawatt. The two-level VSI consists of six power semiconductor switches with anti-parallel freewheeling diodes. In the variable speed AC motor drive systems, VSI drives AC motor by converting a direct current (DC) voltage to 3ϕ/AC voltage with variable frequency and magnitude. The fixed DC voltage source can be DC power supply such as lithium-ion battery, shown in Fig. 1.2(a). As shown in Fig. 1.2(b), the fixed DC voltage can be also generated by converting three phase grid AC voltages with the 3ϕ/AC–DC converter, of which configuration is same as the DC–3ϕ/AC VSI [1-3]. This system is called as back-to-back (BTB) system due to the fact that two same



(a) Battery embedded system.



(b) Back-to-back (BTB) system.

Fig. 1.2. Classic configurations of AC motor drive systems.

circuits are back to back. Both of configurations have the capacitors in DC stage; the capacitors are defined as dc-link capacitors hereafter.

For power electronics systems based on dc-link voltage, the dc-link capacitors contribute significantly to the converter volume and hence influence the power density of the total system. Maximization of the converter's power density has to focus on dc-link optimization. The tasks of the dc-link capacitors are [1-4]:

1. to “absorb” the high-frequency switching component of the 3ϕ/AC–DC converter’s output current and/or to “compensate” the high-frequency switching component of the DC–3ϕ/AC converter’s input current,
2. to minimize the voltage variation in the dc-link,
3. to serve as an energy storage to provide hold-up and/or to absorb a power injection from the load.

Hence, the selection of the dc-link capacitor must consider its rated current as well as the required storage capacitance. Their size is typically one of drawback for high power density in highly integrated systems such as in automobile industry.

Fig. 1.3 shows the capacitor life estimation table from manufacturer’s technical note [1-5]. For the electrolytic capacitors, wear out issue due to the

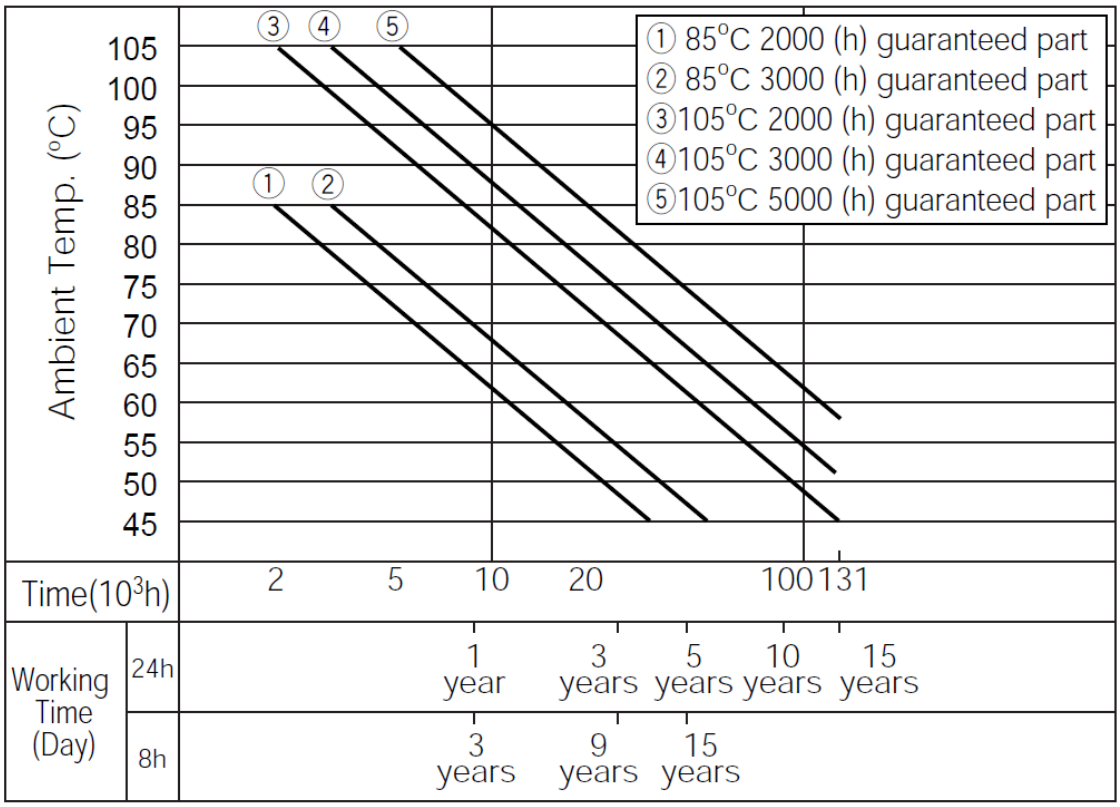


Fig. 1.3. Capacitor lifetime estimation table.
(Adapted from [1-5] Nichicon Corp., Tokyo, Japan. *Technical Notes on Aluminum Electrolytic Capacitors*, Cat. 8101E-1.)

evaporation of the electrolyte is closely related to the capacitor temperature. These lifetimes are approximately reduced by half if the capacitor core temperature increases by 10℃, according to the *Arrhenius equation*. In addition to its volume issue described in above paragraph, the dc-link capacitors might also lead to the reliability bottleneck of the electronic systems.

Table 1.1 and 1.2 list the typical rated temperatures of main components in AC motor drive systems. So far, there are mainly three types of capacitors which are available for dc-link applications. The property of dielectric materials is a major factor that limits not only the performance of capacitors but also the maximum operating temperatures, which are typically lower than those of semiconductors. The ceramic capacitors operate up to 200℃ and might remove the dc-link capacitor operating temperature bottleneck. However, they suffer from higher cost and mechanical sensitivity such as cracking due to vibration which is frequently occurs in traction applications. Therefore, the dc-link capacitors lead to constraints on thermal dissipation with the trends for high power density electronic systems [1-19].

TABLE 1.1.
MAXIMUM OPERATING TEMPERATURES OF CAPACITORS FOR DC-LINK APPLICATIONS.

Electrolytic Capacitor [1-6]–[1-7]	Film (PP) Capacitor [1-8]–[1-9]	Ceramic Capacitor [1-10]–[1-11]
85–105℃	85–105℃	150–200℃

TABLE 1.2.
MAXIMUM STORAGE TEMPERATURES OF SEMICONDUCTORS.

IGBT [1-12]–[1-13]	Si-MOSFET [1-14]–[1-15]	SiC MOSFET [1-16]–[1-17]	GaN-HEMT [1-18]
125–175℃	150–175℃	150–175℃	150℃

Since the dc-link capacitors might be the lifetime bottleneck and the barrier for high power density, some approaches to extend its lifetime or reduce the capacitor size have been studied.

In order to extend the dc-link capacitor reliability, the control methods to achieve dc-capacitor-less or not to require bulky electrolytic capacitors for the cascaded power conversion systems (1ϕ/AC–DC–3ϕ/AC) have been proposed [1-20]–[1-28]. Due to the remarkably decreased capacity of the dc-link capacitor, it is difficult to maintain dc-link voltage constant. As a result, the dc-link voltage fluctuates with the single-phase grid voltage. In these approaches, the single-phase power ripple, which is not compensated by the bulky electrolytic capacitors, is sent to the motor side as a torque ripple and is absorbed into the moment of inertia. Therefore, these approaches cause motor speed variations, resulting in the limited applications for compressor motor drives that do not require a speed response with high precision.

As another approaches for the cascaded DC–DC–3ϕ/AC power converters, new concepts of coupling the two modulations for DC–DC stage and DC–3ϕ/AC stage to minimize the energy storage at the dc-link have been proposed [1-29]–[1-30]. However, with the considerations of the ride-through during power outage or fault conditions, the applications of these approaches are also limited.

On the other hand, the pulse width modulation (PWM) strategies to reduce the switching-frequency current harmonics on the dc-link capacitors have been also proposed [1-31]–[1-34]. In the widely utilized PWM methods, the inverter output voltage approximates the reference value through high frequency switching. So, those approaches improve the current harmonics on the dc-link capacitor without the limitations of application. However, those approaches are able to reduce the dc-link capacitor current harmonics only when the load power factor, the ratio of the real power absorbed by the motor load to the apparent power flowing in the inverter, is higher than 0.8. This might be a big barrier to apply to the variable speed AC motor drive systems, of which the variation of the load power factor is considerably wide.

1.2 Research Objectives

The objective of this research is to reduce the dc-link capacitor current stress over wide range of load power factor. The dc-link capacitor current stress reduction is accomplished by modifying the PWM switching patterns. Consequently, the AC motor drive systems benefit in term of reliability and size.

First of all, the optimization method for the PWM switching patterns to minimize the dc-link capacitor current stress is studied. As previously mentioned, any cases of the load power factor conditions should be considered to apply to the AC motor drive systems. So, this paper introduces new concept of “load current sector” to the optimization process for the PWM switching patterns. For balanced three-phase load, the combination of three-phase load currents’ directions switches every 60° of phase angle. These 60° periods are defined as the load current sectors. This optimization method is firstly based on the space vector PWM (SVPWM) strategy because its flexibility to modify the switching patterns provides the optimized results. However, the application of the SVPWM leads to a constraint of the digital hardware and the necessity of a high cost hardware such as field-programmable gate arrays (FPGA), which is not typically used in the electric vehicle applications where the high power density is highly desired. Furthermore, the optimized SVPWM strategy results in a trade-off between the improved capacitor current harmonics and the worsened AC motor current harmonics.

Then, the other strategies based on the carrier-based PWM to reduce the dc-link capacitor current stress by using the load current sector are also studied. The same optimization concept for the SVPWM to reduce the dc-link capacitor current stress reduction is also achievable only with the general-purpose micro-computer, which is used in the electric vehicle applications. Those approaches generate the modified switching patterns by comparing the continuous or discontinuous modulating signals with the high-frequency triangular carrier. Furthermore, the carrier-based PWM

approaches obtain the intermediate performances on the dc-link capacitor current stress and the AC motor current harmonics between the conventional PWM strategies and the space vector-based PWM approaches.

Finally, the application of the dc-link capacitor current harmonics reduction PWM to the 3-level three-phase DC–AC power converters is considered. The AC motor drive systems reach not only low voltage applications but also medium-voltage high-power applications. The dc-link capacitor current harmonics reduction for the 3-level VSI, which has higher voltage capacity than the 2-level VSI, might lead to possibility of the high reliability and high power density AC motor drive systems.

1.3 Thesis Organization

Fig. 1.4 shows the outline of this thesis divided into 7 chapters.

Chapter 1 introduces the AC motor drive system composition and its reliability issue due to the heat-sensitivity of the dc-link capacitor. Next, some approaches to extend the dc-link capacitor reliability are introduced. Then, the objectives to reduce the dc-link capacitor current stress over wide range of load power factor are demonstrated.

Chapter 2 introduces the classical PWM strategies which is a key technology to discuss the dc-link capacitor current stress. Next, dc-link capacitor current analysis is performed based on these classical PWM strategies. Then, the state of arts of current approaches to extend the dc-link capacitor reliability and those problems to apply to the AC motor drive system are reviewed. Finally, the proposed PWM strategies using the load current sector, which is the key concept of this thesis, are described and the beneficial position of the proposed approaches along with other conventional approaches is presented.

Chapter 3 discusses the proposed optimization method for the PWM switching patterns to reduce the dc-link capacitor current stress with the consideration of the load power factor variation. First, the methods for reduction of dc-link current harmonics are explained based on the voltage space vector concept. Next, the method how to adapt to the variations of the load power factor using the load current sector is presented. Finally, the comparisons of the dc-link current harmonics and the dc-link capacitor heating are demonstrated in order to verify the effectiveness of the proposed SVPWM.

Chapter 4 discusses the proposed carrier-based continuous PWM strategy to reduce the dc-link capacitor current stress, which is achievable with the more practical digital hardware; micro-computer. First, the adjustment method for the gate pulse timings through the use of signal-updated-timings of the micro-computer is explained. Next, the reduction method for the dc-link current harmonics with the shifted modulating signals

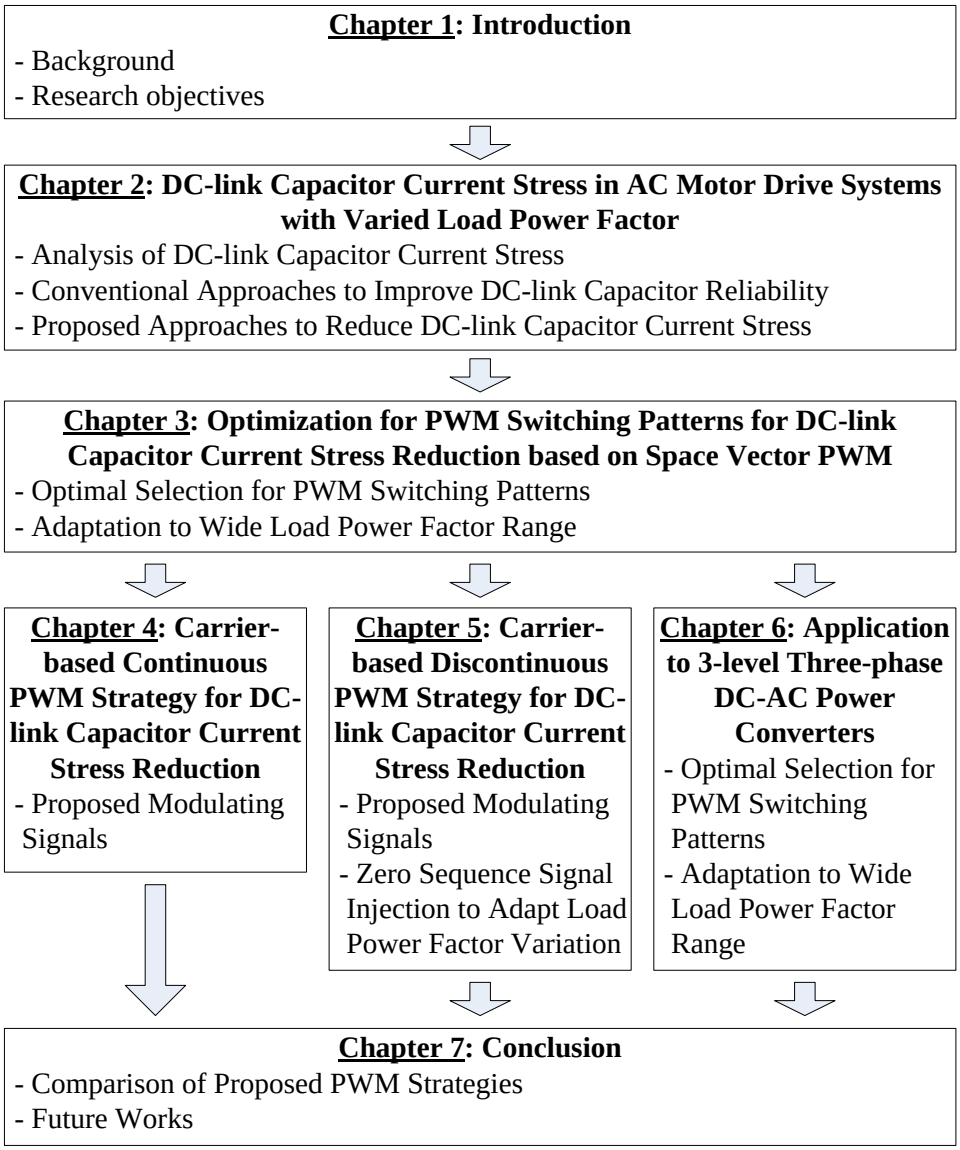


Fig. 1.4. Outline of this thesis.

is proposed. Finally, the effectiveness of the proposed CPWM is verified.

Chapter 5 discusses the proposed carrier-based discontinuous PWM strategy to reduce the dc-link capacitor current stress, which conquer the limited voltage transfer ratio which is big disadvantage of the proposed CPWM. First, the reduction method of the dc-link current harmonics by using the shifting modulating signals and injecting the proper zero-sequence signal are explained. Finally, the effectiveness of the proposed DPWM is verified.

Chapter 6 discusses the new SVPWM strategy for the three-level VSI using the proposed optimization method of the PWM switching patterns for the current harmonic reduction of the dc-link capacitors. The original idea proposed in chapter 3 has been applied to the three-level VSI in this chapter. First, the optimized selection method for the voltage space vectors with the considerations of the dc-link current harmonics and the load current quality is presented. Finally, the operation of the proposed three-level SVPWM is experimentally verified.

Chapter 7 provides the conclusion of this thesis. In this chapter, the advantages and drawbacks of the proposed PWM strategies are classified clearly and compared alongside each other. The present works are summarized and future works which should be carried out will be discussed.

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Chapter 2

DC-link Capacitor Current Stress in AC Motor Drive Systems with Varied Load Power Factor

2.1 Introduction

The previous chapter described the importance of the dc-link capacitors for the AC motor drive systems. The reduction of dc-link capacitor current stress contributes to high system reliability and high power density.

In this chapter, first, the dc-link capacitor current harmonics and its reliability in the AC motor drive system is explained and analyzed in detail with the introductions of the classical PWM strategies of DC–3ϕ/AC power converters. Next, the capacitor types and characteristics for dc-link applications are reviewed. Then, the state-of-the-art approaches to improve the reliability of the dc-link capacitors are reviewed and discussed. Those contain the circuit configuration-dependent and the PWM-dependent approaches. After that, a comparison chart is provided to discuss about the most applicable approaches to improve the reliability of the dc-link capacitors in the AC motor drive systems.

Finally, the proposed PWM strategies is described in detail. The beneficial position of the proposed approaches along with other conventional approaches is presented to show the contribution of this research.

2.2 Classical PWM Strategies of Three-phase DC-AC Power Converters

2.2.1 Space Vector PWM

Fig. 2.1 shows the configuration of two-level three-phase DC-AC VSI employed in the AC motor drive system. The two-level three-phase VSI consists of three half-bridge converters. If the semiconductor switching devices such as insulated gate bipolar transistors (IGBTs) are treated as ideal switches, then the conduction status of any one half-bridge converter are represented by the following binary switching functions

$$s_x(t)=\begin{cases}1, & \left(S_{xp}:\text{ON}, \quad S_{xn}:\text{OFF}\right)\\ 0, & \left(S_{xp}:\text{OFF}, \quad S_{xn}:\text{ON}\right)\end{cases}, \quad (x=u,v,w). \ldots\ldots\ldots\ldots\ldots (2.1)$$

Fig. 2.2 shows the waveforms of the three-phase voltage references and the output phase currents at a modulation index of 0.7 and the load power factor of 0.866 (30° lagging). The three-phase voltage references are considered as the sinusoidal waveforms and expressed as

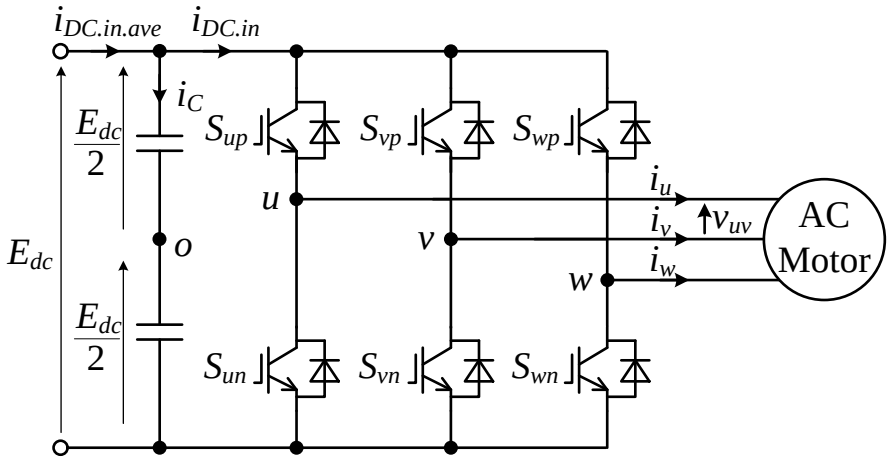


Fig. 2.1. Two-level three-phase VSI.

$$\begin{cases} v_u^*(t) = m \cdot \cos(2\pi ft) \\ v_v^*(t) = m \cdot \cos(2\pi ft - 2\pi/3) \\ v_w^*(t) = m \cdot \cos(2\pi ft + 2\pi/3) \end{cases} \quad \text{.....(2.2)}$$

where m is the modulation index and f is the fundamental frequency. Similarly, the output phase currents of the VSI at steady-state operating condition are expressed as

$$\begin{cases} i_u(t) = I_m \cdot \cos(2\pi ft - \varphi) \\ i_v(t) = I_m \cdot \cos(2\pi ft - 2\pi/3 - \varphi) \\ i_w(t) = I_m \cdot \cos(2\pi ft + 2\pi/3 - \varphi) \end{cases} \quad \text{.....(2.3)}$$

where I_m is the amplitude of the output phase current and φ is the load power factor angle, i.e., the phase shift between the phase current and phase voltage.

Fig. 2.3 shows the available output voltage space vectors of the two-level three-phase VSI in the $\alpha\beta$ reference frame. The α-axis and β-axis available voltages of VSI are calculated from the switching functions on the basis of the *Clarke transform* as

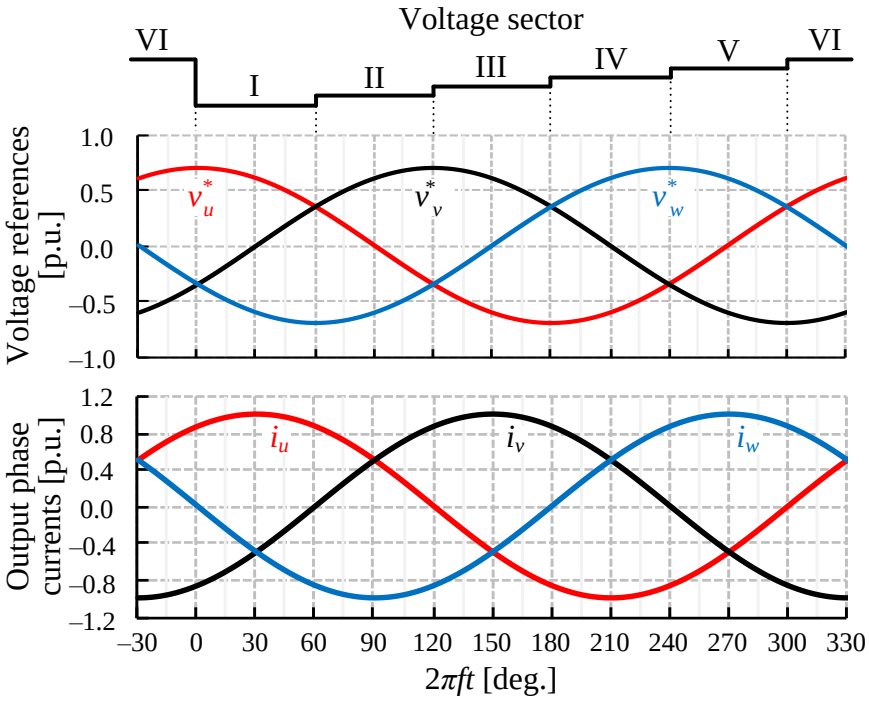


Fig. 2.2. Voltage references v^*_x and output phase currents i_x at m = 0.7 and cos φ = 0.866 (30° lagging).

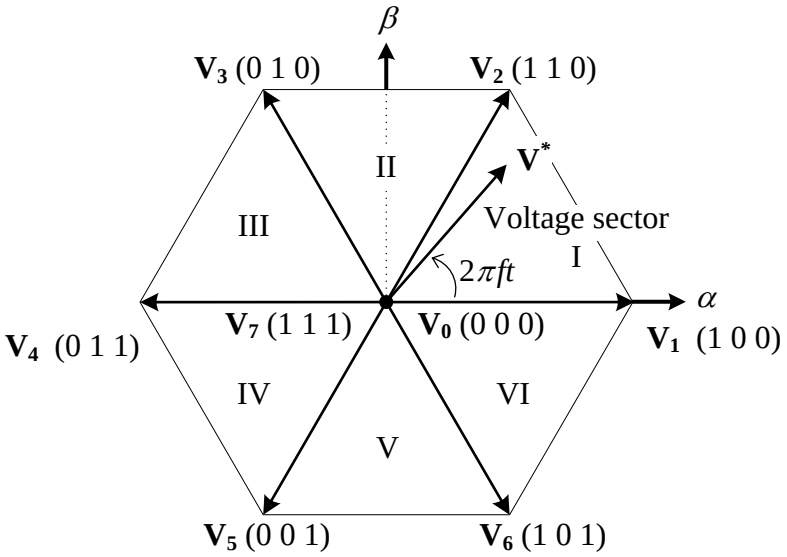


Fig. 2.3. Available output voltage space vectors of two-level three-phase VSI in $\alpha\beta$ reference frame.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} s_u(t) & \overline{s}_u(t) \\ s_v(t) & \overline{s}_v(t) \\ s_w(t) & \overline{s}_w(t) \end{bmatrix}\begin{bmatrix} \frac{1}{2}E_{dc} \\ -\frac{1}{2}E_{dc} \end{bmatrix} \quad \text{.....(2.4)}$$

The switching functions of each phase become only two different values; therefore, there are 8 (= 2^3) output voltage space vectors of the VSI expressed using the switching functions as $\mathbf{V}$ ($s_u(t)$, $s_v(t)$, $s_w(t)$). Six of these ($\mathbf{V_1}$–$\mathbf{V_6}$) are the active vectors and the others ($\mathbf{V_0}$, $\mathbf{V_7}$) are the zero vectors.

The α-axis and β-axis voltages references are also calculated from the three-phase voltage references on the basis of the *Clarke transform* as

$$\begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_u^* \\ v_v^* \\ v_w^* \end{bmatrix}. \quad \text{.....(2.5)}$$

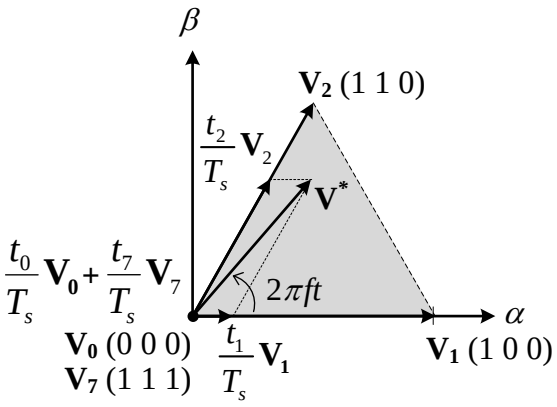
In the SVPWM, the voltage reference vector $\mathbf{V}^*$ sampled in each control period T_s (= $1/f_{sw}$), typically an inverse of the switching frequency f_{sw}, is generated by synthesizing the three voltage space vectors $\mathbf{V_a}$, $\mathbf{V_b}$, and $\mathbf{V_c}$

upon the volt-second balance principle as

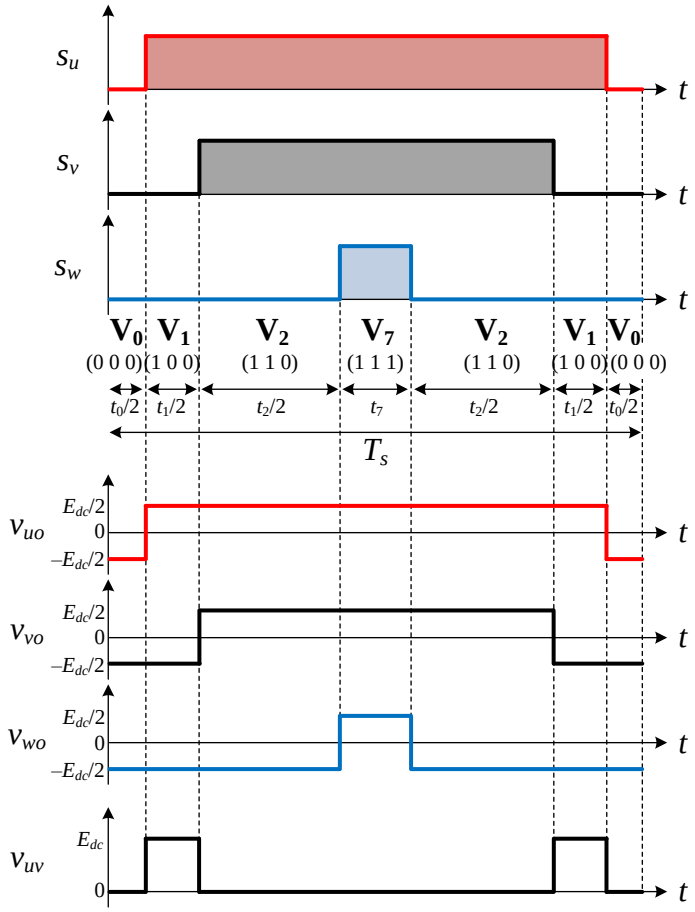
$$\mathbf{V}^* = \frac{t_a}{T_s}\mathbf{V_a} + \frac{t_b}{T_s}\mathbf{V_b} + \frac{t_c}{T_s}\mathbf{V_c} \quad \text{.....(2.6)}$$
$$T_s = t_a + t_b + t_c$$

where t_a – t_c are the duty cycles of each selected voltage space vector and a – c represent the number of selected voltage space vectors, as defined in Fig. 2.3.

Fig. 2.4 shows the conventional two-level SVPWM strategy. The output phase current harmonics are caused by the difference between the applied voltage space vector and the voltage reference vector $\mathbf{V}_x - \mathbf{V}^*$ (x = 0 – 7). So, in the conventional SVPWM strategies [2-1]–[2-7], three voltage space vectors which are the nearest to the voltage reference vector are used to minimize the output phase current harmonics. In the example shown in Fig. 2.4, the voltage reference vector is generated using two adjacent active vectors of $\mathbf{V_1}$ and $\mathbf{V_2}$ and the zero vectors $\mathbf{V_0}$ and $\mathbf{V_7}$ at each control period when the voltage reference vector is located in the voltage sector of I. Generally, the duty cycles of the zero vectors are equally partitioned as $t_0 = t_7$. The voltage space vectors are symmetrically allocated in each control period as $\mathbf{V_0}$–$\mathbf{V_1}$–$\mathbf{V_2}$–$\mathbf{V_7}$–$\mathbf{V_2}$–$\mathbf{V_1}$–$\mathbf{V_0}$ with the minimum total switching transitions in this example. In practical, any vector allocations and divisions of the duty cycles are implemented by the design of the digital hardware such as field-programmable gate array (FPGA).



(a) Voltage space vector synthesizing.



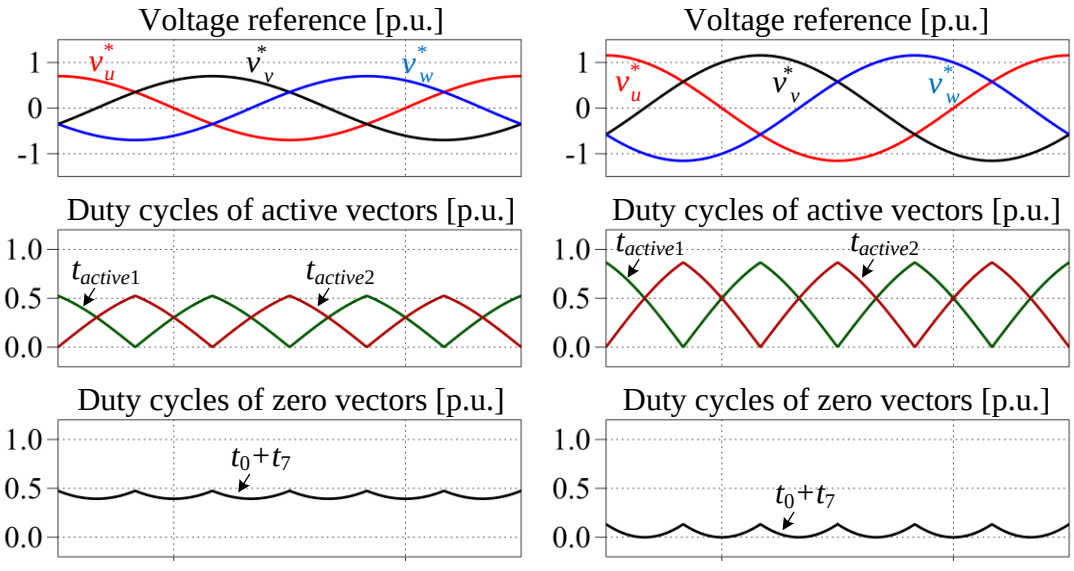
(b) Zoomed-in waveforms of switching functions and VSI voltages.

Fig. 2.4. Conventional SVPWM strategy at voltage sector of I.

Fig. 2.5 shows the calculated duty cycles of the voltage space vectors at the modulation index of 0.7 and 1.155 ($=2/\sqrt{3}$). The ratio of the amplitude of the VSI line-to-line voltage V_{out} and the dc-link voltage E_{dc}, defined as the voltage transfer ratio, is calculated as

$$\text{Voltage transfer ratio} = \frac{V_{out}}{E_{dc}} = \frac{\sqrt{3}}{2} m. \quad \text{.....(2.7)}$$

Fig. 2.5 demonstrates that the duty cycles of the voltage space vectors are realistic values up to the modulation index of 1.155. If the modulation index is set to more than 1.155, the non-linear voltage error occurs in the VSI line-to-line voltage. The space vector PWM approaches achieve the maximum voltage transfer ratio of 1.0.



(a) m = 0.7. (b) m = 1.155.

Fig. 2.5. Calculated duty cycles of voltage space vectors.

2.2.2 Carrier-based Continuous PWM

Fig. 2.6 shows the triangular carrier-based continuous PWM (CPWM) strategies. Note that the switching frequency (carrier frequency) is set to be low for the better illustration. In practical, the switching frequency is set to several ten times higher than the fundamental frequency in order to achieve the lower switching harmonics of the VSI output voltages and the higher control response. The three-phase continuous modulating signals are expressed as

$$\begin{cases} v^*_{u.CPWM}(t) = m \cdot \cos(2\pi ft) \\ v^*_{v.CPWM}(t) = m \cdot \cos(2\pi ft - 2\pi/3) \\ v^*_{w.CPWM}(t) = m \cdot \cos(2\pi ft + 2\pi/3) \end{cases} \quad \text{.....(2.8)}$$

The switching functions are directly obtained by comparing the three-phase continuous modulating signals and the high-frequency triangular carrier. So, these approaches require only the general-purpose micro-computer and do not require FPGA. On the other hand, the linear modulation region is limited to the positive-peak and negative-peak of the triangular carrier. The maximum voltage transfer ratio is limited to 0.866 ($=\sqrt{3}/2$) in the carrier-based continuous PWM approaches.

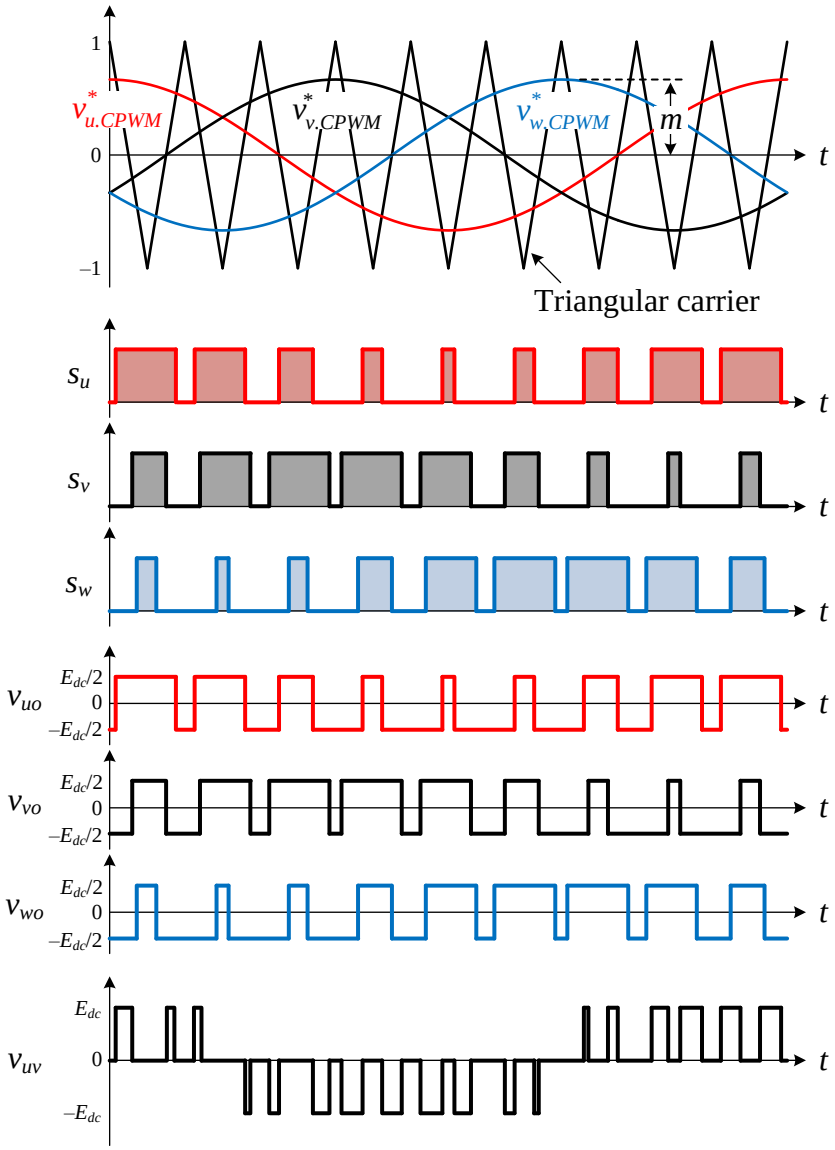


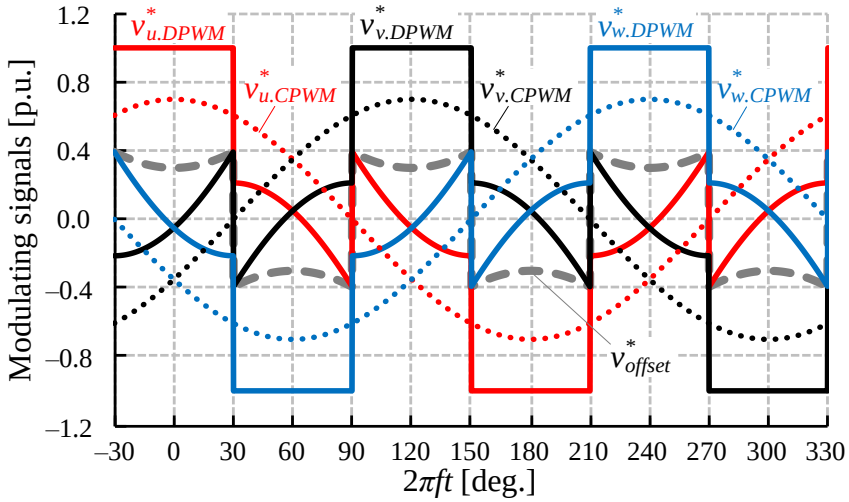
Fig. 2.6. Triangular carrier-based continuous PWM strategies.

2.2.3 Carrier-based Discontinuous PWM

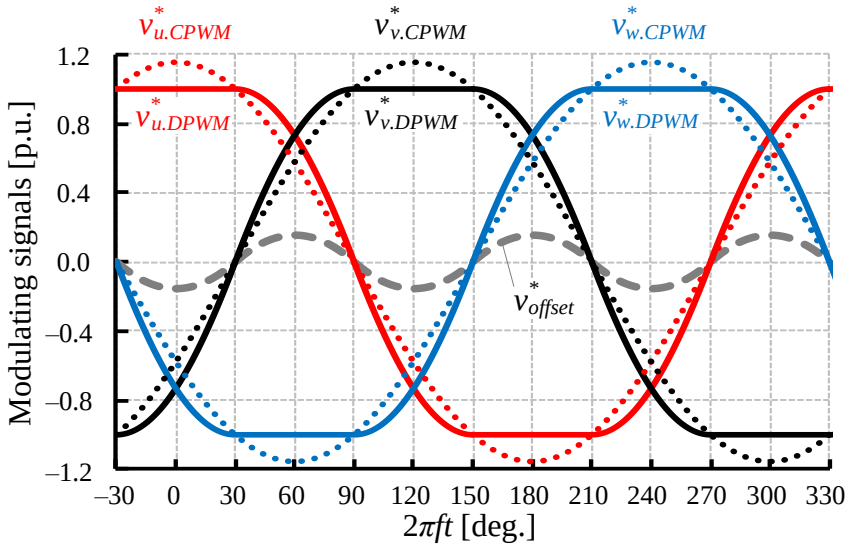
Fig. 2.7 shows the waveforms of conventional discontinuous modulating signals and its injected zero-sequence signals at the modulation index of 0.7 and 1.155 ($=2/\sqrt{3}$). The discontinuous modulating signals are obtained by injecting the zero-sequence signal v^*_{offset} into the continuous modulating signals as [2-8]–[2-10]

$$
\begin{aligned}
&v^*_{x.DPWM} = v^*_{x.CPWM} + v^*_{offset}, \quad (x = u, v, w), \\
&v^*_{offset} = \begin{cases} 1 - |v_{\max}| & \text{if } |v_{\max}| \geq |v_{\min}| \\ -1 + |v_{\min}| & \text{if } |v_{\min}| < |v_{\max}| \end{cases}, \\
&\text{and} \begin{cases} v_{\max} = \max\left[v^*_{u.CPWM}, v^*_{v.CPWM}, v^*_{w.CPWM} \right] \\ v_{\min} = \min\left[v^*_{u.CPWM}, v^*_{v.CPWM}, v^*_{w.CPWM} \right] \end{cases}.
\end{aligned}
\qquad \text{.....(2.9)}
$$

The absence of the neutral current path in the AC motor load provides a degree of freedom in determining the duty cycles. In a carrier-based approaches, this degree of freedom appears in injecting zero-sequence signal to the continuous modulating signals. By injecting the zero-sequence signal defined in (2.9), the voltage linearity is kept up to the modulation index of 1.155, leading the maximum voltage transfer ratio of 1.0.



(a) m = 0.7.



(b) m = 1.155.

Fig. 2.7. Modulating signals of conventional DPWM and its injected zero-sequence signal.

Fig. 2.8 shows the triangular carrier-based discontinuous PWM (DPWM) strategies. The number of switching transitions is reduced compared to SVPWM and CPWM because one leg is always clamped during each control period.

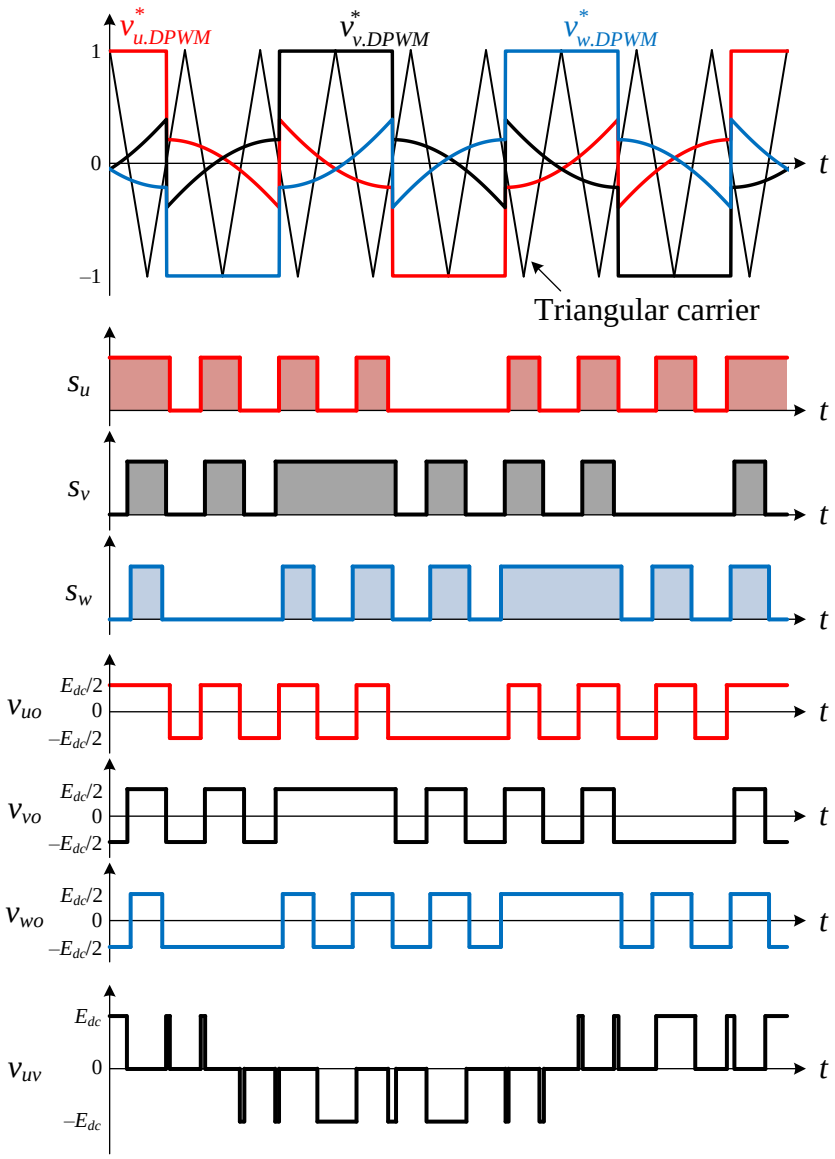


Fig. 2.8. Triangular carrier-based discontinuous PWM strategies.

2.2.4 Comparison of Classical PWM Strategies

Although the space vector PWM approaches and the carrier-based PWM approaches provide PWM control of VSI in different ways, they have certain similarities and are shown to be identical [2-11].

Fig. 2.9 shows the equivalent modulating signals of SVPWM when the duty cycles of two zero vectors are equally partitioned (t_0 = t_7) at the modulation index of 0.7. The equivalent modulating signals of SVPWM and its injected zero-sequence signal are expressed as [2-11]

$$v^*_{x.SVPWM} = v^*_{x.CPWM} + v^*_{offset}, \quad (x = u, v, w),$$
$$v^*_{offset} = \frac{1}{2} v_{\text{mid}}, \qquad \text{.....(2.10)}$$
$$\text{and } v_{\text{mid}} = \text{mid}\left[v^*_{u.CPWM}, v^*_{v.CPWM}, v^*_{w.CPWM} \right].$$

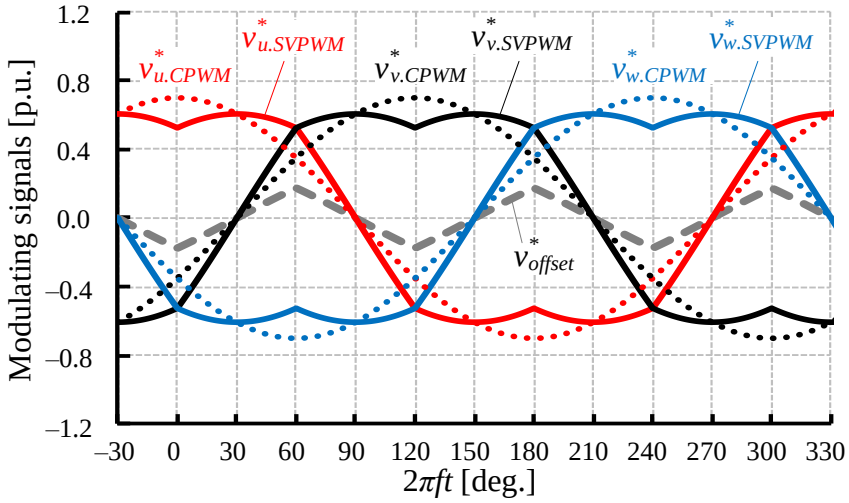


Fig. 2.9. Equivalent modulating signals of SVPWM at m = 0.7.

Fig. 2.10 shows the harmonic contents contained in modulating signals of CPWM, DPWM, and SVPWM at modulation index of 0.7. The modulating signals of DPWM have the largest triplen harmonics under this condition due to the injected zero-sequence signal. SVPWM also have the triplen harmonics which is not so large as DPWM. These increased triplen harmonics of the modulating signals generate the larger baseband harmonics,

the first carrier sidebands, in the line-to-line voltage of VSI, worsening the AC motor current quality [2-12].

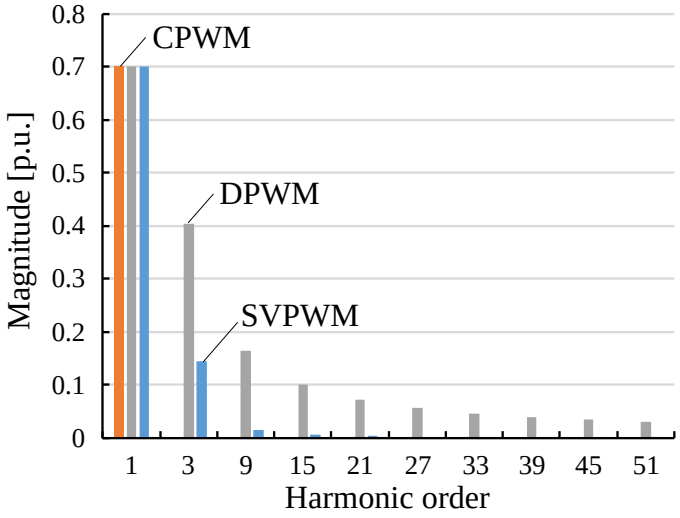


Fig. 2.10. Harmonic contents in modulating signals of CPWM, DPWM, and SVPWM at m = 0.7.

Table 2.1 lists the comparison of classical PWM strategies. Each approach has both of advantage and disadvantage. CPWM offers the PWM signals with no injection of zero-sequence signal, leading the smallest harmonics in VSI output voltage and current. However, CPWM leads to poor voltage transfer ratio compared to the other strategies.

On the other hand, DPWM achieves the maximum transfer ratio of 1.0. In addition, the number of switching transitions is only two-thirds of those with other strategies, leading to the reduction of switching losses. However, the large injected triplen harmonics in its modulating signal causes the large harmonics in AC motor current, leading increase of AC motor losses or torque ripple.

On another front, SVPWM achieves the maximum transfer ratio of 1.0 with not so large injected zero-sequence signal. The highest hardware demand of SVPWM leads to not only the degree of freedom in the gate pulse

layout but also the increase in cost. In some AC motor drive applications such as the electric vehicle, FPGA is not used due to its cost issue.

Note that the comparison of the dc-link capacitor current harmonics with classical PWM strategies is performed in the following chapter with the detailed analysis.

TABLE 2.1.
COMPARISON OF CLASSICAL PWM STRATEGIES.

Comparison Aspects	Strategy		
	Carrier-based CPWM	Carrier-based DPWM	SVPWM
Number of switching transitions in control period	6	4	6
Maximum modulation index with voltage linearity	1.0	1.155	1.155
Maximum voltage transfer ratio	0.866	1.0	1.0
Injected triplen harmonics in modulating signals	No injection	Large	Medium
Digital hardware demand	Micro-computer	Micro-computer	DSP + FPGA

2.3 Analysis of DC-link Capacitor RMS Current

Table 2.2 lists the instantaneous values of the dc-link current with regard to the voltage space vector. The dc-link current is the superposition summation of the switched current pulses from each leg and is calculated as [2-13]–[2-15]

$$i_{DC.in}(t) = \sum_{x=u,v,w} \left(s_x(t) \times i_x(t) \right). \quad \text{..... (2.11)}$$

This equation (2.11) indicates that the dc-link current is dependent on not only the switching patterns but also the load current conditions.

The dc-link current $i_{DC.in}$ is split into two ways.

- A current $i_{DC.in.ave}$, coming from the converter-side or battery-side, of which the average value is constant.
- A variable current i_C, flowing through the DC-link capacitors.

Fig. 2.11 shows the zoomed-in waveforms of the dc-link current $i_{DC.in}$, defined in Fig. 2.1, with each classical PWM strategy at the modulation index of 0.7, the phase angle of 25°, and the load power factor of 0.866. Note that the phase currents are assumed to be almost constant during a control

TABLE 2.2.
INSTANTANEOUS VALUES OF DC-LINK CURRENT WITH REGARD TO VOLTAGE SPACE VECTOR.

Voltage space vector	$i_{DC.in}$
$\mathbf{V_0}$ (0 0 0)	0
$\mathbf{V_1}$ (1 0 0)	i_u
$\mathbf{V_2}$ (1 1 0)	$i_u+i_v= -i_w$
$\mathbf{V_3}$ (0 1 0)	i_v
$\mathbf{V_4}$ (0 1 1)	$i_v+i_w= -i_u$
$\mathbf{V_5}$ (0 0 1)	i_w
$\mathbf{V_6}$ (1 0 1)	$i_u+i_w= -i_v$
$\mathbf{V_7}$ (1 1 1)	0

period. The shaded area of the dc-link current waveform in Fig. 2.11 indicates the root-mean-square (rms) value of the current flowing into the dc-link capacitors, which is calculated as

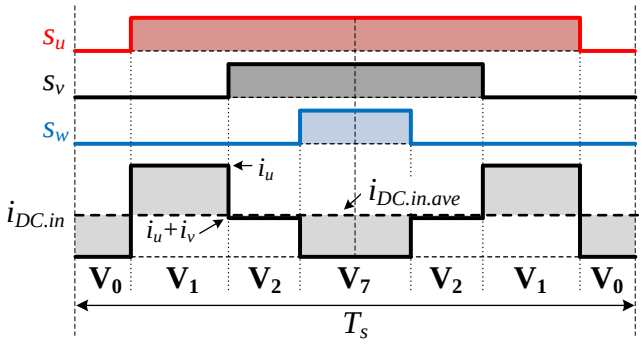
$$i_{C.rms}(T_s)=\sqrt{i^2_{DC.in.rms}(T_s)-i^2_{DC.in.ave}},$$
$$\begin{cases} i_{DC.in.rms}(T_s)=\sqrt{\dfrac{1}{T_s}\int_0^{T_s} i^2_{DC.in}\,dt} \\ i_{DC.in.ave}=\dfrac{3}{4}m\cdot I_m\cos\varphi \end{cases}. \quad \text{.....(2.12)}$$

Fig. 2.11 demonstrates that the difference between the classical PWM strategies is only the layout of the zero vectors $\mathbf{V_0}$ and $\mathbf{V_7}$. According to (2.12), the layout of the voltage space vectors in each control period does not affect the rms value of the dc-link capacitor current. Therefore, there is no difference in the dc-link capacitor current harmonics between the classical PWM strategies.

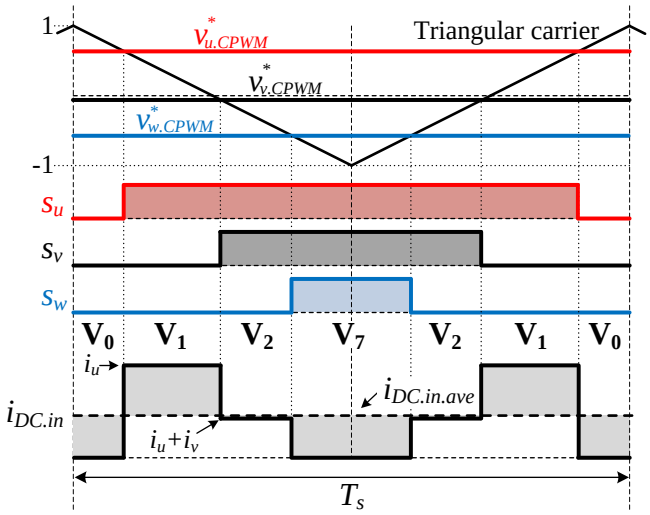
The dc side of the three-phase VSI operates at six-fold fundamental frequency. Hence, the normalized dc-link capacitor rms current is calculated based on (2.12) by considering only a sixth of the fundamental period as

$$I_{C.rms(\text{p.u.})}=\frac{1}{I_m}\sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}}\left(\sum\left[\frac{t_k}{T_s}\left(i_{DC.in.k}-i_{DC.in.ave}\right)^2\right]\right)d\theta} \quad \text{.....(2.13)}$$

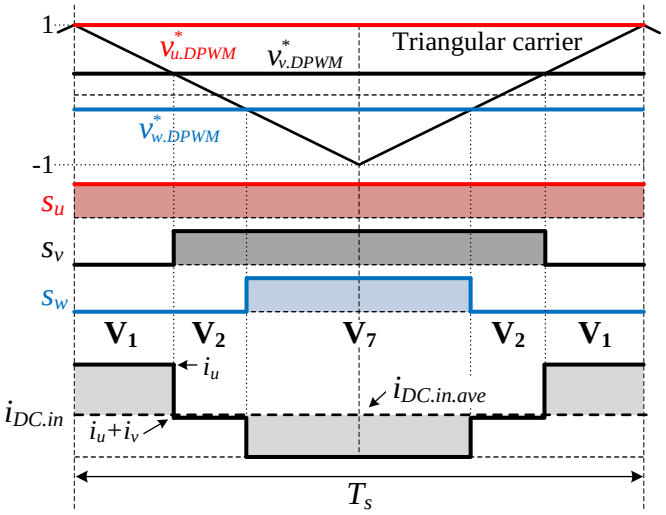
where t_k (k = 0 – 7) is the duty cycle of the applied voltage space vector $\mathbf{V_k}$ within T_s, and $i_{DC.in.k}$ is the instantaneous value of dc-link current with the voltage space vector $\mathbf{V_k}$.



(a) SVPWM.



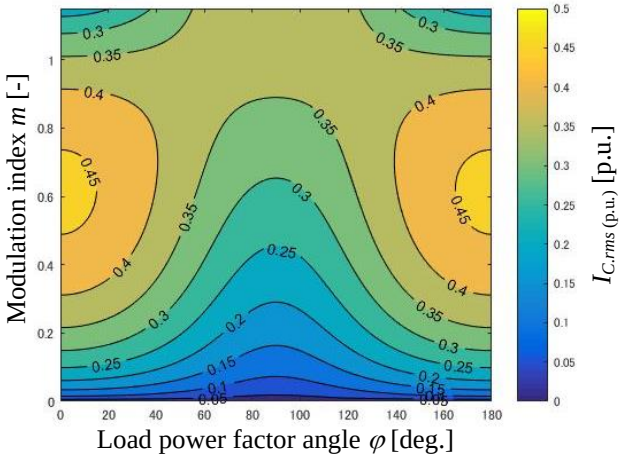
(b) CPWM.



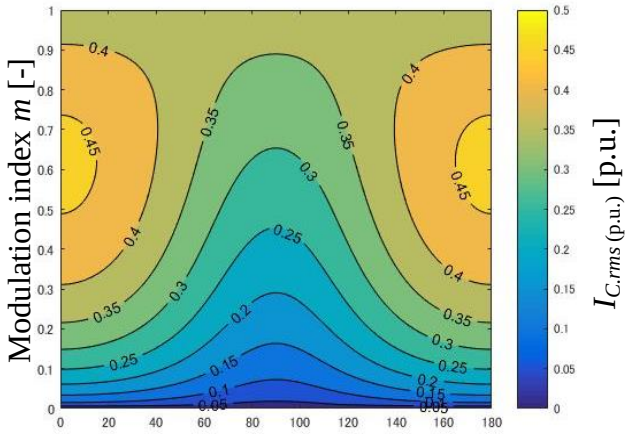
(c) DPWM.

Fig. 2.11. Zoomed-in waveforms of dc-link current at m = 0.7, $2\pi ft$ = 25°, and cos φ = 0.866 (30° lagging).

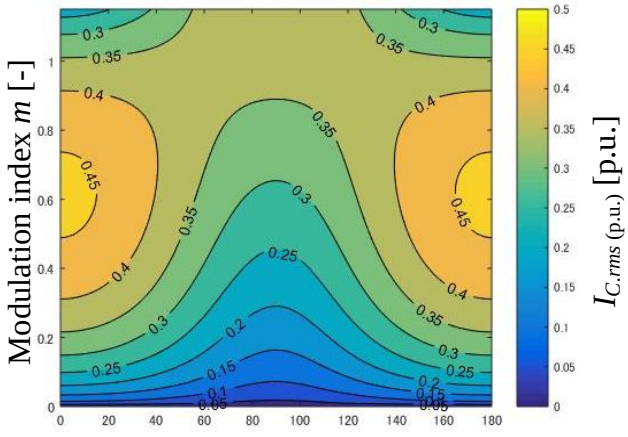
Fig. 2.12 shows the analytical results of the rms value of dc-link capacitor current with regard to the modulation index and the load power factor angle. These analytical results demonstrate that the dc-link capacitor current harmonics is exactly same between the classical SVPWM, CPWM and DPWM. The dc-link capacitor current harmonics become the maximum at around $m = 0.6$ and absolute value of the load power factor $|\cos \varphi| = 1.0$ due to the large difference between $i_{DC.in}$ (= 0 A) and $i_{DC.in.ave}$ at the applying duration of zero vectors $\mathbf{V_0}$ and $\mathbf{V_7}$.



(a) SVPWM.



(b) CPWM.



(c) DPWM.

Fig. 2.12. Analytical results of dc-link capacitor rms current with regard to modulation index m and load power factor angle φ.

2.4 Capacitor Types and Characteristics for DC-link Application

According to the previous chapter, the high-frequency ripple current which is dependent on the PWM strategy flows in the dc-link capacitor. This chapter introduces the capacitor types and its characteristics.

Three types of capacitors are generally available for dc-link applications, which are the aluminum electrolytic capacitors (Al-Caps), metallized polypropylene film capacitors (MPPF-Caps), and high capacitance multi-layer ceramic capacitors (MLC-Caps).

Fig. 2.13 depicts the relative permittivity, continuous operational field strength and energy density limits of Al_2O_3, polypropylene, and ceramics which are the dielectric used in Al-Caps, MPPF-Caps, and MLC-Caps,

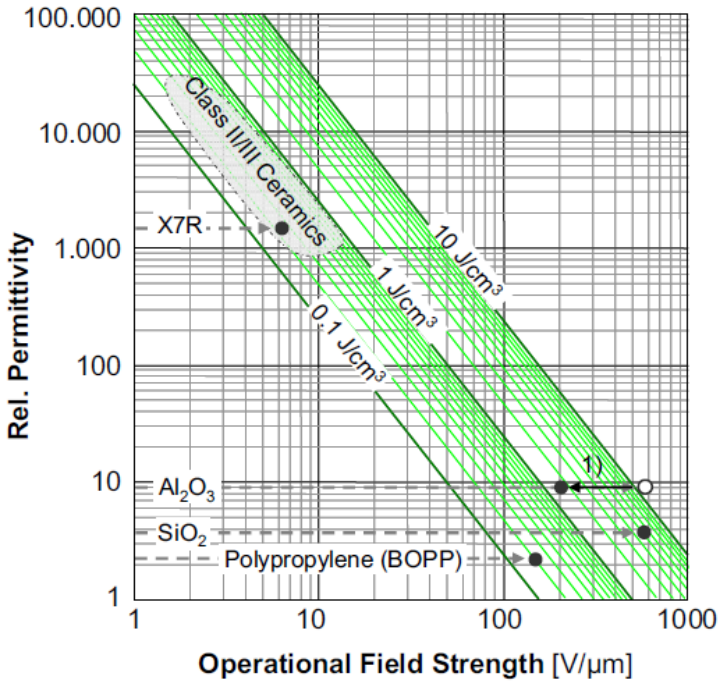


Fig. 2.13. Energy storage density for various dielectrics.
(Adapted from [2-16] M. Marz, A. Schletz, B. Eckardt, S. Egelkraut, and H. Rauh, “Power electronics system integration for electric and hybrid vehicles,” in *Proc. Int. CIPS*, pp. 1–10, 2010.)

respectively [2-16]. This figure demonstrates that Al_2O_3 has the highest energy density due to its high field strength and high relative permittivity. On the other hand, ceramics could have much higher relative permittivity, however, it suffers from low field strength, resulting in similar energy density as those of film.

Al-Caps could achieve the highest energy density; however, it has a few critical problems such as low ripple current ratings due to its relatively high equivalent series resistances (ESRs), and wear out issue due to evaporation of electrolyte. So, the capacitor ripple current capability should be considered to achieve the high power density of the AC motor drive system.

Fig. 2.14 shows the capacitance requirement against the ripple current rating. The ripple current capability of the three types of capacitors is approximately proportional to their capacitance values. Those capacitance values are defined as the minimum required capacitance value to fulfill the

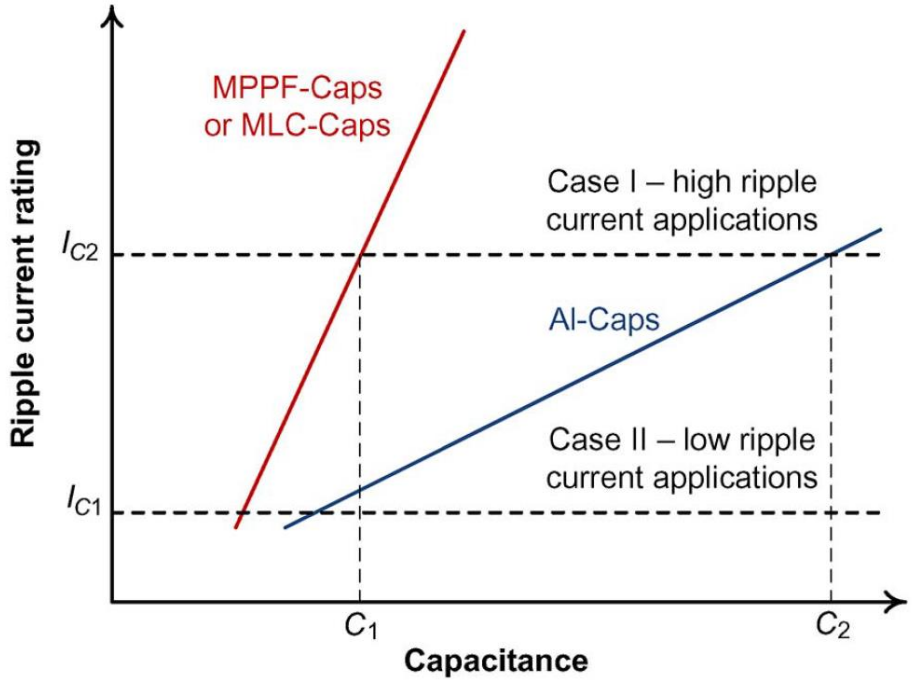


Fig. 2.14. Capacitance requirement against ripple current rating.
(Adapted from [2-17] H. Wang and F. Blaabjerg, "Reliability of Capacitors for DC-Link Applications in Power Electronics Converter—An Overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, 2014.)

voltage ripple specification. The gradient A/μF of Al-Caps is relatively smaller than those of MPPF-Caps and MLC-Caps. This is due to the design requirements, the intrinsic relationship between stored energy and ESR of capacitor dielectric, the thermal conductivity, and economic constraints [2-17]. Therefore, in high ripple current applications such as electric vehicles, the higher power density dc-link design with MPPF-Caps can be achieved.

Table 2.3 lists the comparison of failure and self-healing capability of Al-Caps, MPPF-Caps, and MLC-Caps [2-17]. Electrolyte vaporization is the major wear out mechanism of Al-Caps due to their high ESR [2-18]. The most reliability feature of MPPF-Caps is their self-healing capability [2-19]–[2-20]. Initial breakdowns at load weak points will be cleared and the capacitor regains its full ability except for a negligible capacitance reduction.

TABLE 2.3.
COMPARISON OF FAILURE AND SELF-HEALING CAPABILITY OF THREE TYPES OF CAPACITORS.
(Adapted from [2-17] H. Wang and F. Blaabjerg, "Reliability of Capacitors for DC-Link Applications in Power Electronics Converter—An Overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, 2014.)

	Al-Caps	**MPPF-Caps**	**MLCC-Caps**
Dominant failure modes	wear out		
	open circuit	open circuit	short circuit
Dominant failure mechanisms	electrolyte vaporization; electrochemical reaction	moisture corrosion; dielectric loss	insulation degradation; flex cracking
Most critical stressors	T_a, V_C, i_C	T_a, V_C, humidity	T_a, V_C, vibration
Self-healing capability	moderate	good	no

T_a: ambient temperature,
V_C: capacitor voltage stress,
i_C: capacitor ripple current stress.

For MPPF-Caps, the self-heating leads to connection instability. The MLC-Caps have high ripple current capability and its current stress reduction might not be effective in improving the reliability. However, the failure of MLC-Caps may induce severe consequences to AC motor drive systems due to the short circuit failure mode. The dominant failure causes of MLC-Caps are insulation degradation and flex cracking. So, MLC-Caps might not be suitable for traction applications, where the vibration frequently occurs.

As a conclusion, Al-Caps and MPPF-Caps are suitable for the dc-link applications of the AC motor drive systems. Al-Caps achieves high energy density; however, it suffers from wear out issue due to evaporation of electrolyte, leading to short lifetime expectancy. Thus, AL-Caps are not suitable for high ripple current applications. On the other hand, MPPF-Caps achieves longer lifetime expectancy due to the lack of wear out issue. However, the capacitance value and volume of MPPF-Caps are determined by its rated ripple current and those volume is relatively high in the whole AC motor drive system, especially in the high ripple current applications such as electric vehicles (EVs). So, this paper focuses on mainly EV applications where the capacitor ripple current is key factor in the system power density. In order to extend the dc-link capacitor lifetime or reduce its volume for the high power density, there are two possible approaches: removing the dc-link capacitor or reducing its required capacitance values, and reducing the dc-link capacitor current stress.

2.5 Conventional Approaches to Improve Reliability of DC-link Capacitors

2.5.1 Circuit Configuration-Dependent Approaches

Matrix Converter (3ϕ/AC–3ϕ/AC)

Fig. 2.15 shows the configuration of matrix converter. The matrix converter is defined as the forced commutated AC–AC converter topologies that provide simultaneous amplitude and frequency transformation of multi-phase voltage-current systems without intermediate energy storage [2-21]–[2-24]. Due to the elimination of the dc-link energy storage capacitor, not only the system reliability but also the system volume and weight are improved. This converter requires a bidirectional four-quadrant switch capable of blocking voltage and conducting current in both directions. The two reverse blocking IGBTs connected in antiparallel provide the switch requirement for the matrix converter [2-25]. With those advantages, the matrix converter has been commercialized for industry use [2-26]. However, the matrix converter has several concerns for the wide applications. First, there is a limitation of maximum voltage transfer ratio, which is up to 0.866, might be imposing AC motor voltage derating. Second, the matrix converter does not have dc-link capacitors, thus cannot store meaningful energy. Therefore, the matrix converter provides limited ability to maintain control of the load motor during a power fluctuation [2-27].

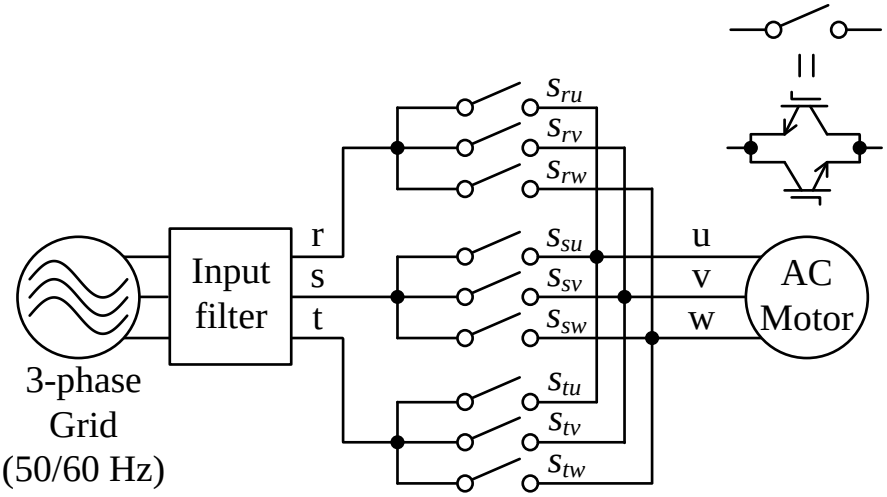


Fig. 2.15. Configuration of matrix converter.

BTB System (3ϕ/AC–DC–3ϕ/AC)

Also in the BTB system shown in Fig. 1.2(b), the dc-link capacitance can be reduced by reducing the capacitor current ripple. The causes of ripple current are placed into two groups: power flow unbalance and high-frequency PWM switching.

Power flow unbalance occurs due to the imperfections in the control of energy flow between 3ϕ/AC–DC converter and DC–3ϕ/AC inverter. The difference between the dc-link currents of 3ϕ/AC–DC converter and DC–3ϕ/AC inverter will flow to/from the capacitor, causing the low-frequency capacitor current ripple. So, by directly controlling the capacitor current in order to match the input and output powers of the system, a very small dc-link capacitor is applicable [2-28]. However, due to the control bandwidth limitation imposed by the switching frequency, these methods suppress only low-frequency ripple effects.

On the other hand, the capacitor current ripple caused by PWM switching is to be reduced by specific control over the converter and inverter PWM carriers' phase angles. As a result of the carrier phase angle optimization, the harmonics of the converter and inverter are synchronized in phase such that their cancellation occurs in the dc-link capacitor [2-29]. As another approach,

DPWM-based approach to optimizing the clamped phase of the modulating signals for the capacitor current reduction has been also proposed [2-30]. However, a limitation of those approaches is that the switching frequency of both converter and inverter should be same, which is not typical for some applications.

Electrolytic Capacitor-less Converter (1ϕ/AC–DC–3ϕ/AC)

Fig. 2.16 shows the configuration of electrolytic capacitor-less converter [2-31]–[2-35]. It consists of a single-phase diode rectifier, a small film capacitor, and a three-phase VSI. This system does not compensate the single-phase power ripple at the DC-stage and directly send it to the motor side as a torque ripple. The torque ripple is finally absorbed into the AC motor's moment of inertia. This system can achieve the low cost and high reliability AC motor drive system. However, the large motor speed variations caused by the torque ripple limits the applications where the motor moment of inertia is relatively large or the motor speed ripple is ignorable.

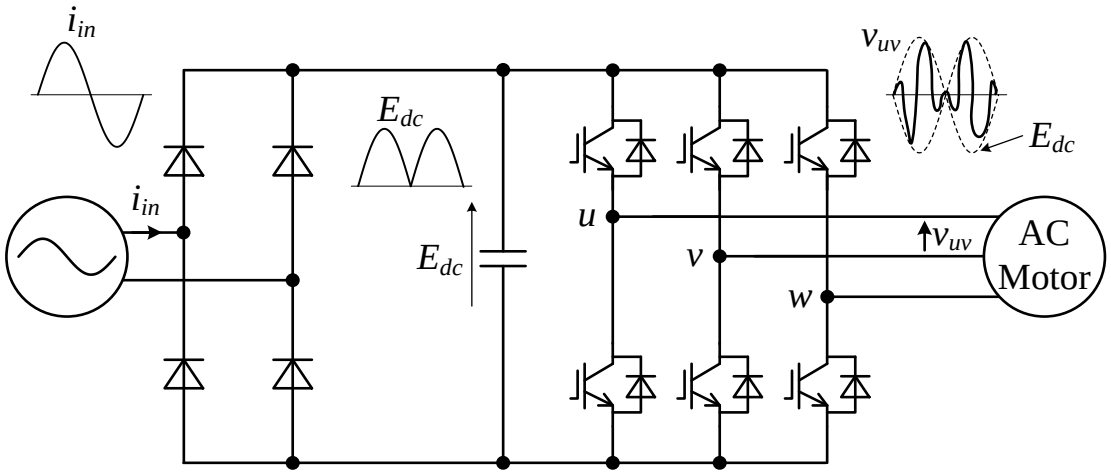


Fig. 2.16. Configuration of electrolytic capacitor-less converter.

Cascaded Converter (DC–DC–3ϕ/AC)

Fig. 2.17 shows the configuration of the cascaded DC–DC–3ϕ/AC converter. It consists of a DC-DC boost converter, a small intermediate film capacitor, and a DC–3ϕ/AC VSI. As the similar PWM concepts for the dc-link capacitance reduction in the BTB systems, modulations for DC-DC stage and DC-3ϕ/AC stage are coupled, known as stored energy modulation (SEM) [2-36]–[2-37].

Fig. 2.18 depicts the example of the equivalent voltage injections in terms of DC and AC voltages [2-36]. The energy storage in dc-link is just sufficient to provide one high switching frequency cycle of AC output at the rated power. The energy stored in the small dc-link capacitor is returned to zero at the end of every control period. With the carefully regulated duty cycles σ_1, σ_2, and σ_3 for charging and discharging and σ_i for idle interval, DC-3ϕ/AC power conversion is achieved without the large dc-link capacitor. Nevertheless, too small dc-link stored energy results in limited ability of absorbing the power injection from load during fault conditions as well as the matrix converter.

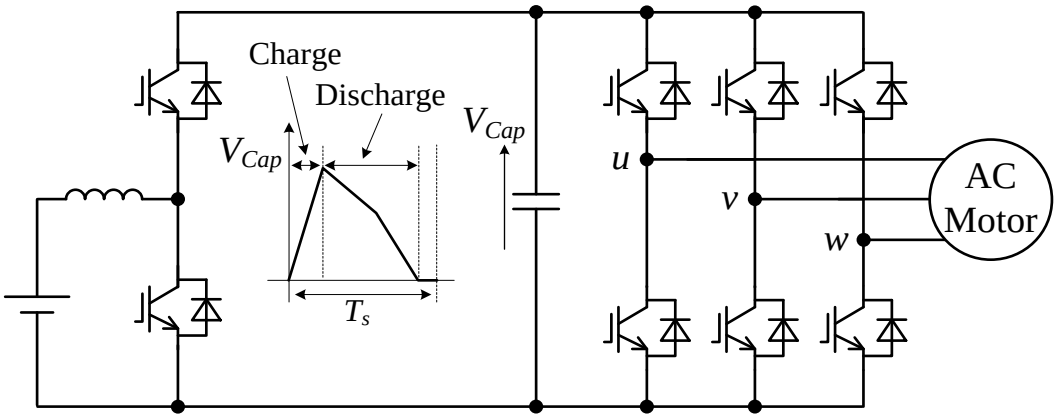


Fig. 2.17. Configuration of cascaded DC–DC–3ϕ/AC converter.

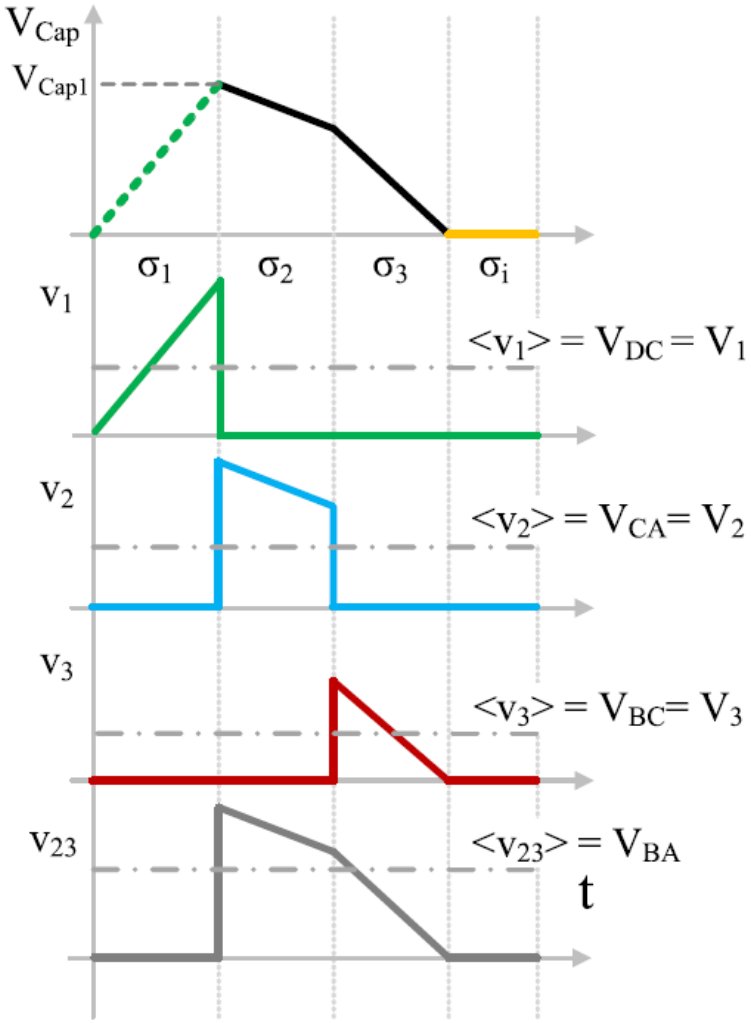


Fig. 2.18. Example of equivalent voltage injections in terms of dc and ac voltages in stored energy modulation (SEM). Indices 1–3 correspond to phase *u*–*w*, respectively.
(Adapted from [2-36] M. Gupta and G. Venkataramanan, "A DC-to-Three-Phase Boost–Buck Inverter With Stored Energy Modulation and a Tiny DC-Link Capacitor," *IEEE Trans. Ind. Appl.*, vol. 53, no. 2, pp. 1280–1288, 2017.)

Paralleled Inverters (DC–Multiple 3ϕ/AC)

Fig. 2.19 shows the configuration of the paralleled three-phase VSIs. The dc-link current of the paralleled system is calculated as a sum of the dc-link currents of each three-phase VSI as

$$i_{DC.in} = i_{DC.in.1} + i_{DC.in.2} + \cdots + i_{DC.in.N} \quad \text{.....(2.14)}$$

The use of interleaving technique in this parallel VSIs system helps cancel the dc-link capacitor current ripples [2-38]–[2-40]. This PWM techniques interleave or phase shift the inverter switching cycles, which is done by phase shifting for the carriers of the inverters. However, these approaches can be applied to a limited applications where several inverters are connected in parallel such as AC or DC electric railcars [2-41]–[2-42].

As discussed in this chapter, a lot of circuit configuration-dependent approaches to improve the dc-link capacitor reliability have been proposed. These approaches benefit the elimination of the dc-link capacitor or significant reduction of the dc-link capacitance. In contrast, the poor energy storage in the dc-link results in no ability of absorbing power injection from load during fault conditions, leading to the limited applications. Furthermore, these approaches are dependent on the circuit configuration and not to be applied to the simplest battery embedded DC–3ϕ/AC system shown in Fig. 1.2(a), which is typically applied in the electrical vehicle application where the high power density play a key role in improving fuel economy [2-43].

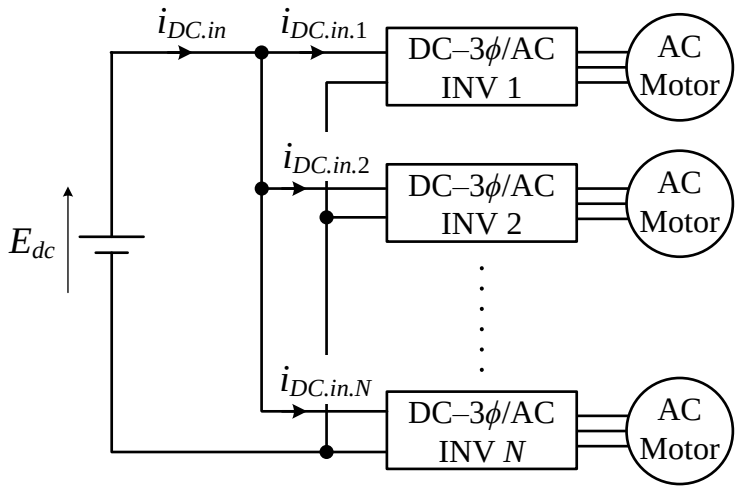


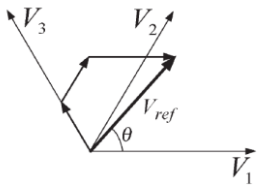
Fig. 2.19. Configuration of paralleled DC–3ϕ/AC inverters.

2.5.2 Modified PWM Approaches

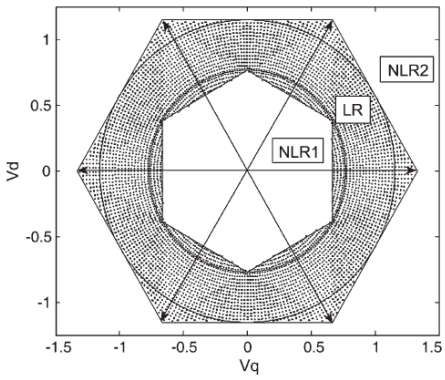
So far, several modified PWM strategies of the DC–3ϕ/AC VSI to reduce the dc-link capacitor current harmonics have been proposed [2-44]–[2-47]. These approaches are applicable for any kind of the 3ϕ/AC motor drive system due to the commonality of PWM technique.

Near-State PWM (NSPWM)

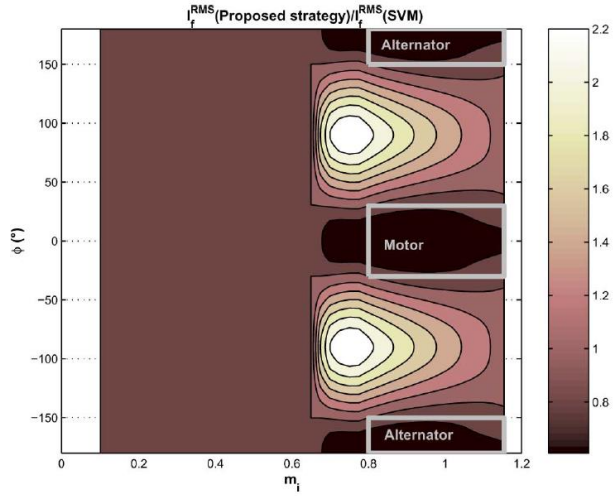
Fig. 2.20 depicts the concept of the near-state PWM (NSPWM) [2-44]–[2-46]. NSPWM has been proposed to reduce the common-mode voltage for a two-level three-phase VSI. This strategy uses a group of three neighbor active voltage vectors to match the output and reference volt-seconds, resulting in an omission of the zero vectors at high-modulation index region as shown in Fig. 2.20(a). As a result, not only the common-mode voltage but also the dc-link capacitor current harmonics are reduced when the load power factor is higher than 0.8. However, NSPWM is applicable only when the modulation index is higher than 0.667 (= 2/3) due to the restrictions on the voltage space vector use as shown in Fig. 2.20(b). Therefore, the dc-link capacitor current harmonics are not to be reduced at low-modulation indices with NSPWM as shown in Fig. 2.20(c).



(a) Applied active voltage space vectors.



(b) Voltage linearity range (voltage normalized to $E_{dc}/2$).



(c) Reduction ratio of rms value of DC-link capacitor current with NSPWM compared with those with SVPWM [2-45].

Fig. 2.20. Concept of near-state PWM (NSPWM).

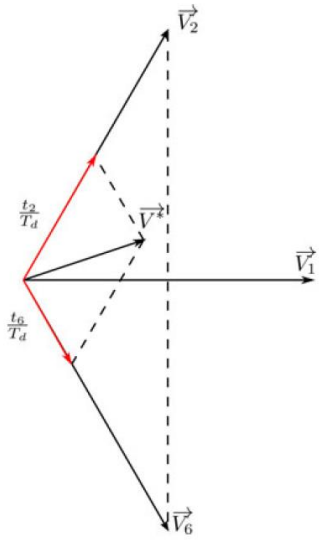
(Figs. (a) and (b): Adapted from [2-44] E. Ün and A. M. Hava, "A Near-State PWM Method With Reduced Switching Losses and Reduced Common-Mode Voltage for Three-Phase Voltage Source Inverters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 2, pp. 782–793, 2009.)

(Fig. (c): Adapted from [2-45] J. Hobraiche, J.-P. Vilain, P. Macret, and N. Patin, "A New PWM Strategy to Reduce the Inverter Input Current Ripples," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 172–180, 2009.)

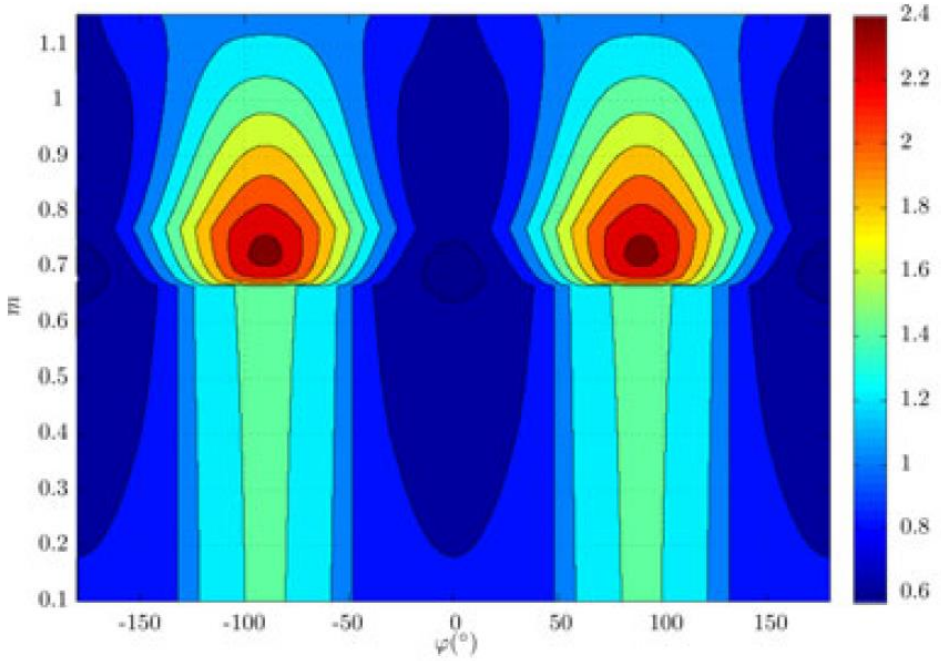
Extended Double-Carrier PWM (Ext-DCPWM)

Fig. 2.21 depicts the concept of the extended double-carrier PWM (Ext-DCPWM) [2-47]. This strategy uses the three consecutive active voltage vectors as well as NSPWM at high-modulation indices. In addition, it uses two nonadjacent active voltage space vectors and one zero vector to reduce the dc-link capacitor current harmonics when the modulation index is lower the 0.667 (= 2/3) as shown in Fig. 2.21(a). Finally, Ext-DCPWM reduces the dc-link capacitor current harmonics for all values of the modulation index when the load power factor is higher than 0.8 as shown in Fig. 2.21(b). In contrast, Ext-DCPWM worsens the dc-link capacitor harmonics at the low-load power factor region as shown in Fig. 2.21(b), indicating that this strategy is not applicable for the AC motor drive system of which the variation of the load power factor is considerably wide.

As discussed in this chapter, several modified PWM strategies of the DC–3ϕ/AC VSI to reduce the dc-link capacitor current harmonics have been proposed. These approaches benefit the reduction of the dc-link capacitor current harmonics at high load power factor ($\cos \varphi > 0.8$) region. However, the main issue occurs with the worsened dc-link capacitor current harmonics when the load power factor varies due to the variations of the motor operating condition. Furthermore, the used combinations of the voltage space vectors in those PWM strategies result in the large injected zero-sequence signal of the modulating signals. It is also necessary to consider the AC motor current quality, which is affected by those injected signals, for the AC motor's loss reduction or torque quality improvement.



(a) Applied voltage space vectors at low-modulation indices.



(b) Reduction ratio of rms value of DC-link capacitor current with Ext-DCPWM compared with those with SVPWM.

Fig. 2.21. Concept of extended double-carrier PWM (Ext-DCPWM).

(Adapted from [2-47] T. D. Nguyen, N. Patin, and G. Friedrich, “Extended Double Carrier PWM Strategy Dedicated to RMS Current Reduction in DC Link Capacitors of Three-Phase Inverters,” *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 396–406, 2014.)

2.5.3 Comparison of Conventional Approaches

Table 2.4 lists the comparison of the conventional approaches to improve the reliability of the dc-link capacitors or increase the power density. In the term of dc-link capacitance value, the matrix converter eliminates the capacitance and results in the greatest dc-link capacitor volume reduction. Similarly, BTB, electrolytic capacitor-less converter, and cascaded converter approaches enable the small and reliable film capacitor as the dc-link capacitor, also leading to the great volume reduction. In contrast, the small dc-link stored energy results in poor ability of absorbing a power injection from the load during fault conditions (e.g., in case of an emergency stop of a converter, where the magnetic excitation energy of the AC motor may be fed back to the dc-link), leading to the over voltage issue in dc-link. In addition, several circuit configuration-dependent approaches might have influences on the motor control performance. The limited maximum voltage transfer ratio of the matrix converter might limit the motor operating region. The dc-link capacitance reduction approaches in BTB system are based on the assumption of same fundamental frequencies of the grid side and the load side, limiting the motor variable speed range. The electrolytic capacitor-less converter directly send the single-phase power ripple to the motor side as a torque ripple. Finally, in the term of the configuration simplicity, the matrix converter and the paralleled inverters might result in complicated system. While the DC–3ϕ/AC inverter itself in the paralleled system is the simple, the parallelization of the inverters increases the number of components in the total system; so, it is applied only for the high-power applications such as electric railcars.

As a conclusion, the current stress reduction for the stiff dc-link capacitance by modifying the PWM strategies for the DC–3ϕ/AC VSI (including three-level VSI) might count for a great deal.

TABLE 2.4.
COMPARISON OF CONVENTIONAL APPROACHES TO IMPROVE RELIABILITY OF DC-LINK CAPACITORS OR INCREASE POWER DENSITY

Comparison Aspects	Circuit Configuration-Dependent Approaches					Modified PWM Approaches (NSPWM, Ext-DCPWM)
	Matrix Converters	BTB	Electrolytic Capacitor-less	Cascaded Converter	Paralleled Inverters	
Power Conversion Type	3ϕ/AC–3ϕ/AC, 1ϕ/AC–3ϕ/AC	3ϕ/AC–DC–3ϕ/AC	1ϕ/AC–DC–3ϕ/AC	DC–DC–3ϕ/AC	DC–Multiple 3ϕ/AC	DC–3ϕ/AC
DC-link Capacitance	N/A	Small	Small	Small	Large	Large
Fault-condition capability	Poor	Poor	Poor	Poor	Good	Good
Influence for Motor Control	Voltage limitation	Output freq. limitation	Torque Ripple	N/A	N/A	N/A
Configuration Simplicity	Complicated	Simple	Simple	Simple	Complicated	Simple

2.6 Proposed PWM Strategies to Reduce DC-link Capacitor Current Stress based on Load Current Sector

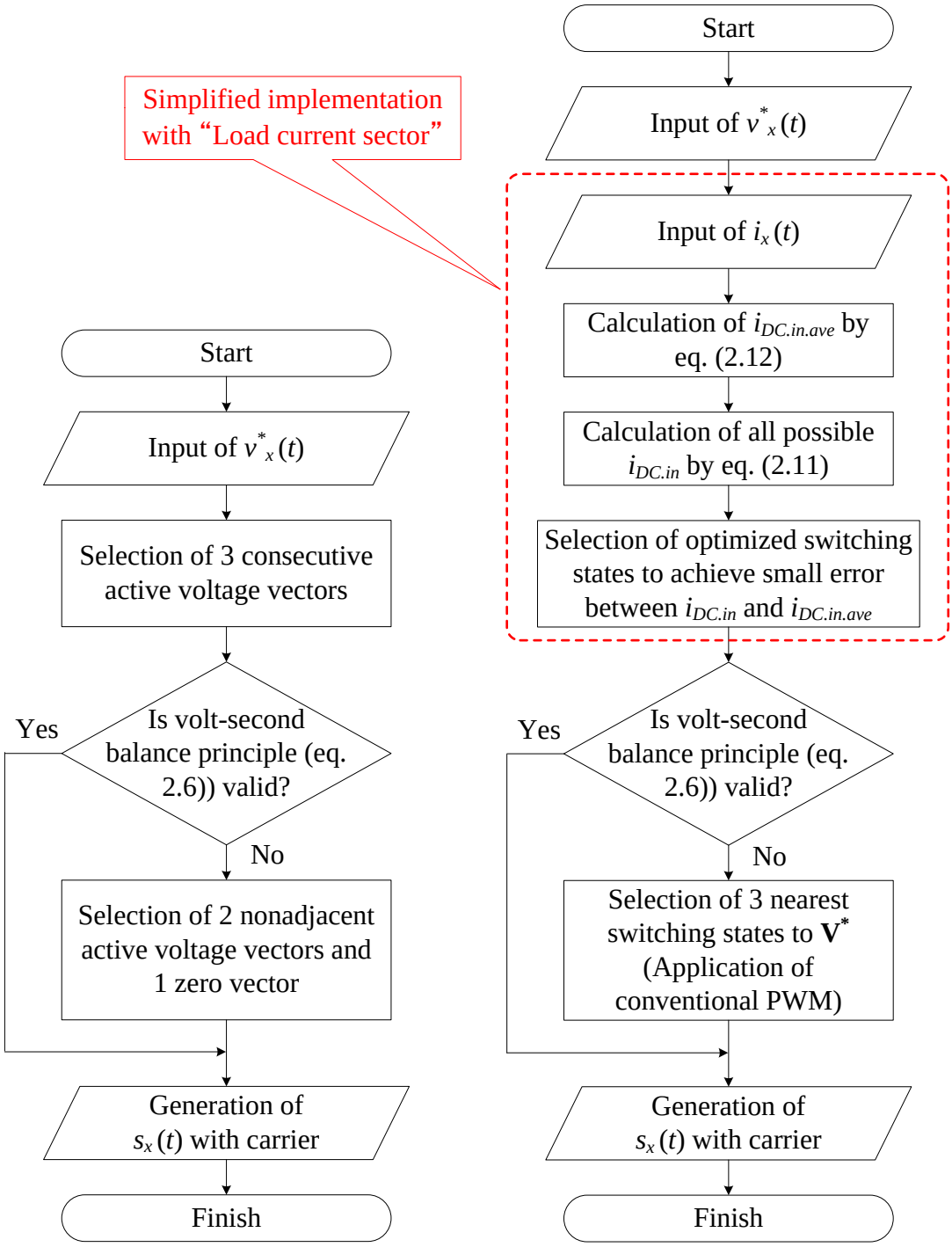
According to the previous surveys for the dc-link capacitor reliability improvements, the modification for the PWM switching patterns are chosen as the approach in this research because of the following reasons.

1. PWM is the commonality technique for the AC motor drive system, so, this approach is applicable for wide types of converter configuration.
2. Reliability improvement can be achieved without the dc-link capacitance reduction, which leads to poor ability of absorbing a power injection from the load in case of fault conditions and limitation for the application.

2.6.1 Switching Pattern Generation to Reduce DC-link Capacitor Current Stress based on Load Current Sector

Fig. 2.22 shows the switching pattern optimization principles of the conventional modified PWM strategy (Ext-DCPWM) and the proposed PWM strategy. In conventional modified PWM strategy (Ext-DCPWM), the combination of three consecutive active voltage space vectors or the combination of two nonadjacent active voltage space vectors and one zero vector is selected. These combinations are based on the off-line calculations of the dc-link capacitor rms current (2.12) under assumption of unity load power factor. Thus, the dc-link capacitor rms current is not minimized when the load power factor is varied. On the other hand, the proposed PWM strategy keeps up with the detected load current information and uses it to optimize the switching pattern. As a result, the dc-link capacitor rms current is minimized even when the load power factor is varied. However, this proposed optimization principle requires several on-line calculations,

leading to heavy computation load for the controller; thus, should not be implemented directly. Then, this paper proposes the concept of "Load current sector" to simplify the on-line optimization process for the switching pattern. For balanced three-phase load, the combination of three-phase load currents' directions switches every 60° of phase angle. In each 60° period, the optimized three switching states to achieve small error between $i_{DC.in}$ and $i_{DC.in.ave}$ are unchanged because nothing will change in the magnitude relationships of all possible values of $i_{DC.in}$ (2.11) during each 60° period. So, these 60° periods, determined by the combinations of three-phase load currents' directions, are defined as load current sectors and used for an implementation of the proposed optimization processes circled with a red-dashed-line in Fig. 2.22(b).



(a) Conventional modified PWM Strategy (Ext-DCPWM).

(b) Proposed PWM Strategy.

Fig. 2.22. Switching pattern optimization principles of conventional modified PWM strategy (Ext-DCPWM) and proposed PWM strategy.

Fig. 2.23 shows the concept of the proposed PWM strategies to reduce dc-link capacitor current stress based on the load current sector. The original point is to use the load current sector, determined by the directions (signum functions) of the three-phase load currents, in order to select the optimized switching states in the given load current condition. Note that the optimized switching states at each load current sector are stored in the database in advance based on the off-line calculations. Consequently, the proposed PWM strategies achieve the dc-link capacitor current ripple reduction at any conditions of the modulation index and the load power factor, which has not been achieved by past works. Note that the load currents are detected in most

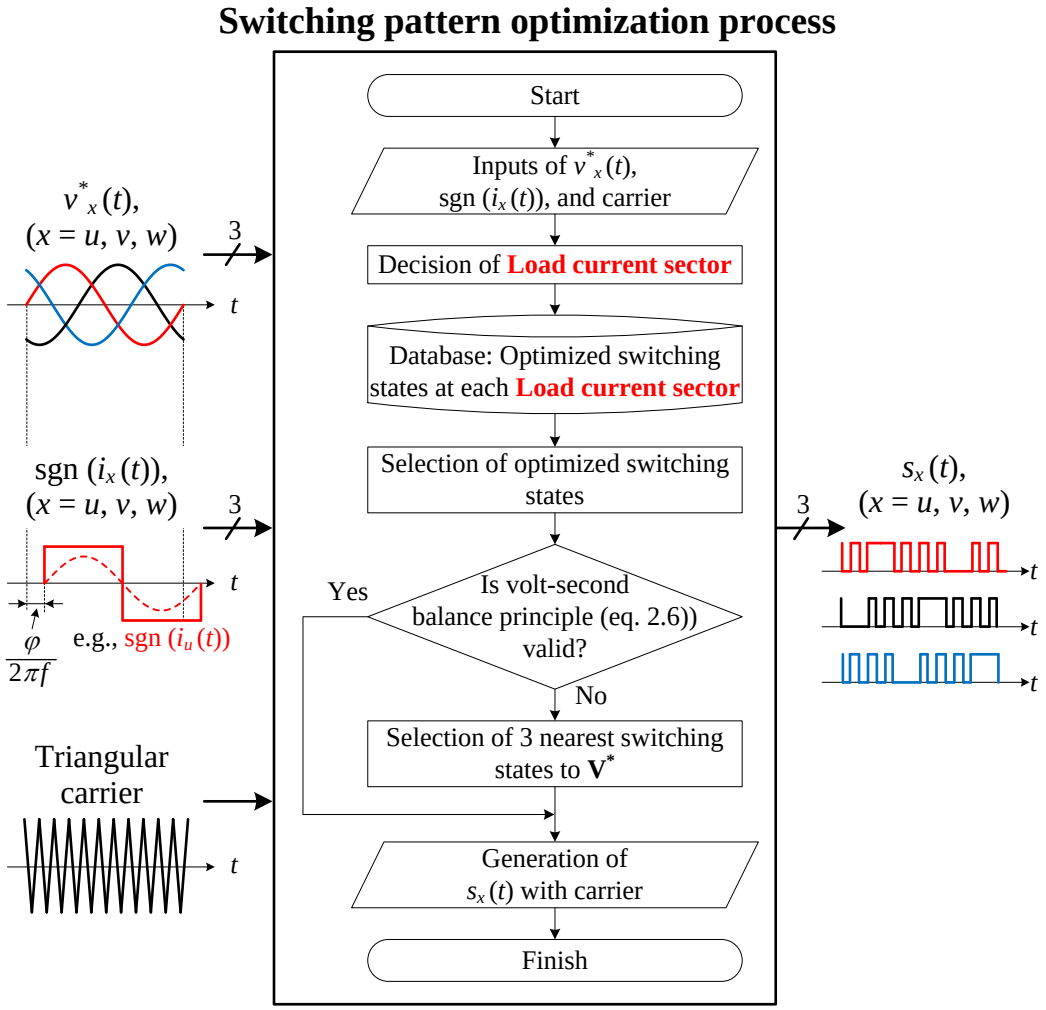


Fig. 2.23. Concept of proposed PWM strategies to reduce dc-link capacitor current stress based on load current sector.

of the AC motor drive system to control the motor torque. So, the additional current sensor is not necessary.

In addition, it is also necessary to consider not only the dc-link capacitor current stress but also the load current quality for the practical application to the AC motor drive system because the load current quality determines the load motor torque quality and its losses. Furthermore, the digital hardware demand should be also considered because it might increase the cost and be dependent on the application. Also, the maximum voltage transfer ratio is important factor for the AC motor drive system because it determines the available motor operating region. In order to reduce the dc-link capacitor current stress of the high-voltage AC motor drive system, it is also necessary to consider the application to three-level VSI, of which voltage capacity is higher than those of two-level VSI.

2.6.2 Beneficial Position of Proposed PWM Strategies

Fig. 2.24 shows the beneficial position of the proposed PWM strategies compared to the conventional PWM approaches. The x-axis and y-axis indicate the dc-link capacitor rms current $I_{C.rms}$ reducible ranges of modulation index and load power factor, respectively. Those ranges of each strategy are determined compared to $I_{C.rms}$ with the conventional PWMs, shown in Fig. 2.12. In terms of the modulation index range where $I_{C.rms}$ is reducible (x-axis), the NSPWM strategy reduces the dc-link current harmonics only when the modulation index is higher than 0.667, whereas the Ext-DCPWM strategy reduces the harmonics for all values of the modulation index. However, in terms of the load power factor range where $I_{C.rms}$ is reducible (y-axis), those strategies are effective in reducing the dc-link current harmonics only when the load power factor is high (i.e., $\cos \varphi > 0.8$). Therefore, those approaches are applicable to only the applications with the fixed and high load power factor operating condition such as grid-tied three-phase VSI [2-48] or uninterruptible power supply (UPS) [2-49]. On the other hand, the proposed PWM strategies show superior characteristics which are suitable for both fixed and varied load power factor applications. The proposed PWM strategies determine the switching patterns with the considerations of the load current conditions by using the load current sector. Consequently, the proposed PWM strategies reduce the dc-link capacitor current ripple at any conditions of the modulation index and the load power factor, which are required for the AC motor drive applications.

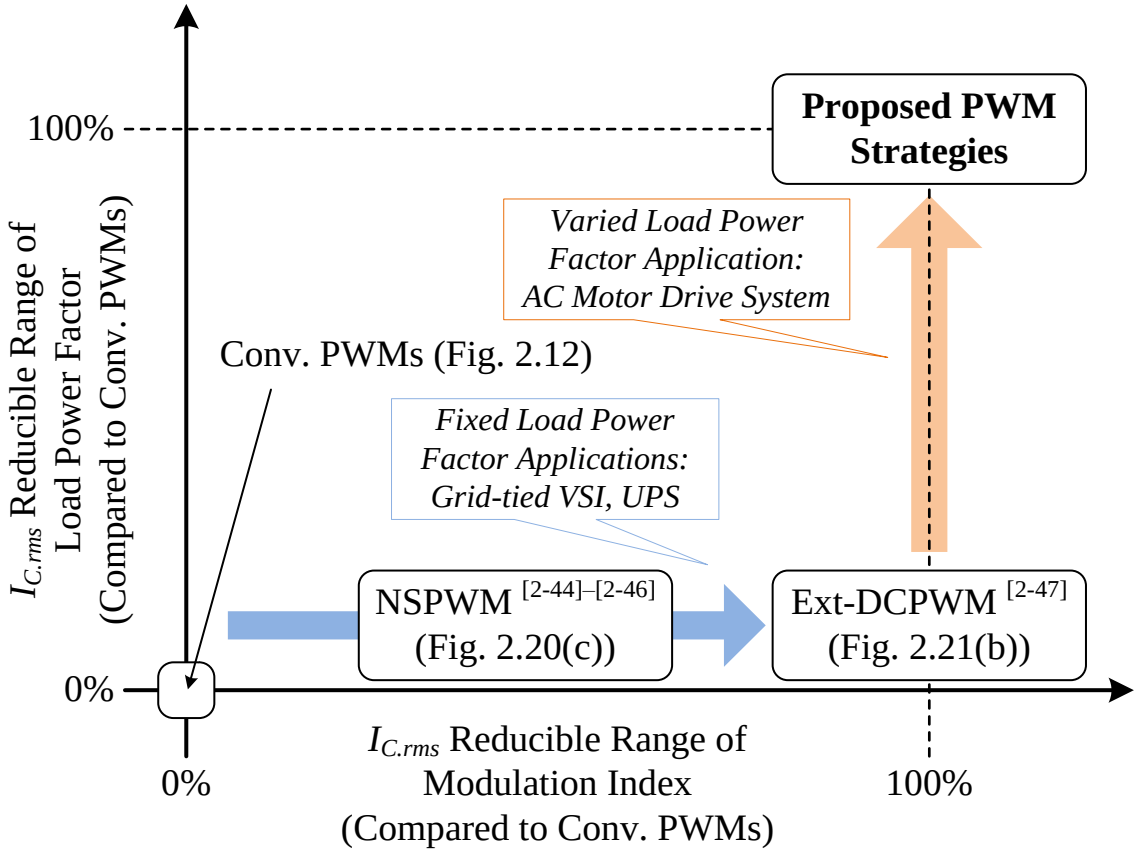


Fig. 2.24. Beneficial position of proposed PWM strategies compared to conventional PWM approaches.

2.7 Conclusion

In this chapter, first, the classical PWM strategies have been reviewed and those PWM-dependent dc-link capacitor current harmonics have been analyzed. Next, the analysis results confirm that the PWM strategy plays a key role for the dc-link capacitor current harmonics. Then, the three types of capacitors which are generally available for dc-link applications have been reviewed. It is revealed that the ceramic capacitors which have a large enough current capacity is not suitable for the traction applications where the vibration frequently occurs. Therefore, the electrolytic capacitors or film capacitors which are heat-sensitive components are necessary for the dc-link applications. For high ripple current applications such as EVs, the capacitor ripple current rating mainly determines the capacitor volume and power density; thus, this paper focuses on mainly the EV applications. After that, numerous approaches to improve the reliability of the dc-link capacitors have been reviewed. The circuit configuration-dependent approaches improve the dc-link capacitor reliability by elimination or great reduction of the dc-link capacitance. Nevertheless, those approaches raise a big problem with the low stiffness of the dc-link, which is unsuitable for the AC motor drive systems with the consideration of fault conditions. The modified PWM approaches avoids the problem and might be considered as the best way. Nevertheless, the conventional PWM approaches are able to reduce the dc-link capacitor current ripple only in a limited load power factor range.

The proposed PWM strategies determine the switching patterns with the considerations of the load current conditions by using load current sector. The concept of load current sector enables to optimize the switching states for the dc-link capacitor current stress reduction even when the load power factor is varied. Consequently, the proposed PWM strategies reduce the dc-link capacitor current ripple at any conditions of the modulation index and the load power factor, which are required for the AC motor drive applications. In addition, the load current quality, the digital hardware demand, and the application to the high-voltage AC motor drive systems are also considered.

Especially for the digital hardware demand in the EV applications, FPGA is not used due to its cost issue. So, the gate pulse generation process without FPGA should be considered. The next chapter will explain the mechanism of the proposed PWM strategies and demonstrate its superior characteristics.

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Chapter 3

Optimization for PWM Switching Patterns for DC-link Capacitor Current Stress Reduction based on Space Vector PWM Strategy

3.1. Introduction

This chapter presents an optimization method for the PWM switching patterns for the current stress reduction of the dc-link capacitor in the two-level three-phase VSI based on the SVPWM strategy. Note that the optimized PWM switching patterns are implemented based on the use of high-cost digital hardware such as FPGA, whereas FPGA is not used due to its cost issue in electric vehicle applications. The original idea in this optimized PWM switching patterns is that the used voltage space vectors are selected based on the load current sector which is determined from detected three-phase load current directions. The advantages of the proposed SVPWM is the minimization for the dc-link capacitor current stress under any conditions of the modulation index and the load power factor, which is not achieved by the past works.

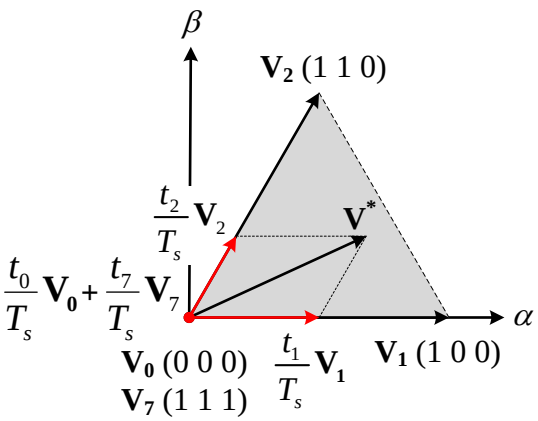
This chapter is organized as follows: First, in chapter 3.2, the methods

for reduction of the dc-link current harmonics by optimization of the voltage space vectors introduced in Ext-DCPWM [3-1] are explained in detail. In chapter 3.3, the method used to adapt to the variations of the load power factor is then presented. In chapter 3.4 and chapter 3.5, analytical, simulation, and experimental results are presented to verify the effectiveness in terms of the reduction of the dc-link current harmonics, the impact on the output phase current quality, inverter efficiency, and the dc-link capacitor heating. After that, in chapter 3.6, the lifetime of the electrolytic capacitors is estimated and compared. Finally, in chapter 3.7, the conclusion of this chapter will be presented.

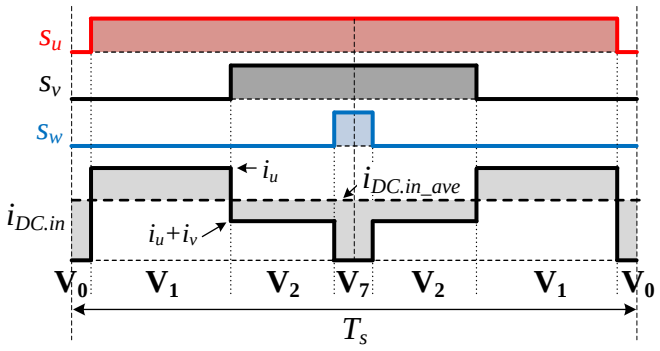
3.2. Optimal Selection for Voltage Space Vector

3.2.1 At High Modulation Indices Region

Fig. 3.1 shows the conventional SVPWM strategies and the zoomed-in waveforms of the dc-link current at the modulation index of 1.0, the load power factor of 0.866, and the phase angle of 25°. It should be recalled that the dc-link current $i_{DC.in}$ is the superposition summation of the switched pulses from each leg and is calculated as (2.11). Furthermore, the shaded area of the dc-link current waveform indicates the rms value of the dc-link



(a) Combination of voltage space vectors.



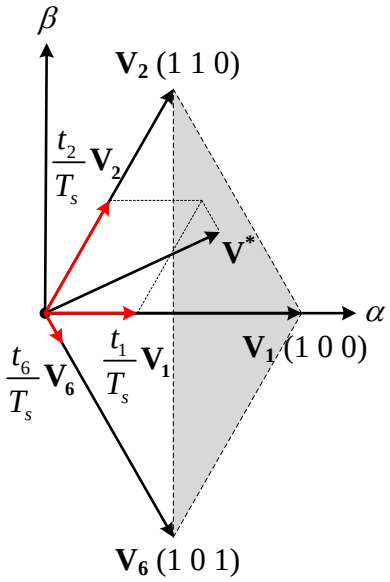
(b) Zoomed-in waveform of dc-link current.

Fig. 3.1. Conventional SVPWM strategies and zoomed-in waveforms of dc-link current at m = 1.0, cos φ = 0.866 (30° lagging), and $2\pi ft$ = 25°.

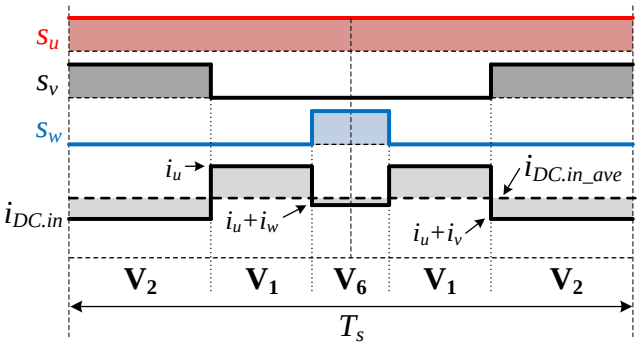
capacitor current which is calculated as (2.12). Note that a smaller difference between the instantaneous value and the average value of the dc-link current results in a smaller rms value of the dc-link capacitor current. When the conventional SVPWM is applied, two zero vectors $\mathbf{V_0}$ and $\mathbf{V_7}$ are used at each control period. When the zero vector is applied, the instantaneous value of the dc-link current becomes zero, which leads to the large dc-link current fluctuations around its average value.

Fig. 3.2 shows the optimized combination of the voltage space vectors to minimize the rms value of the dc-link current at the modulation index of 1.0, the load power factor of 0.866, and the phase angle of 25°, and when the phase currents i_u is positive, i_v and i_w are negative. As shown in Fig. 3.2(a), three consecutive active vectors ($\mathbf{V_6}$–$\mathbf{V_1}$–$\mathbf{V_2}$) are used to generate the voltage reference vector, which results in the omission of the zero vector [3-2]–[3-4]. Note that the omission of the zero vector is achieved only when the tip of the voltage reference vector belongs to the triangle formed by the tips of the three consecutive voltage space vectors shown by the shaded area in Fig. 3.2(a), i.e., at high-modulation indices. The area that is output using three consecutive voltage space vectors is the same as that with the conventional SVPWM. Thus, the optimized combinations of the voltage space vectors for the minimum rms value of the dc-link current allows the same maximum voltage transfer ratio as the conventional SVPWM to be obtained. The instantaneous dc-link input current does not become zero during a control period, as shown in Fig. 3.2(b) because the zero vectors are not applied. Furthermore, when the phase currents i_u is positive, i_v and i_w are negative, the dc-link current fluctuations around the average value is minimized with this optimized combination of the voltage space vectors ($\mathbf{V_6}$–$\mathbf{V_1}$–$\mathbf{V_2}$) at high-modulation indices compared with the conventional SVPWM shown in Fig. 3.1(b), which results in the minimum rms value of the dc-link capacitor current. Note that there is only one optimized combination of the voltage space vectors, and this optimized combination is dependent on the modulation index, phase angle, and load currents. In order

to optimize the combination of the voltage space vectors to obtain the minimum rms value of the dc-link current, first, the instantaneous values of the dc-link current of each combination of three voltage space vectors are calculated based on (2.11). Next, the combination, which makes the instantaneous values of the dc-link current become the closest to its average value, is selected.



(a) Combination of voltage space vectors.

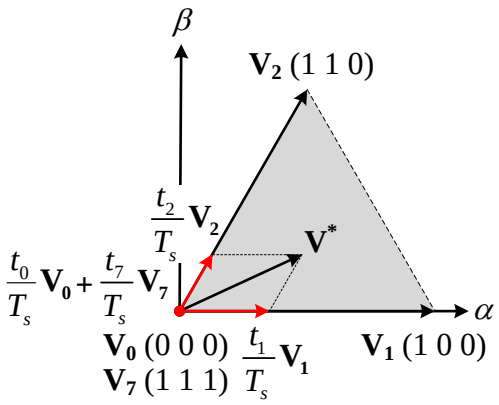


(b) Zoomed-in waveform of dc-link current.

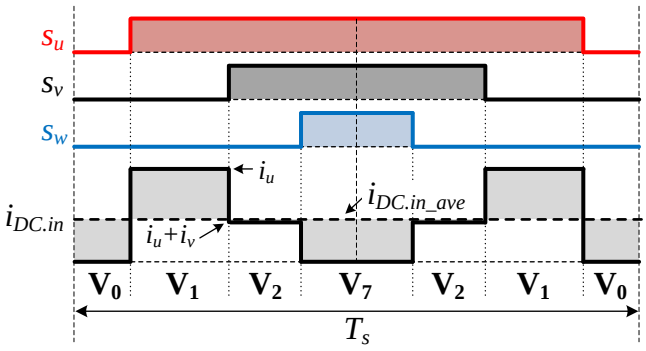
Fig. 3.2. Optimized combination of voltage space vectors for minimum rms value of dc-link current when i_u is positive and i_v and i_w are negative at m = 1.0, cos φ = 0.866 (30° lagging), and $2\pi ft$ = 25°.

3.2.2 At Low Modulation Indices Region

Fig. 3.3 shows the conventional SVPWM strategies and the zoomed-in waveforms of the dc-link current at the modulation index of 0.7, the load power factor of 0.866, and the phase angle of 25°. In this case, the largest difference between the instantaneous and the average values of the dc-link current occurs when the active voltage space vector of $\mathbf{V_1}$ is applied.



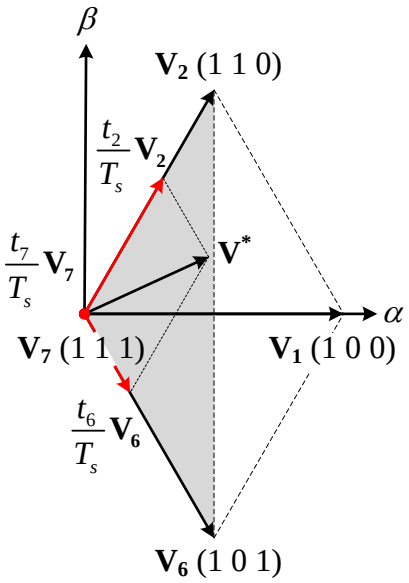
(a) Combination of voltage space vectors.



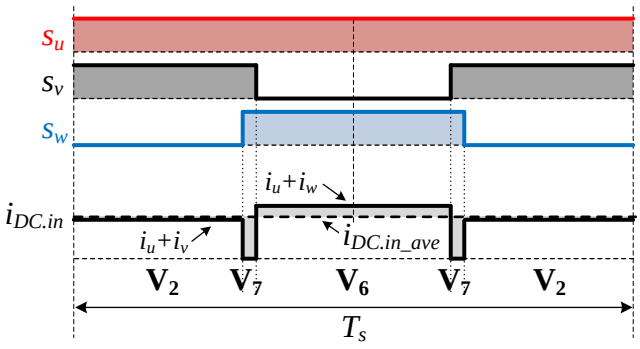
(b) Zoomed-in waveform of dc-link current.

Fig. 3.3. Conventional SVPWM strategies and zoomed-in waveforms of dc-link current at m = 0.7, cos φ = 0.866 (30° lagging), and $2\pi ft$ = 25°.

Fig. 3.4 shows the optimized combination of the voltage space vectors to minimize the rms value of the dc-link current at the modulation index of 0.7, the load power factor of 0.866, and the phase angle of 25°, and when the phase currents i_u is positive, i_v and i_w are negative. As shown in Fig. 3.4(a), one active vector ($\mathbf{V_6}$), one nonadjacent active vector ($\mathbf{V_2}$), and one zero vector ($\mathbf{V_7}$) are used to generate the reference vector [3-1]. Fig. 3.4(b) confirms that the dc-link capacitor current ripple is reduce with the combination of the voltage space vectors compared to those with the conventional SVPWM shown in Fig. 3.3(b). When the tip of the voltage reference vector belongs to the triangle formed by the tips of these three voltage space vectors ($\mathbf{V_6}$–$\mathbf{V_2}$–$\mathbf{V_7}$), i.e., at low-modulation indices, the use of the zero vector at each control period is unavoidable. However, the effect of the zero current on the dc-link current fluctuations around the average value is low at low-modulation indices because the difference between the zero current and the dc-link average current is small. On the other hand, as mentioned before, the largest difference between the dc-link current (= i_u) and the average value occurs when the active voltage space vector $\mathbf{V_1}$ is applied as shown in Fig 3.3(b). So, the active voltage space vector $\mathbf{V_1}$ that results in the largest difference between the dc-link current and the average value, when i_u is positive and i_v and i_w are negative, is avoided and $\mathbf{V_6}$ is alternatively selected for the minimum rms value of the dc-link current at low-modulation indices. In addition, only one zero vector of $\mathbf{V_7}$ is applied in this case, whereas the two zero vectors are applied in the conventional SVPWM. This is because the number of switching transitions are reduced by selecting only one zero vector ($\mathbf{V_7}$ (1 1 1)) of which switching states are similar to those of the other two active vectors ($\mathbf{V_6}$ (1 0 1), $\mathbf{V_2}$ (1 1 0)). Note that one of the two zero vectors ($\mathbf{V_0}$ or $\mathbf{V_7}$) is selected alternately in every 60° of the phase angle.



(a) Combination of voltage space vectors.



(b) Zoomed-in waveform of DC-link current.

Fig. 3.4. Optimized combination of voltage space vectors for minimum rms value of dc-link current when i_u is positive and i_v and i_w are negative at m = 0.7, cos φ = 0.866 (30° lagging), and $2\pi ft$ = 25°.

The selection of switching states in the proposed SVPWM switches from that shown in Figs. 3.2 and 3.4 by using the modulation index and the phase angle of the voltage references. First, due to that the loading condition is unknown, the loading condition is assumed to be high-modulation indices, i.e., the switching states shown in Fig. 3.2. Then, the duty cycles (t_6, t_1, t_2) of three consecutive active vectors, which are selected at high-modulation indices, are calculated. Next, following conditional expressions are calculated based on these duty cycles:

$$0 \le t_6, t_1, t_2 \le T_s. \quad \text{.....(3.1)}$$

If these conditional expressions are satisfied, three selected consecutive active vectors are directly used as shown in Fig. 3.2, i.e., the high-modulation indices. In contrast, if these conditional expressions are not satisfied, it means that the voltage reference vector is not to be generated by synthesizing three selected consecutive active vectors. So, the duty cycles of two nonadjacent active vectors and one zero vector, which are selected at low-modulation indices, are calculated and these voltage space vectors are used as shown in Fig. 3.4.

Note that the optimized selection of switching states in the proposed SVPWM at the load power factor of 0.866, i.e., high-load power factor, shown in Figs. 3.2 and 3.4 correspond to those of Ext-DCPWM [3-1].

In terms of the number of switching transitions, it is observed from Figs. 3.1 and 3.3 that the number of switching transitions in the conventional SVPWM is 6 per control period. On the other hand, Figs. 3.2 and 3.4 demonstrate that the number of switching transitions in the proposed SVPWM is 4 per control period due to smaller number of the applied voltage space vectors. Therefore, the proposed SVPWM leads to a higher inverter efficiency than that of the conventional SVPWM because one leg is clamped during each control period such as carrier-based DPWM.

3.2.3 Dead Time Error Compensation

Fig. 3.5 shows the dead time error voltage vector in the proposed SVPWM when the phase currents i_u and i_v are positive and i_w is negative at low-modulation indices. In practical, the duty cycles of each selected voltage space vector contain duty cycle errors due to the dead time t_d. With this duty cycle errors, the α-component ($v^*_{\alpha.error}$) and β-component ($v^*_{\beta.error}$) of the dead time error voltage vector are calculated as [3-5]

$$\begin{aligned} v^*_{\alpha.error} &= v_{a.\alpha}\frac{t_{a.dead}}{T_s} + v_{b.\alpha}\frac{t_{b.dead}}{T_s} + v_{c.\alpha}\frac{t_{c.dead}}{T_s} \\ v^*_{\beta.error} &= v_{a.\beta}\frac{t_{a.dead}}{T_s} + v_{b.\beta}\frac{t_{b.dead}}{T_s} + v_{c.\beta}\frac{t_{c.dead}}{T_s} \end{aligned} \quad \text{.....(3.2)}$$

where a–c represent the number of selected voltage space vectors, $v_{a–c.\alpha}$ and $v_{a–c.\beta}$ are the α-component and β-component of each selected voltage space vector, and $t_{a–c.dead}$ are the duty cycle error times of each selected voltage space vector due to the dead time. In the proposed SVPWM, the dead time error voltage is compensated with feedforward compensation by subtracting $v^*_{\alpha.error}$ and $v^*_{\beta.error}$ from the α-component (v^*_α) and β-component (v^*_β) of the voltage reference vector, respectively.

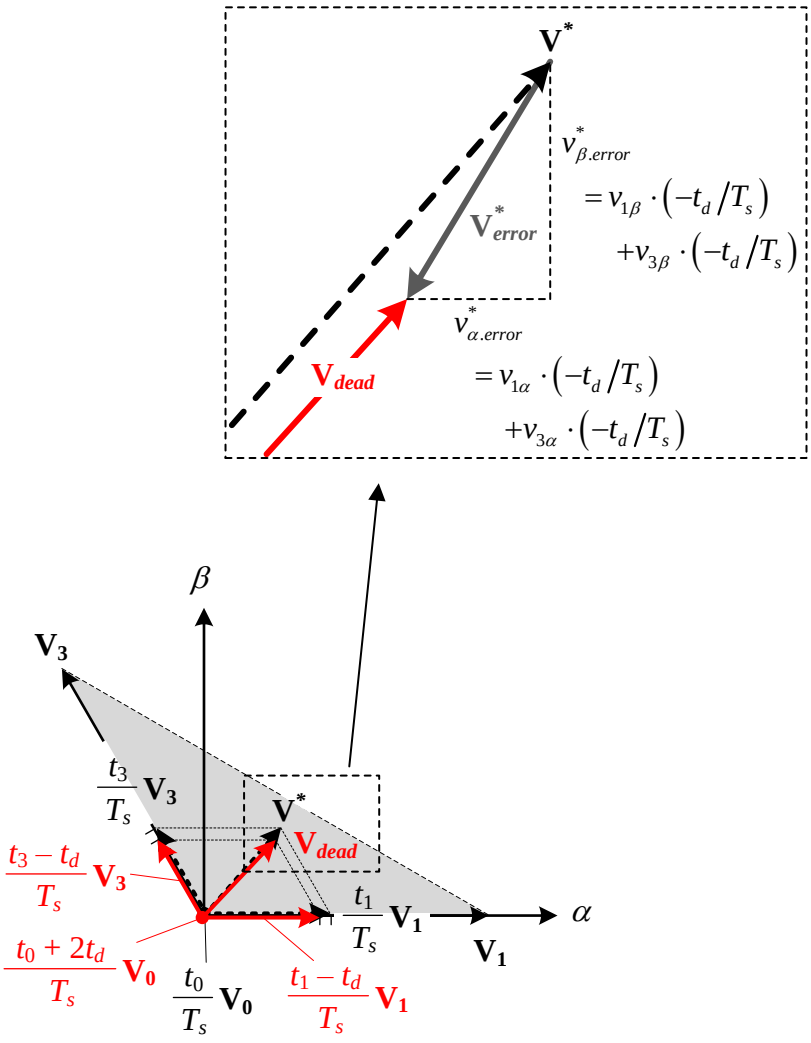


Fig. 3.5. Dead time error voltage vector in proposed SVPWM when i_u and i_v are positive and i_w is negative at low-modulation indices.

Table 3.1 lists the α-component and β-component of the dead time error voltage vector in the proposed SVPWM with regard to the load current conditions. The values of $v^*_{\alpha.error}$ and $v^*_{\beta.error}$ are dependent only on the dead time and the three-phase load currents directions. Therefore, only 6 patterns of the calculation for the dead time error voltages are necessary in advance.

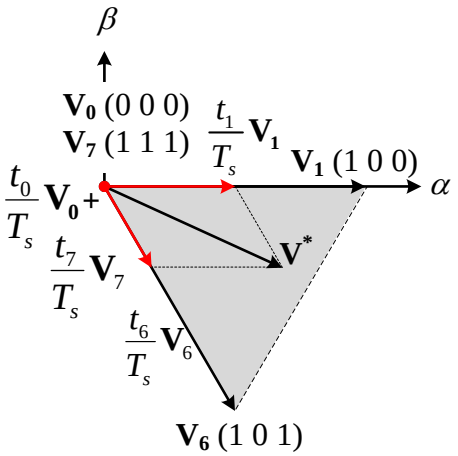
TABLE 3.1.
DEAD TIME ERROR VOLTAGE VECTOR COMPONENTS IN PROPOSED SVPWM WITH REGARD TO LOAD CURRENT CONDITIONS.

Current directions (P: Positive, N: Negative)			Dead time error voltage vector	
i_u	i_v	i_w	$v^*_{\alpha.error}$	$v^*_{\beta.error}$
P	N	N	$-4/3\times t_d/T_s$	0
P	P	N	$-2/3\times t_d/T_s$	$-2/\sqrt{3}\times t_d/T_s$
N	P	N	$2/3\times t_d/T_s$	$-2/\sqrt{3}\times t_d/T_s$
N	P	P	$4/3\times t_d/T_s$	0
N	N	P	$2/3\times t_d/T_s$	$2/\sqrt{3}\times t_d/T_s$
P	N	P	$-2/3\times t_d/T_s$	$2/\sqrt{3}\times t_d/T_s$

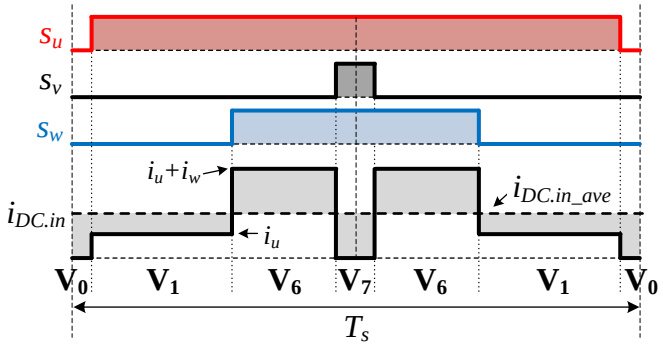
3.3. Problem with Conventional PWM Strategies to Reduce DC-link Capacitor Current Stress

Note that the previous chapter discussed the optimized selection of the switching states to reduce the dc-link capacitor current stress at the high-load power factor. However, the reduction effect on the rms value of the dc-link current through the use of these combinations of the voltage space vectors is dependent on the load power factor because the instantaneous value of the dc-link current is dependent on the output phase currents.

Fig. 3.6 shows the zoomed-in waveforms of the dc-link current at the modulation index of 1.0, the load power factor of 0.643 (50° lagging), and the phase angle of –25°, and when the phase currents i_u and i_w are positive, i_v is negative with the conventional SVPWM and the modified switching patterns ($\mathbf{V_2}$–$\mathbf{V_1}$–$\mathbf{V_6}$) shown in Fig. 3.2. Note that the modified switching patterns ($\mathbf{V_2}$–$\mathbf{V_1}$–$\mathbf{V_6}$) are the optimized results for the region when the phase currents i_u is positive, i_v and i_w are negative. If those switching patterns are applied to the regions with the different load current conditions as shown in Fig. 3.6(b), the dc-link capacitor current ripple worsen rather than improve compared to those with the conventional SVPWM. This is the critical problem of the conventional PWM strategies to reduce the dc-link capacitor current stress.

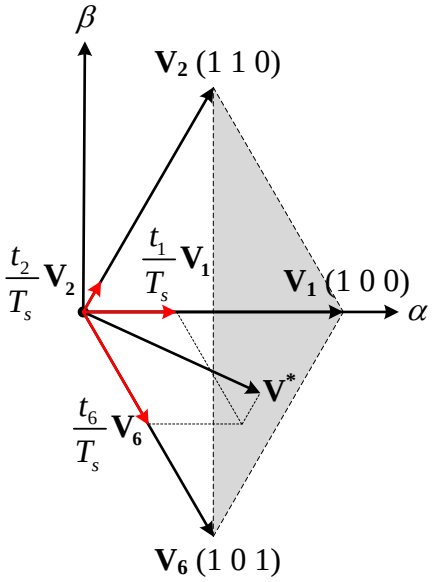


(i) Combination of voltage space vectors.

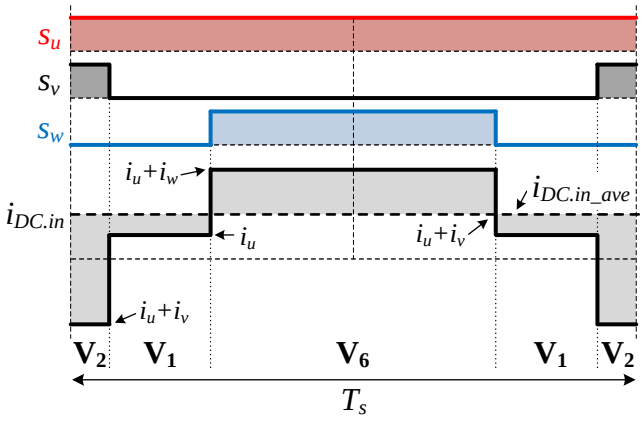


(ii) Zoomed-in waveform of dc-link current.

(a) Conventional SVPWM.



(i) Combination of voltage space vectors.



(ii) Zoomed-in waveform of dc-link current.

(b) Modified switching patterns ($\mathbf{V_2}$–$\mathbf{V_1}$–$\mathbf{V_6}$) shown in Fig. 3.2.

Fig. 3.6. Zoomed-in waveforms of dc-link current when i_u and i_w are positive, i_v is negative at m = 1.0, cos φ = 0.643 (50° lagging), and $2\pi ft$ = –25°.

3.4. Adaptation to Wide Load Power Factor Range using Load Current Sector

Due to the reason explained in previous chapter, it is necessary to deal with the variation of the load power factor to reduce the dc-link current stress over a wide power factor range, which is a typical requirement of the AC motor drive system.

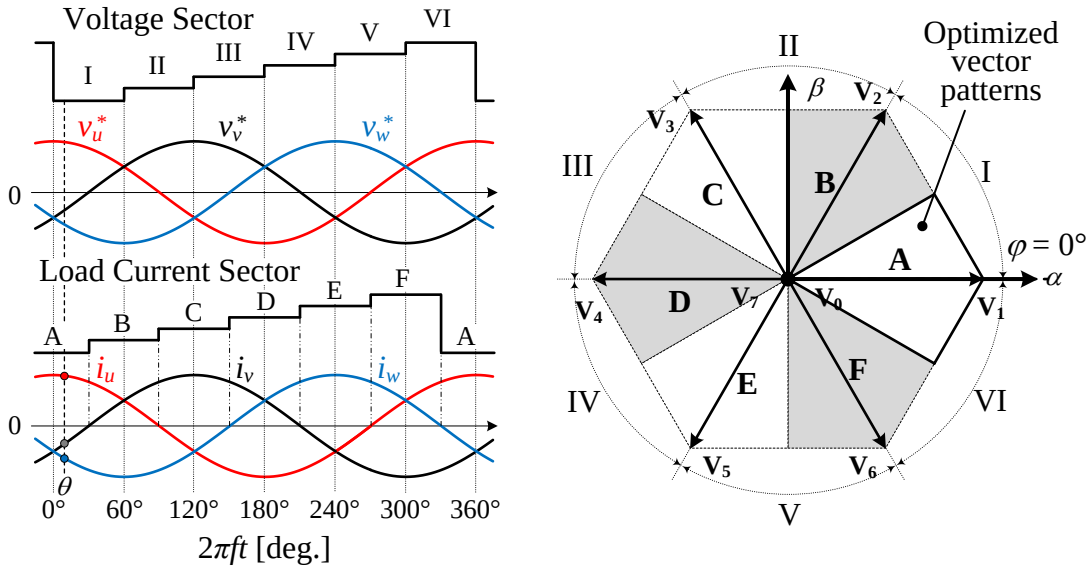
Table 3.2 lists the load current sector definitions. These sectors (A–F) are determined by the combination of the output phase current directions. With these load current sectors, the load current conditions are recognized.

Fig. 3.7 shows the layouts of the voltage sectors and the load current sectors in phase angle domain and $\alpha\beta$ reference frame at a unity load power factor. When i_u is positive and i_v and i_w are negative, i.e., at load current sector A, the dc-link current harmonics are minimized with optimized combinations of the voltage space vectors $\mathbf{V_6}$–$\mathbf{V_1}$–$\mathbf{V_2}$ or $\mathbf{V_6}$–$\mathbf{V_7}$–$\mathbf{V_2}$, as shown in Figs. 3.2 and 3.4, respectively. Fig. 3.7(b) demonstrates that the entire region of load current sector A is available with these optimized combinations of the voltage space vectors with a unity load power factor.

TABLE 3.2.
LOAD CURRENT SECTOR DEFINITIONS.

Load current sector	Current directions (P: Positive, N: Negative) i_u	i_v	i_w
A	P	N	N
B	P	P	N
C	N	P	N
D	N	P	P
E	N	N	P
F	P	N	P

Thus, optimized switching patterns for reduction of the dc-link current harmonics are applied over the entire phase angle region for the case $|\varphi| < 30°$, i.e., with a high-load power factor.

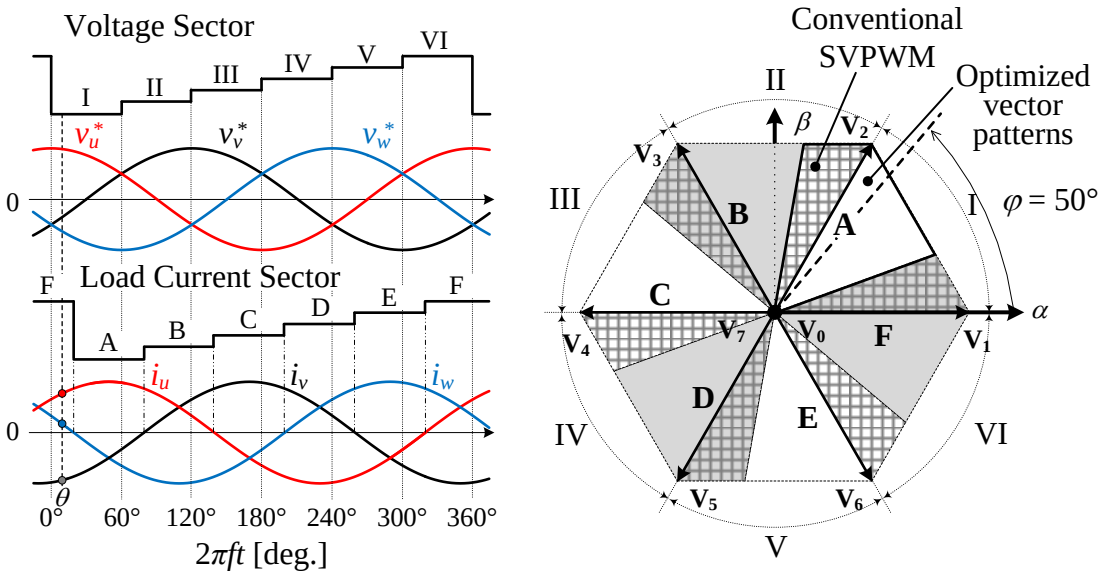


(a) In phase angle domain. (b) In $\alpha\beta$ reference frame.

Fig. 3.7. Layouts of voltage sectors and load current sectors at unity load power factor ($\varphi = 0°$).

Fig. 3.8 shows the layouts of the voltage sectors and the load current sectors at a load power factor of 0.643 (50° lagging), i.e., driving mode. When the load power factor is varied, the load current sectors shift according to the phase shift of the output phase currents. As a result, the polarity of i_v at the timing of the phase angle θ differs compared with that when the load power factor is unity, shown in Fig. 3.7(a). This leads to an increase of the dc-link current harmonics, even with the same optimized combinations of the voltage space vectors for a unity load power factor. In $\alpha\beta$ reference frame, the load current sectors are rotated by the phase shift angle φ as shown in Fig. 3.8(b), according to the variation of the load power factor. As shown by mesh area in Fig. 3.8(b), a part of the load current sector A is not available with the optimized combinations of the voltage space vectors ($\mathbf{V_6}$–$\mathbf{V_1}$–$\mathbf{V_2}$ or $\mathbf{V_6}$–$\mathbf{V_7}$–$\mathbf{V_2}$) for the load current sector A for $30° < |\varphi| < 90°$, i.e., low-load power

factor in driving mode. In these areas, new combinations of the voltage space vectors such as three consecutive voltage space vectors or two nonadjacent voltage space vectors with one zero vector, do not reduce the dc-link current harmonics but rather increase it. Hence, the conventional SVPWM is applied in these areas and the optimized combinations of the voltage space vectors are applied in other areas, which results in the minimum dc-link current harmonics, even when the load power factor is varied.

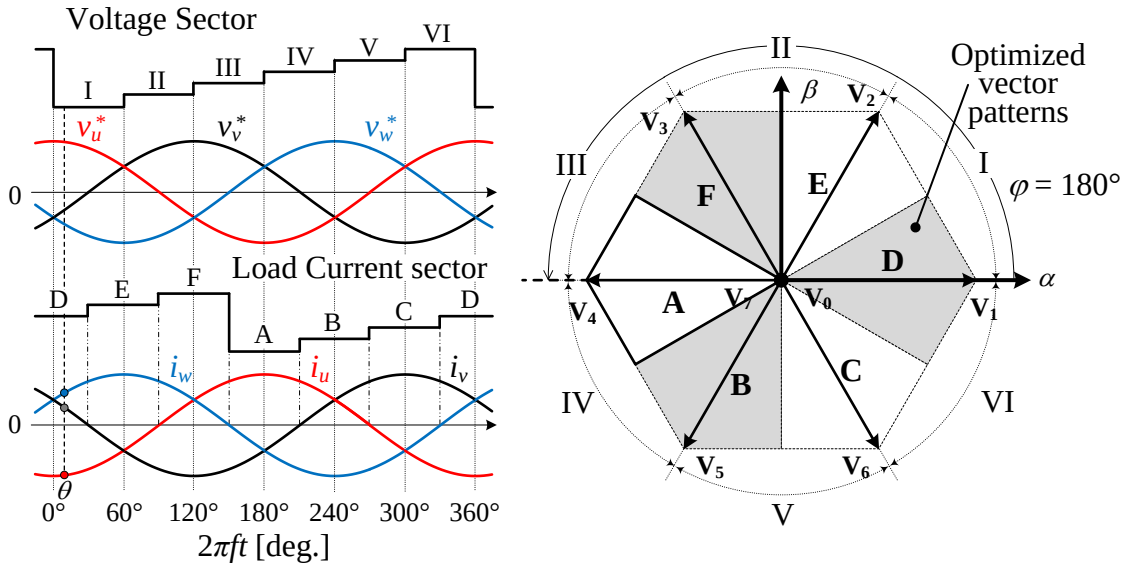


(a) In phase angle domain. (b) In $\alpha\beta$ reference frame.

Fig. 3.8. Layouts of voltage sectors and load current sectors at load power factor of 0.643 (50° lagging).

Fig. 3.9 shows the layouts of the voltage sectors and the load current sectors at a load power factor of –1.0 (180° lagging), i.e., regenerative braking mode. When the load power factor is –1.0, the polarities of all phase currents at the phase angle of θ reverse compared with that when the load power factor is unity, shown in Fig. 3.7(a). However, the absolute values are the same as those when the load power factor is unity. This leads to the same reduction effect on the dc-link current harmonics, even with the same optimized combinations of the voltage space vectors for a unity load power factor. Thus, the dc-link current harmonics are minimized in regenerative

braking mode as well as in driving mode. In $\alpha\beta$ reference frame, even though the load current sectors are rotated by 180° according to φ, the reduction of the dc-link current harmonics is possible. Note that the area of the load current sector A is no longer available with the optimized combinations of the voltage space vectors ($\mathbf{V_6}$–$\mathbf{V_1}$–$\mathbf{V_2}$ or $\mathbf{V_6}$–$\mathbf{V_7}$–$\mathbf{V_2}$) for load current sector A. Alternatively, the optimized combinations for sector A ($\mathbf{V_6}$–$\mathbf{V_1}$–$\mathbf{V_2}$ or $\mathbf{V_6}$–$\mathbf{V_7}$–$\mathbf{V_2}$) are effective in reducing the dc-link current harmonics for the load current sector D, which is an opposite side sector of the load current sector A, in regenerative braking mode. Thus, the optimized combinations of the voltage space vectors in regenerative braking mode are opposite to those in driving mode.



(a) In phase angle domain. (b) In $\alpha\beta$ reference frame.

Fig. 3.9. Layouts of voltage sectors and load current sectors at load power factor of –1.0 (180° lagging).

Table 3.3 lists the selected voltage space vectors to minimize the dc-link current harmonics for each combination of the voltage sector and the load current sector. The combinations of voltage space vectors in the white-colored cells represent the optimized combinations of the voltage space

vectors to minimize the dc-link current harmonics in driving mode. On the other hand, the voltage space vectors in the light-gray-colored cells represent the optimized combinations in terms of reducing the dc-link current harmonics in a regenerative braking mode. Furthermore, the combinations of the voltage space vectors in conventional SVPWM are listed in the gray-colored cells, i.e., the region where the dc-link current harmonics are not to be reduced with the proposed combinations of the voltage space vectors. Note that in the proposed SVPWM, the load power factor is indirectly detected only by the polarities of the output phase currents and the definition of the load current sectors. Therefore, the optimized combinations of the voltage space vectors to minimize the dc-link current harmonics under any conditions of the load power factor are simply employed.

TABLE 3.3.
SELECTED VOLTAGE SPACE VECTORS FOR MINIMUM DC-LINK CURRENT HARMONICS.

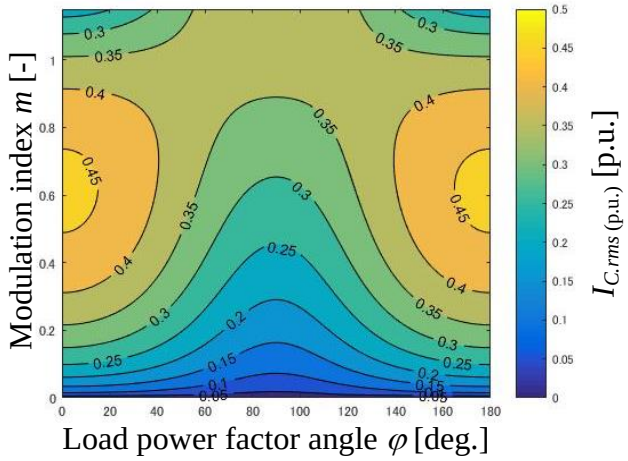
		Load Current Sector					
		A	B	C	D	E	F
Voltage Sector	I	V_6-V_1-V_2 or V_6-V_7-V_2	V_1-V_2-V_3 or V_1-V_0-V_3	V_0-V_1-V_2-V_7	V_6-V_1-V_2 or V_6-V_7-V_2	V_1-V_2-V_3 or V_1-V_0-V_3	V_0-V_1-V_2-V_7
	II	V_0-V_3-V_2-V_7	V_1-V_2-V_3 or V_1-V_0-V_3	V_2-V_3-V_4 or V_2-V_7-V_4	V_0-V_3-V_2-V_7	V_1-V_2-V_3 or V_1-V_0-V_3	V_2-V_3-V_4 or V_2-V_7-V_4
	III	V_3-V_4-V_5 or V_3-V_0-V_5	V_0-V_3-V_4-V_7	V_2-V_3-V_4 or V_2-V_7-V_4	V_3-V_4-V_5 or V_3-V_0-V_5	V_0-V_3-V_4-V_7	V_2-V_3-V_4 or V_2-V_7-V_4
	IV	V_3-V_4-V_5 or V_3-V_0-V_5	V_4-V_5-V_6 or V_4-V_7-V_6	V_0-V_5-V_4-V_7	V_3-V_4-V_5 or V_3-V_0-V_5	V_4-V_5-V_6 or V_4-V_7-V_6	V_0-V_5-V_4-V_7
	V	V_0-V_5-V_6-V_7	V_4-V_5-V_6 or V_4-V_7-V_6	V_5-V_6-V_1 or V_5-V_0-V_1	V_0-V_5-V_6-V_7	V_4-V_5-V_6 or V_4-V_7-V_6	V_5-V_6-V_1 or V_5-V_0-V_1
	VI	V_6-V_1-V_2 or V_6-V_7-V_2	V_0-V_1-V_6-V_7	V_5-V_6-V_1 or V_5-V_0-V_1	V_6-V_1-V_2 or V_6-V_7-V_2	V_0-V_1-V_6-V_7	V_5-V_6-V_1 or V_5-V_0-V_1

3.5. Analytical Evaluations

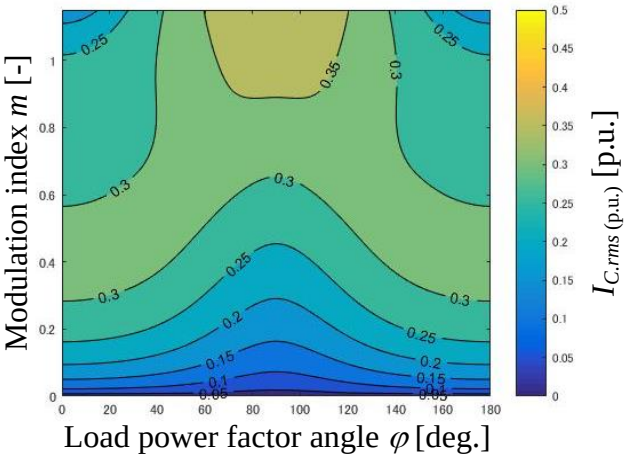
3.5.1 DC-link Capacitor RMS Current

In this chapter, the normalized dc-link capacitor rms current $I_{C.rms}$ (p.u.) which is calculated as (2.13) is used for the evaluation of dc-link capacitor current stress reduction with the proposed SVPWM.

Fig. 3.10 shows the analytical results of the rms value of dc-link capacitor current with regard to the modulation index and the load power factor angle. When the conventional SVPWM is applied, the maximum value of $I_{C.rms}$ (p.u.) is 0.459 p.u. at $|\cos \varphi| = 1.0$ and a modulation index of 0.62. On the other hand, when the optimized combinations of the voltage space vectors for reduction of the dc-link current harmonics are applied, the values of $I_{C.rms}$ (p.u.) at these points are reduced by 38.6%. Furthermore, it is demonstrated that the rms value of the dc-link capacitor current is reduced under any conditions of the load power factor and modulation index. A higher absolute value of the load power factor $|\cos \varphi|$ enables a greater reduction effect on the rms value of the dc-link capacitor current to be obtained. This is because the applied ratio of the optimized combinations of voltage space vectors becomes higher as $|\cos \varphi|$ becomes higher. The application ratio of the proposed switching patterns decreases with the smaller reduction effect on $I_{C.rms}$ (p.u.) as $|\cos \varphi|$ becomes small, and there is no $I_{C.rms}$ (p.u.) difference between conventional and proposed SVPWM when $\cos \varphi = 0$.



(a) Conventional SVPWM.



(b) Proposed SVPWM.

Fig. 3.10. Analytical results of dc-link capacitor rms current with regard to modulation index m and load power factor angle φ.

3.5.2 Load Current Quality

In order to evaluate the load current quality, the concept of harmonic flux [3-6] is used. Assuming that the motor switching frequency model is an inductance L, a harmonic flux load current vector $\mathbf{I_h}$ has a proportional relationship between the harmonic flux vector $\boldsymbol{\lambda}_\mathbf{h}$, which is calculated as time integral of the instantaneous error voltage vector, as

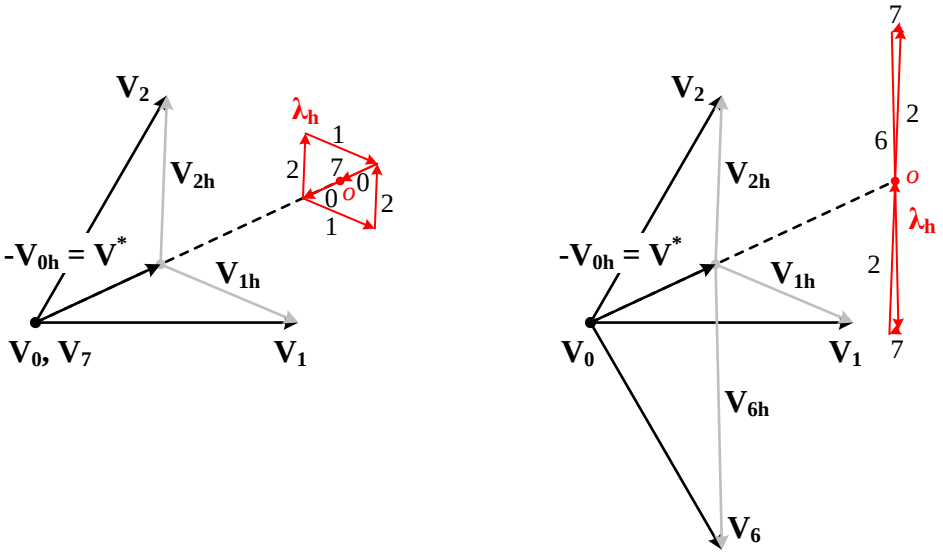
$$\boldsymbol{\lambda}_\mathbf{h} = L\mathbf{I}_\mathbf{h} = \int_{NT_s}^{(N+1)T_s} \left(\mathbf{V}_\mathbf{k} - \mathbf{V}^*\right) \cdot dt. \quad \text{.....(3.3)}$$

Fig. 3.11 shows an example of the harmonic flux trajectories at the modulation index of 0.7 and the phase angle of 25°, same conditions as in Figs. 3.3 and 3.4. The calculation of (3.3) and Fig. 3.11 evaluate and visualize the ripple current on a per-carrier cycle base. The distance between the harmonic flux trajectories and the origin o, which is the initial value of $\boldsymbol{\lambda}_\mathbf{h}$ at the beginning of the carrier cycle, is equal to the magnitude of the harmonic flux. Therefore, Fig. 3.11 demonstrates that the optimized vector combinations for the minimum rms value of the dc-link capacitor current worsen the load current quality compared to those with the conventional SVPWM. Since the voltage space vectors which are symmetric with regard to every 60° of phase angle are applied in the modern PWM strategy for three-phase system, the harmonic flux vector characteristic has six-fold space symmetry. So, the rms value of the harmonic flux over fundamental period λ_{rms}, which characterizes the load current quality and the harmonic losses in the test motor, is calculated as follows:

$$\lambda_{rms} = \sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}}\int_{NT_s}^{(N+1)T_s} \left\|\boldsymbol{\lambda}_\mathbf{h}\right\|^2 \cdot dt.d\theta.} \quad \text{.....(3.4)}$$

Fig. 3.12 shows the harmonic flux rms values with the conventional SVPWM and the proposed SVPWM. Fig. 3.12 demonstrates that the proposed SVPWM worsens the harmonic flux rms values compared to those obtained with the conventional SVPWM. The reason is because the proposed SVPWM results in the application of the voltage space vector which is not

the closest to $\mathbf{V}^*$, i.e., $\mathbf{V_6}$ in Fig. 3.11.



(a) Conventional SVPWM. (b) Proposed SVPWM.

Fig. 3.11. Harmonic flux trajectories at m = 0.7 and $2\pi ft$ = 25°. The distance between the origin (o) and the trajectory of $\boldsymbol{\lambda_h}$ is equal to the magnitude of the harmonic flux, and continuously fluctuates.

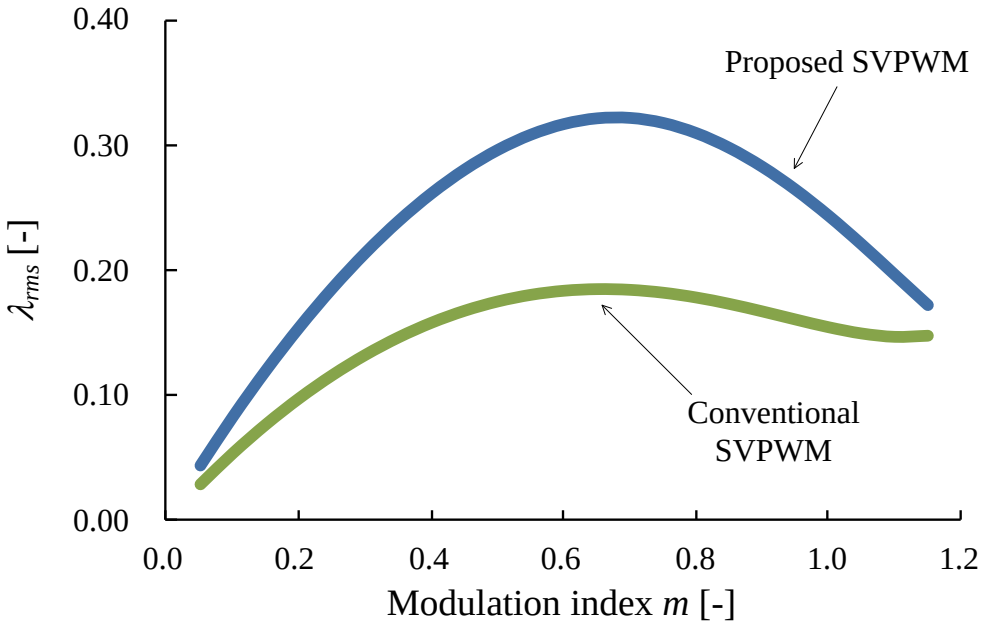


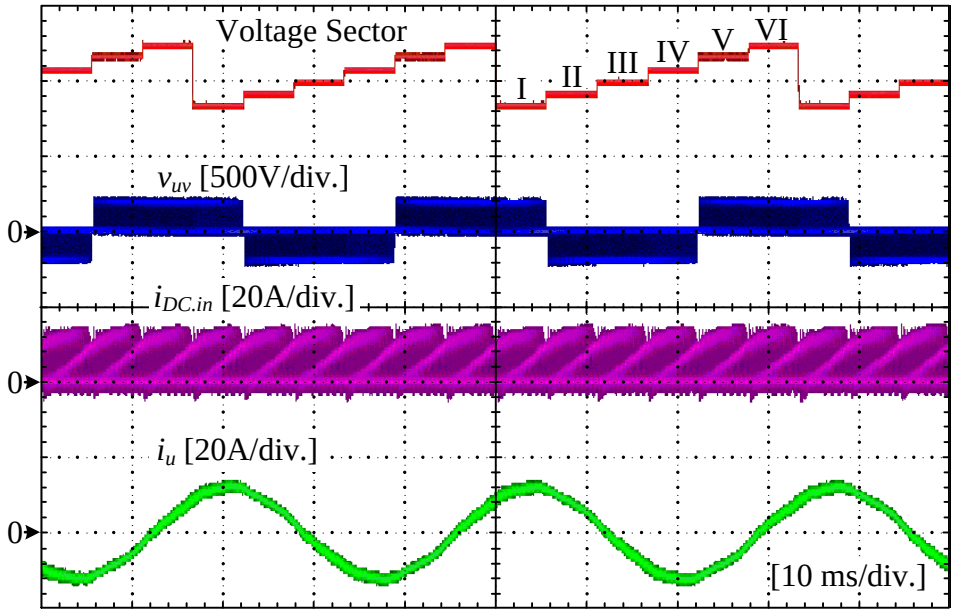
Fig. 3.12. Comparison of harmonic flux rms values with regard to modulation index. In the proposed SVPWM calculations, the load power factor is set to 1.

3.6. Simulation and Experimental Results

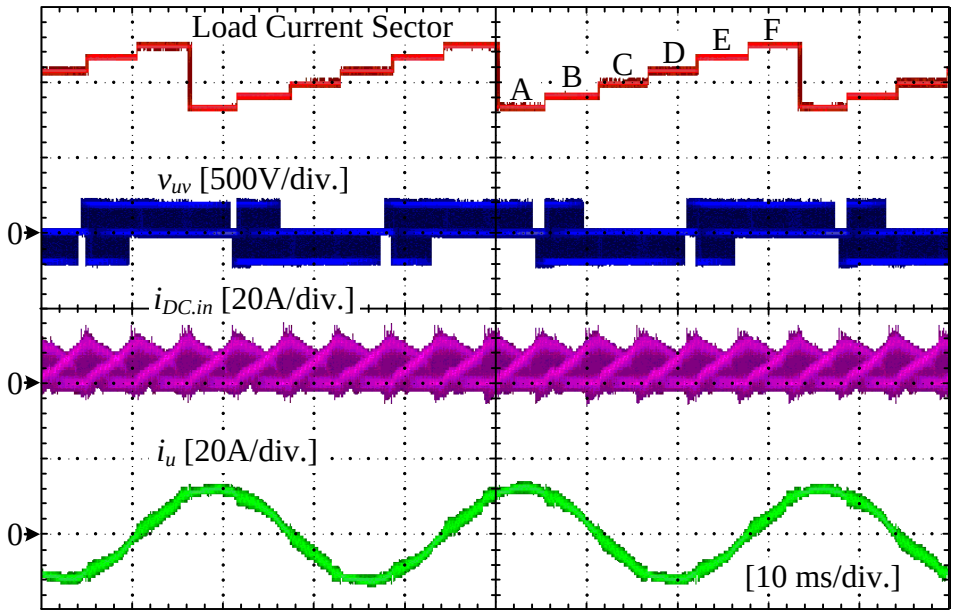
The effectiveness of the proposed SVPWM was verified by the PLECS simulation and the experiment. In the experiment, the three-phase 2-level VSI, composed of IGBT power module (7MBP50RA120, Fuji Electric Co., Ltd.), was operated at the switching frequency of 10 kHz with the dead time of 4 μs (4% of the control period). A three-phase induction motor (MVK8115A-R, Fuji Electric Co., Ltd.) with a rated power of 3.7 kW was used as the test motor and controlled by V/f control with the conventional and proposed SVPWM, which are implemented into an evaluation board (TMS320C6713, Texas Instruments). The load power factor was varied by controlling the torque reference of the load motor.

3.6.1. DC-link Current Harmonics

Fig. 3.13 shows the operating waveforms of the VSI with the conventional and proposed SVPWM at a modulation index of 0.705 and a load power factor of 0.866 (φ = 30°), i.e., driving mode with a high-load power factor. When the load power factor is high, the applied ratio of the proposed SVPWM is also high. In particular, the proposed SVPWM is applied at all times with a load power factor of 0.866 (φ = 30°). The results in Fig. 3.13 demonstrate that the width of the envelope in the dc-link current is reduced by the application of the proposed SVPWM. On the other hand, the output phase current with the proposed SVPWM seems to be slightly distorted than that with the conventional SVPWM. Furthermore, the transitions between $+E_{dc}$ to $-E_{dc}$ occur in the line-to-line voltage with the proposed SVPWM. This is because three voltage space vectors, which are not the closest to the voltage reference vector, are used to minimize the dc-link current harmonics in the proposed SVPWM. Note that the averaged line-to-line voltages are sinusoidal waveforms even though such transitions occur.



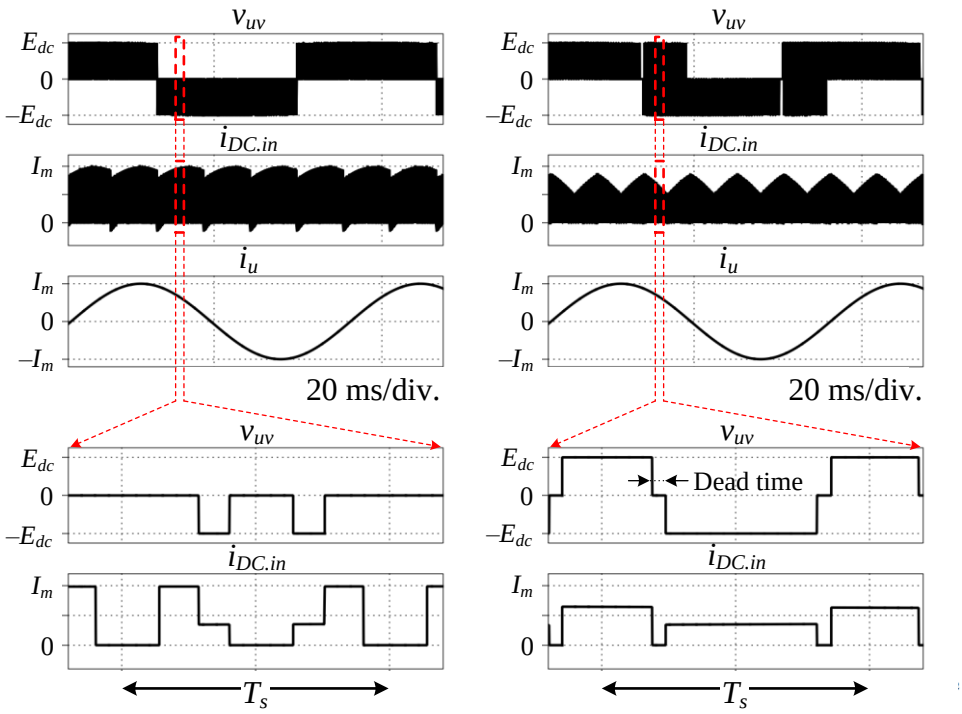
(a) Conventional SVPWM.



(b) Proposed SVPWM.

Fig. 3.13. Experimental waveforms at m = 0.705 and cos φ = 0.866 (30° lagging), i.e., driving mode with high-load power factor; voltage or load current sector, output line-to-line voltage, dc-link current, and u-phase output current.

Fig. 3.14 shows the PLECS simulation results with each modulation method at the modulation index of 0.705 and the load power factor of 0.866 (φ = 30°), same conditions of the experiments in Fig. 3.13. The zoomed-in waveforms of the dc-link current demonstrate that the width of the step change is reduced by the proposed SVPWM. Furthermore, the zoomed-in waveforms of the line-to-line voltage demonstrate that the instantaneous voltage transition between $+E_{dc}$ to $-E_{dc}$ never occurs due to the dead-time period. Therefore, the proposed SVPWM does not increase the motor surge voltage, which is proportional to *dv/dt* of the motor terminal voltage.



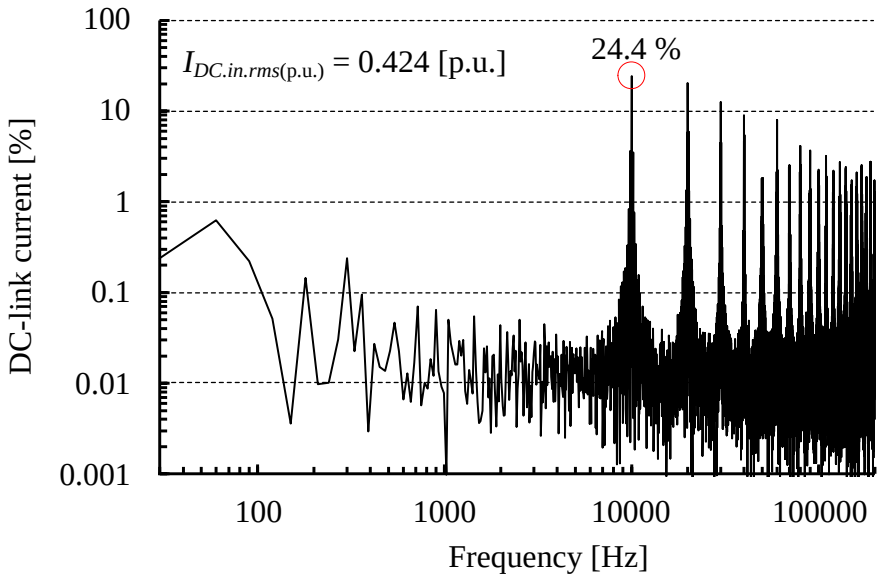
(a) Conventional SVPWM. (b) Proposed SVPWM.

Fig. 3.14. PLECS simulation results with each modulation method at m = 0.705 and cos φ = 0.866 (30° lagging) (under same conditions of experiments in Fig. 3.13).

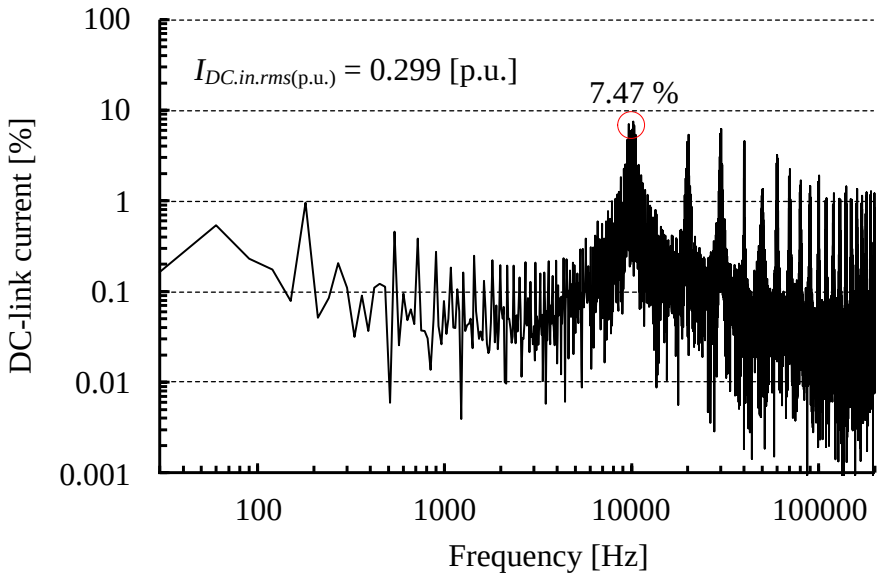
Fig. 3.15 shows the harmonic components of the dc-link current under the same conditions as in Fig. 3.13. The maximum value of the vertical axis (100%) indicates the maximum value of the output phase current. When the conventional SVPWM is applied, the dc-link current contains high integer multiples of the switching frequency, the maximum value of which is 24.4%. Application of the proposed SVPWM reduced the switching frequency component by 7.47%. In this research, the experimental results of the dc-link current harmonics are estimated as the ratio between the rms value of the dc-link current and the amplitude of the output phase current as

$$I_{DC.in.rms(\text{p.u.})} = \frac{1}{I_m}\sqrt{\sum_{n=1}\left(\frac{1}{\sqrt{2}} i_{DC.in.n}\right)^2} \quad \text{.....(3.5)}$$

where n is the harmonic order and $i_{DC.in.n}$ is the n-order component of the dc-link current harmonics. The fundamental component of the dc-link current harmonic is 50 Hz at the rated load. The harmonic components of the dc-link current up to 20th order of the switching frequency are considered in this evaluation. The dc-link current harmonics $I_{DC.in.rms(\text{p.u.})}$ was significantly reduced by 0.299 p.u. when the proposed SVPWM was applied. On the other hand, there are higher low-order harmonics of the dc-link current than those with the conventional SVPWM. This is because the distortions of the output phase current with the proposed SVPWM, which is observed from Fig. 3.13, also appear in the dc-link current due to the fact that the dc-link current is the superposition summation of the switched current pulses from each phase leg. However, even though the proposed SVPWM worsened the low-order harmonics of the dc-link current, the values of those are less than 1% of the rated value. Therefore, the worse low-order harmonics of the dc-link current with the proposed SVPWM are not problem.



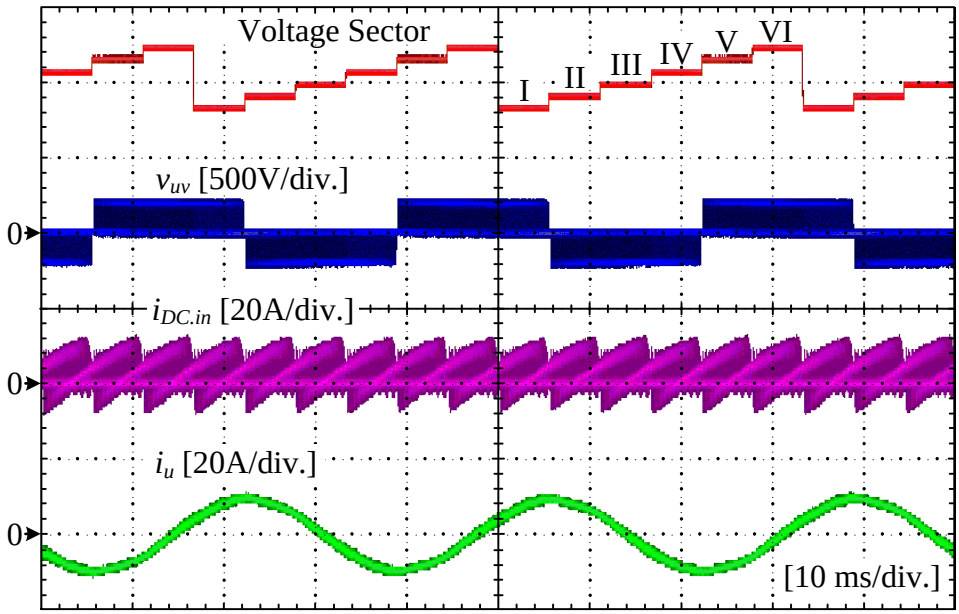
(a) Conventional SVPWM.



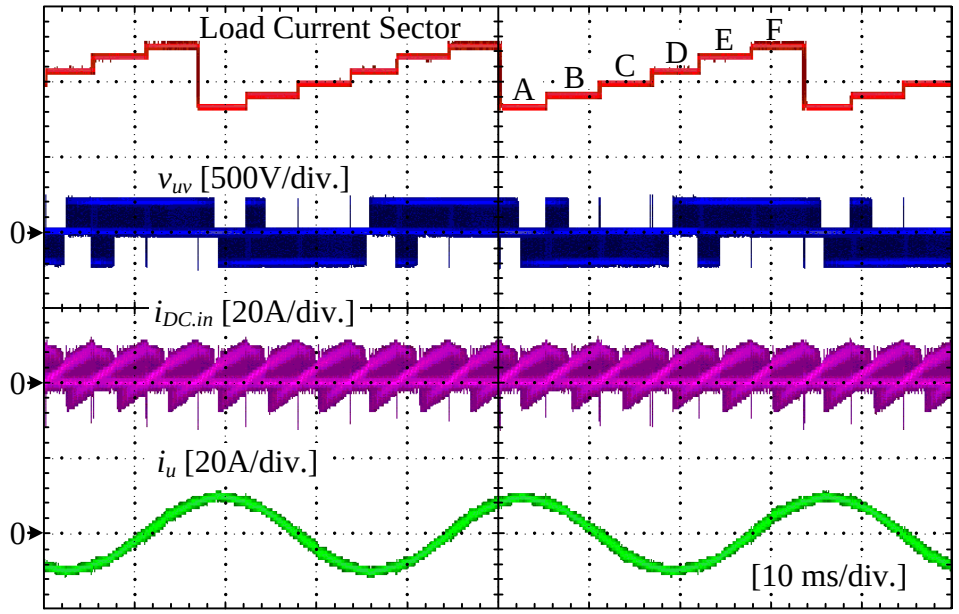
(b) Proposed SVPWM.

Fig. 3.15. Harmonic components of dc-link current at m = 0.705 and cos φ = 0.866 (30° lagging), i.e., driving mode with high-load power factor (under same conditions as in Fig. 3.13).

Figs. 3.16–3.17 show the VSI operating waveforms and the harmonic components of the dc-link current at the modulation index of 0.705 and the load power factor of 0.707 (φ = 45°), i.e., driving mode with a low-load power factor. When the load power is low, both the conventional SVPWM and proposed SVPWM are applied. In particular, the proposed SVPWM is applied within only three-quarters of the entire phase angle region, whereas the conventional SVPWM is applied in the other region at a load power factor of 0.707 (φ = 45°). Fig. 3.16 demonstrates that the width of the envelope in the dc-link current is partially reduced when the proposed SVPWM is applied. When the conventional SVPWM is applied under this low-load power factor condition, the twice switching frequency component of the dc-link harmonics becomes a maximum, the value of which is 22.4%. This value is reduced by 10.6% when the proposed SVPWM is applied. These results demonstrate that the proposed SVPWM is effective in reducing the dc-link current harmonics, even when the load power factor is low.

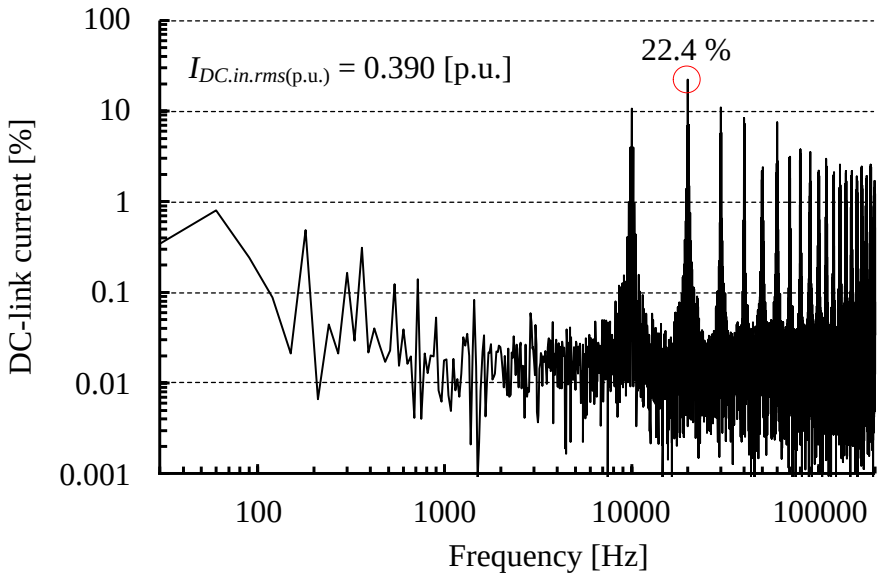


(a) Conventional SVPWM.

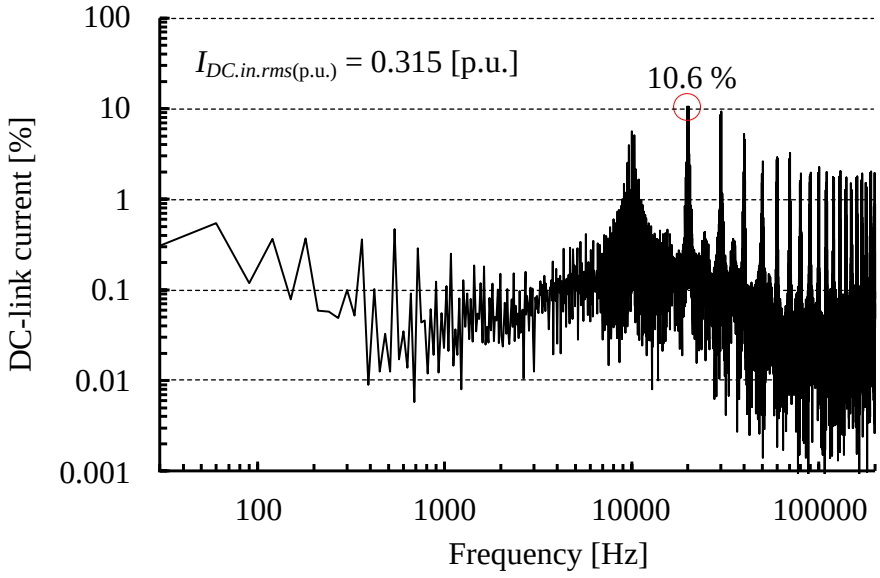


(b) Proposed SVPWM.

Fig. 3.16. Experimental waveforms at m = 0.705 and cos φ = 0.707 (45° lagging), i.e., driving mode with low-load power factor; voltage or load current sector, output line-to-line voltage, dc-link current, and u-phase output current.



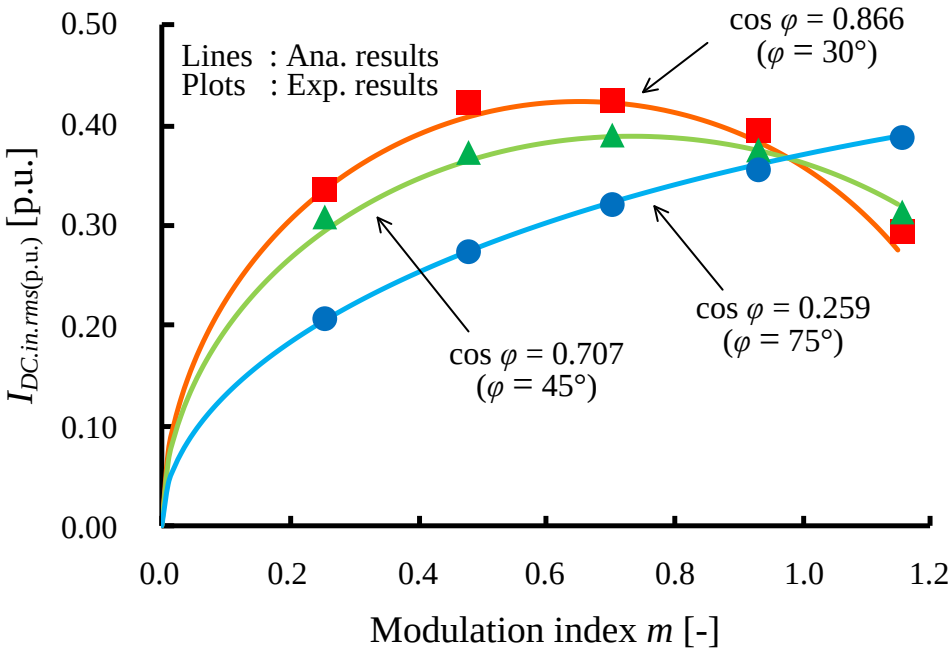
(a) Conventional SVPWM.



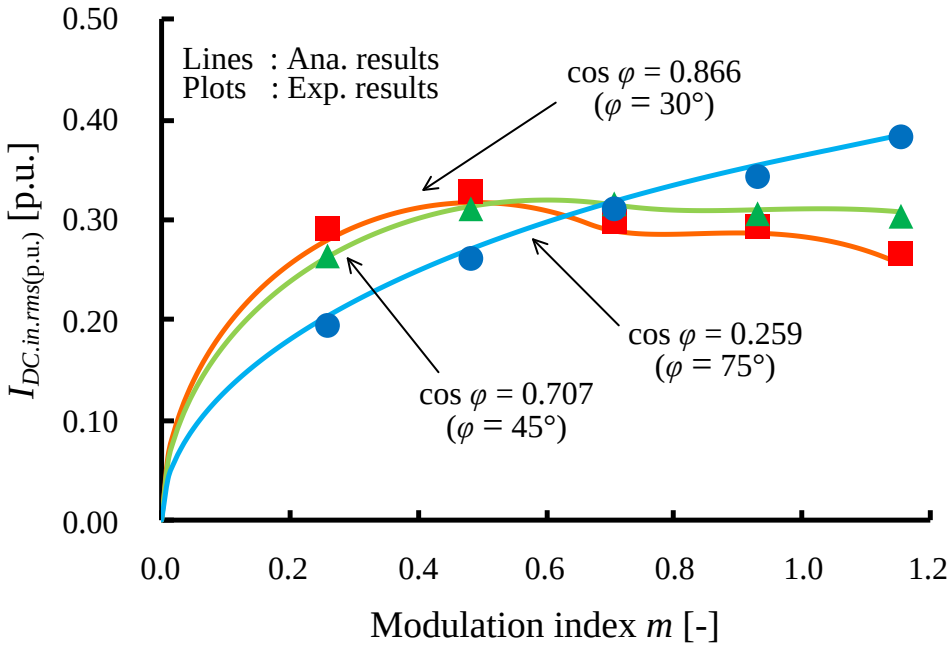
(b) Proposed SVPWM.

Fig. 3.17. Harmonic components of dc-link current at m = 0.705 and cos φ = 0.707 (45° lagging), i.e., driving mode with low-load power factor (under same conditions as in Fig. 3.16).

Fig. 3.18 shows the measured dc-link current harmonics in driving mode. The dc-link current harmonics are reduced under any load power factor and modulation index conditions in driving mode. It is also confirmed that as the load power factor becomes higher, the dc-link current harmonics-reduction effect of the proposed SVPWM increases. This trend is resulted from the relationship between φ and the application ratio of the proposed voltage space vector combinations in whole phase range, observed in Fig. 3.10.



(a) Conventional SVPWM.

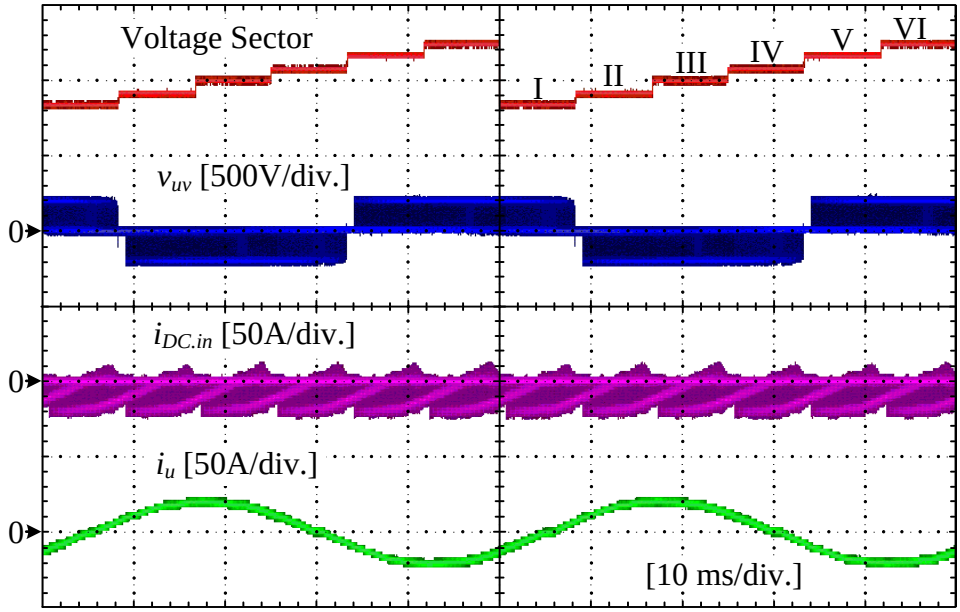


(b) Proposed SVPWM.

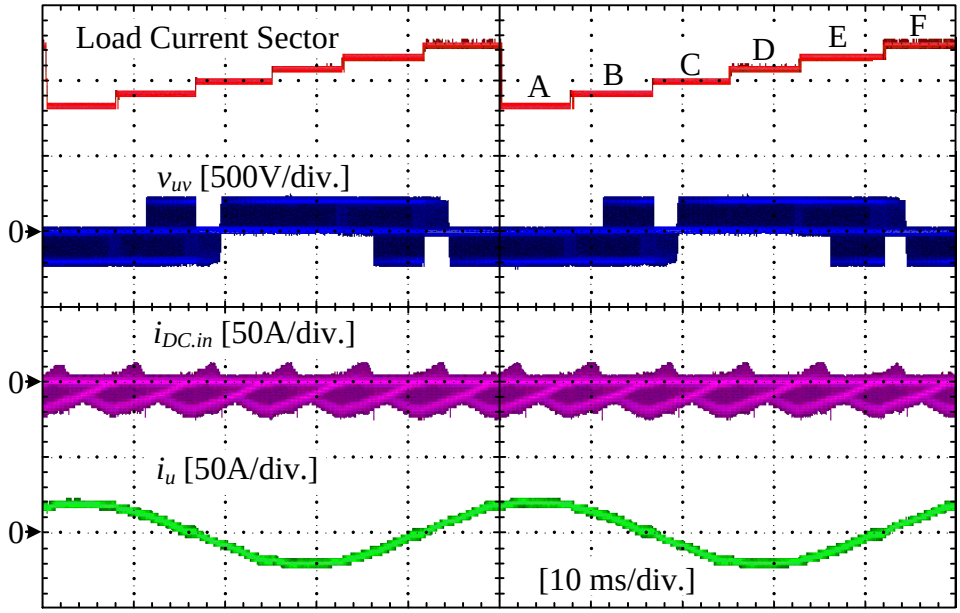
Fig. 3.18. Measured dc-link current harmonics in driving mode.

Figs. 3.19–3.20 show the VSI operating waveforms and the harmonic components of the dc-link current at the modulation index of 0.481 and the load power factor of –0.588 ($\varphi = 126°$), i.e., regenerative braking mode. Even in regenerative braking mode, the proposed SVPWM is also effective in reducing the width of the envelope in the dc-link current, which results in a reduction of the dc-link current harmonics. When the conventional SVPWM is applied, the maximum value of the switching frequency component of the dc-link current harmonics is 25.8% and the dc-link current harmonics is 0.335 p.u. Fig. 3.20 demonstrates that the switching frequency component is reduced by 10.7% and the dc-link current harmonics is reduced by 0.293 p.u. by the application of the proposed SVPWM, even in a regenerative braking mode.

The simulation and experimental results in Figs. 3.13–3.20 verify that the proposed SVPWM is effective in reducing the dc-link current harmonics for a motor drive system, which has a considerably wide variation of the load power factor.

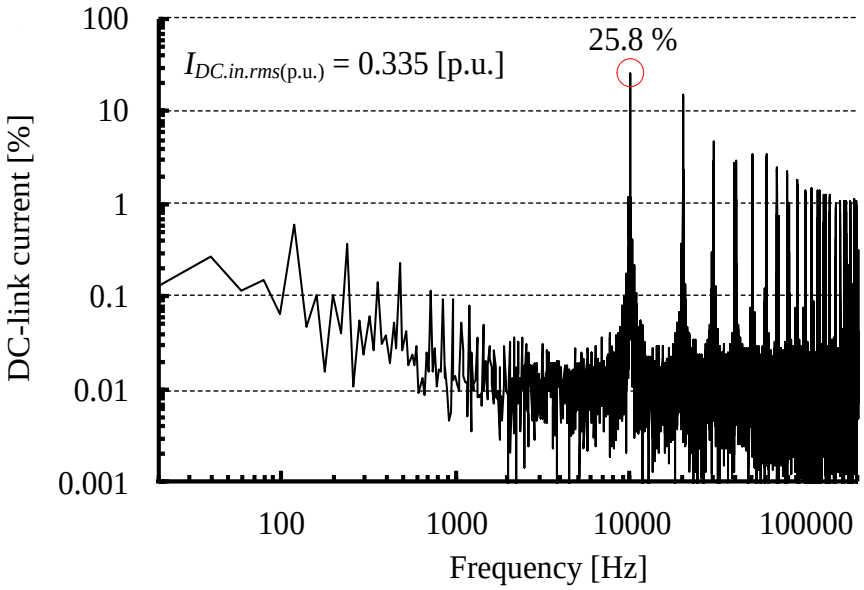


(a) Conventional SVPWM.

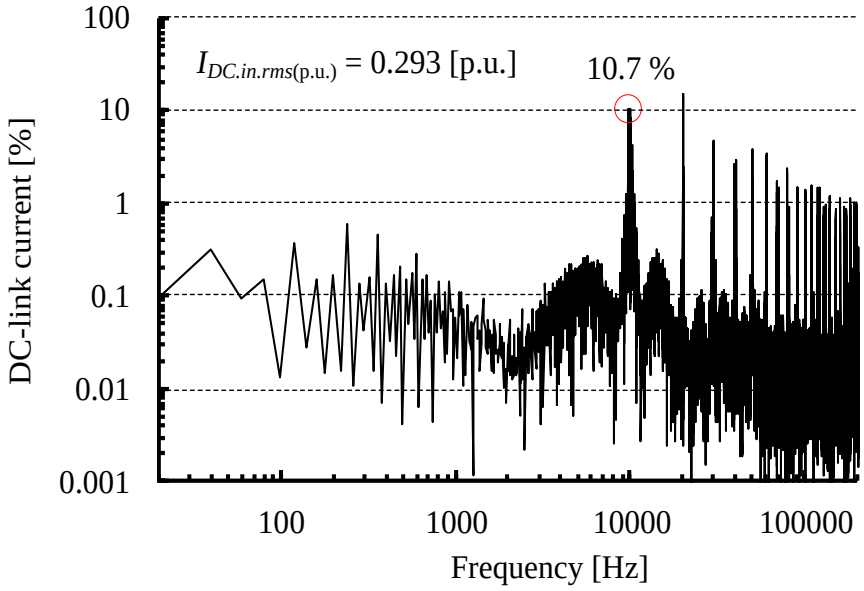


(b) Proposed SVPWM.

Fig. 3.19. Experimental waveforms at m = 0.481 and cos φ = –0.588 (126° lagging), i.e., regenerative braking mode; voltage or load current sector, output line-to-line voltage, dc-link current, and u-phase output current.



(a) Conventional SVPWM.



(b) Proposed SVPWM.

Fig. 3.20. Harmonic components of dc-link current at m = 0.481 and cos φ = –0.588 (126° lagging), i.e., regenerative braking mode (under same conditions as in Fig. 3.19).

3.6.2. Output Phase Current Harmonics

Fig. 3.21 shows the total harmonic distortion (THD) of the *u*-phase output current at a load power factor of 0.866. Harmonic components of not switching frequency components but up to the 40th order of the fundamental frequency component are considered in this evaluation. Note that the dead time error voltage, which is compensated both in the conventional and proposed SVPWM, is estimated from the duty cycle errors due to the dead time in each sector, as shown in Fig. 3.5. Fig. 3.21 confirms that the THD of the output phase current obtained with the proposed SVPWM is slightly higher than that obtained with the conventional SVPWM except for the low value of a modulation index.

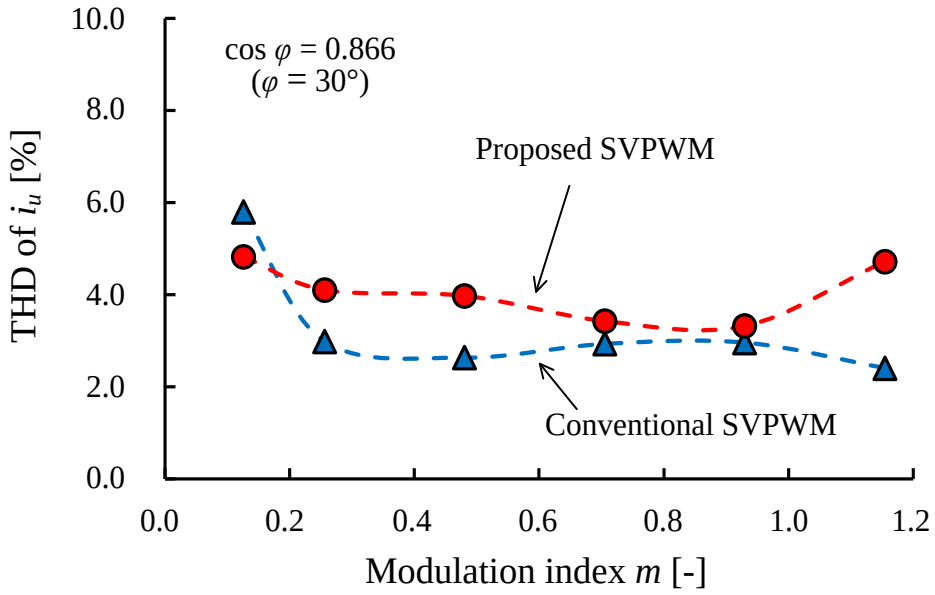


Fig. 3.21. Total harmonic distortion (THD) of *u*-phase output current at cos φ = 0.866 (30° lagging).

Fig. 3.22 shows the equivalent modulating signals and its harmonic contents at the modulation index of 0.705 and the load power factor of 0.866. It is clear that the modulating signals of the proposed SVPWM has a larger triplen harmonic than those of the conventional SVPWM because of the applied optimized combinations of the voltage space vectors for the minimum rms value of the dc-link capacitor current. These increased triplen harmonics of the modulating signals generate the larger baseband harmonics, the first carrier sidebands, in the line-to-line voltage of VSI [3-7]. As a result, the baseband harmonics of the output phase current are also distorted with the proposed SVPWM. In addition, in the proposed SVPWM, the detected polarities of the output phase currents are required in order to determine the load current sectors (A–F) according to Table 3.2. Therefore, the current detection error around zero-current-crossing points causes an incorrect selection of the voltage space vectors, and worsens the THD of the output phase current. A drawback of the proposed strategy is the worse output phase current THD which might cause an increase of the iron loss in the load motor.

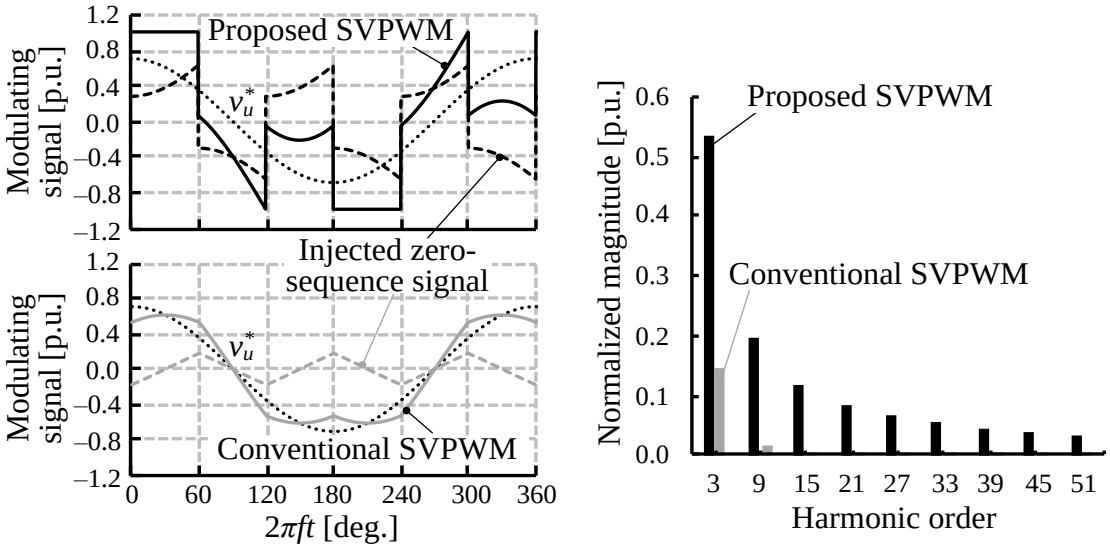


Fig. 3.22. Equivalent modulating signals and its harmonic contents at m = 0.705 and cos φ = 0.866 (30° lagging).

3.6.3. Inverter Efficiency

Fig. 3.23 shows the inverter efficiency between the conventional SVPWM and the proposed SVPWM at the load power factor of 0.866. The inverter efficiency was measured using Yokogawa WT1800 power analyzer. The proposed SVPWM leads to a high inverter efficiency compared to that with the conventional SVPWM due to its less number of switching transitions, which is reduced to two-thirds compared with the conventional SVPWM.

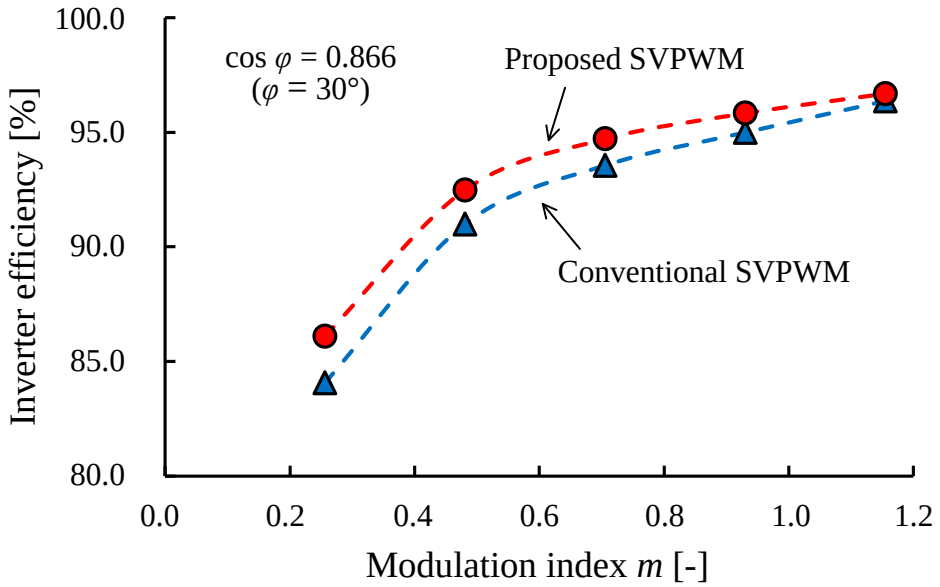


Fig. 3.23. Inverter efficiency comparison between conventional SVPWM and proposed SVPWM against different modulation index at cos φ = 0.866 (30° lagging).

3.6.4. DC-link Film Capacitor Heating

Fig. 3.24 shows the experimental setup to evaluate the dc-link film capacitor heating. The dc-link film capacitor and the inverter are placed inside thermally-insulated container (EPFH-125-2S, ISUZU), whereas the temperature test starts from 25.0℃.

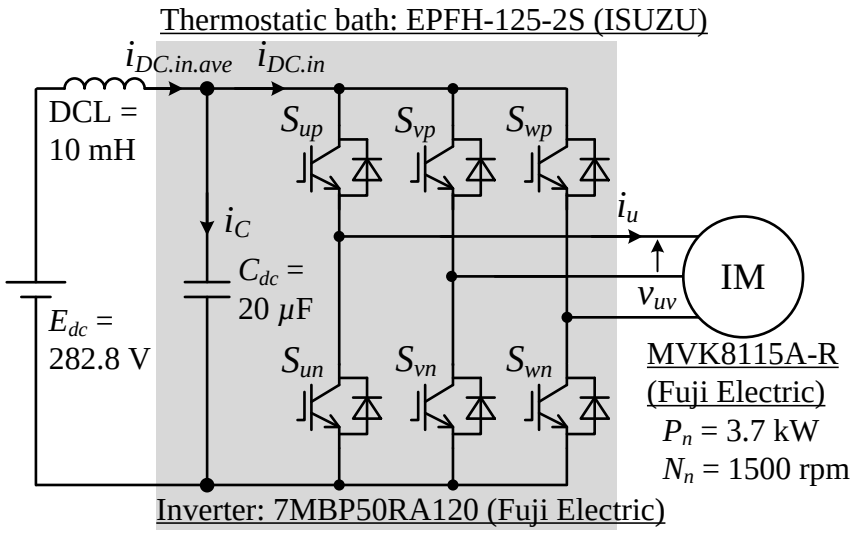
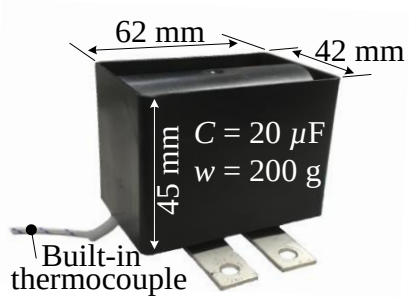
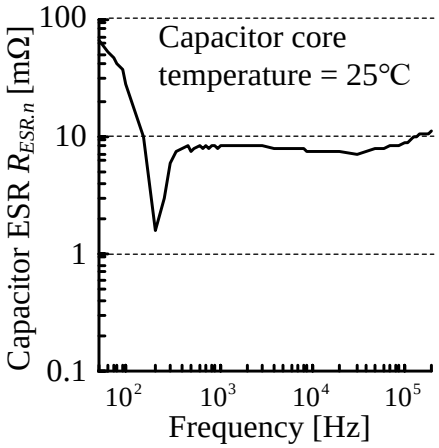


Fig. 3.24. Experimental setup to evaluate dc-link film capacitor heating.

Fig. 3.25 shows the film capacitor under test as the dc-link capacitor. The thermocouple is built in the central part of the film capacitor. An equivalent series resistance (ESR) is measured using HIOKI 3532-50 LCR tester. At very low frequencies, the ESR is high due to prevalent leakage. At low frequencies, ESR is dominated by the dielectric losses which decrease in inverse proportion to the frequency. At medium to high frequencies, the losses in the conductors are dominant and ESR becomes relatively constant. At high frequencies, ESR increases again due to the skin effect [3-8].



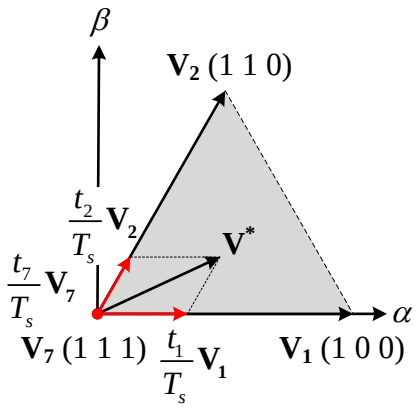
(a) Photograph of film capacitor.



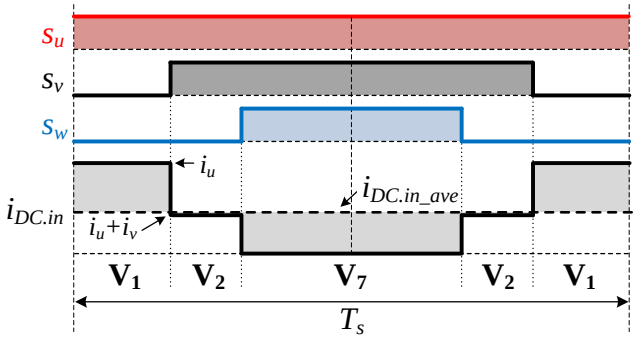
(b) Measured ESR.

Fig. 3.25. Film capacitor under test.

Fig. 3.26 shows the modified conventional SVPWM strategy. In order to evaluate the dc-link capacitor heating which is influenced by only the PWM-induced dc-link capacitor current, it is necessary to neglect the inverter loss difference with the conventional and proposed SVPWM. However, the conventional SVPWM leads to the worse inverter loss compared to those with the proposed SVPWM due to its number of switching transitions as shown in Fig. 3.23. So, in this evaluation, only one zero vector is applied during each control period in the conventional SVPWM in order to achieve the same number of switching transitions as the proposed SVPWM.



(a) Combination of voltage space vectors.

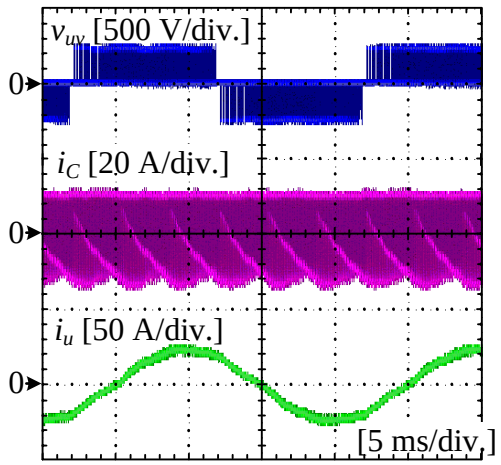


(b) Zoomed-in waveform of dc-link current.

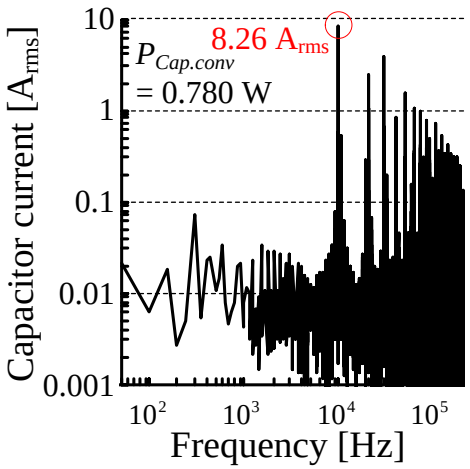
Fig. 3.26. Modified conventional SVPWM strategy and zoomed-in waveform of dc-link current at m = 0.7, cos φ = 0.866 (30° lagging), and $2\pi ft$ = 25°.

Figs. 3.27–3.28 show the VSI operating waveforms and the harmonic components of the dc-link capacitor current through the temperature rise test at the modulation index of 0.643, the load power factor of 0.891, and the inverter output power P_{inv} of 2.7 kW. The measured inverter efficiency was 96.11% with the modified conventional SVPWM, whereas the efficiency was 96.39% with the proposed SVPWM. The proposed SVPWM reduce the capacitor loss, which is calculated as following [3-9]–[3-11], by 54.2%

$$P_{Cap} = \sum_{n=1} \left(R_{ESR.n} \cdot i_C^2 \right). \quad \text{.....(3.6)}$$

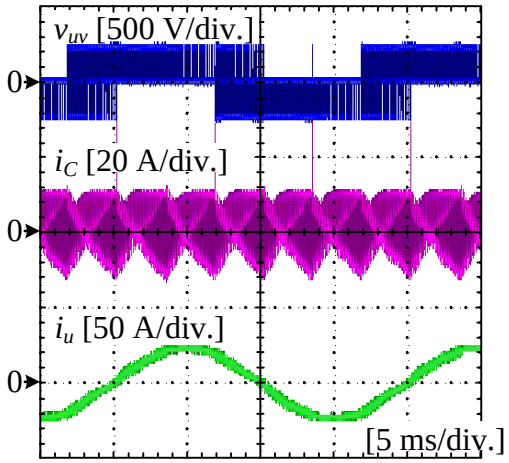


(a) Operating waveforms.

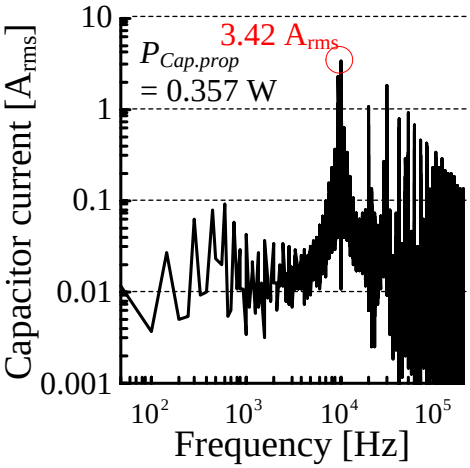


(b) Harmonic spectrum of i_C.

Fig. 3.27. VSI operating waveforms and harmonic components of dc-link capacitor current with conventional SVPWM at m = 0.643, cos φ = 0.891 (27° lagging), and P_{inv} = 2.7 kW.



(a) Operating waveforms.



(b) Harmonic spectrum of i_C.

Fig. 3.28. VSI operating waveforms and harmonic components of dc-link capacitor current with proposed SVPWM at m = 0.643, cos φ = 0.891 (27° lagging), and P_{inv} = 2.7 kW.

Fig. 3.29 shows the measured capacitor core temperature. The temperature rise tests were conducted until the container internal temperature reaches 60℃, the rated temperature of the coated vinyl of wire, while VSI operating under the experimental conditions in Figs 3.27–3.28. Fig. 3.29 confirms the capacitor temperature difference of 9.0℃ after 10800 seconds. Furthermore, the proposed SVPWM lowers the equilibrium capacitor temperature, which is estimated from the test results using the least-square method, by 11℃ compared to the conventional SVPWM. In other words, the proposed SVPWM reduces the film capacitor heating by 18.9% compared to the conventional SVPWM.

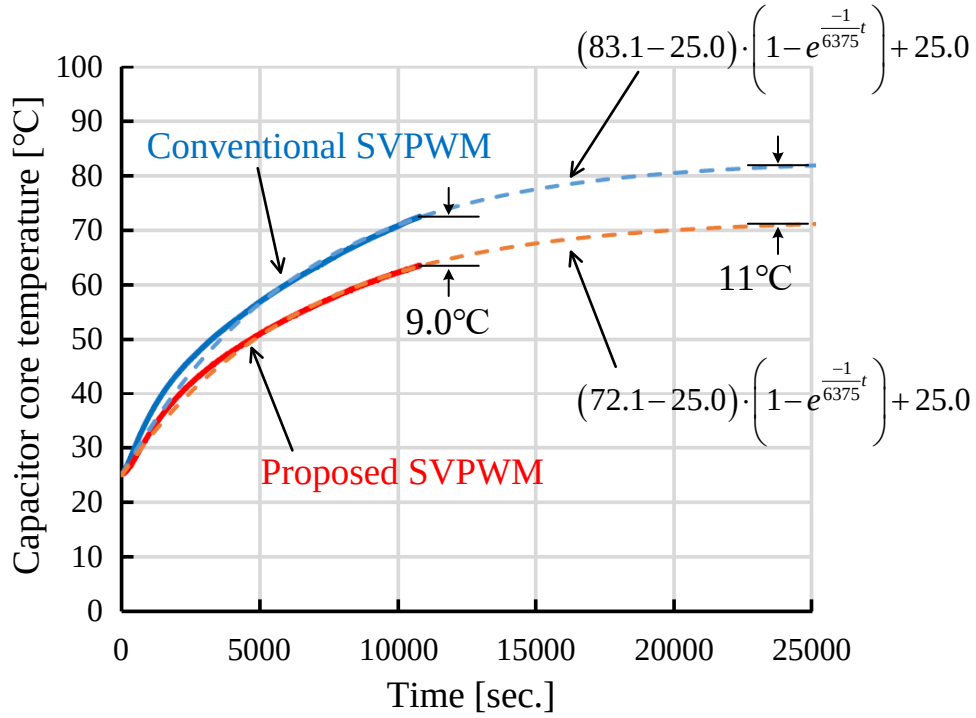


Fig. 3.29. Measured capacitor core temperature and its approximated curve with conventional and proposed SVPWM.

Fig. 3.30 shows the harmonic spectrum of *u*-phase output current under the same experimental conditions as in Figs 3.27–3.28. The proposed SVPWM worsens the phase current THD compared to the conventional SVPWM also in these experimental conditions. These results will be compared with other PWM strategies explained in chapter 4 and chapter 5.

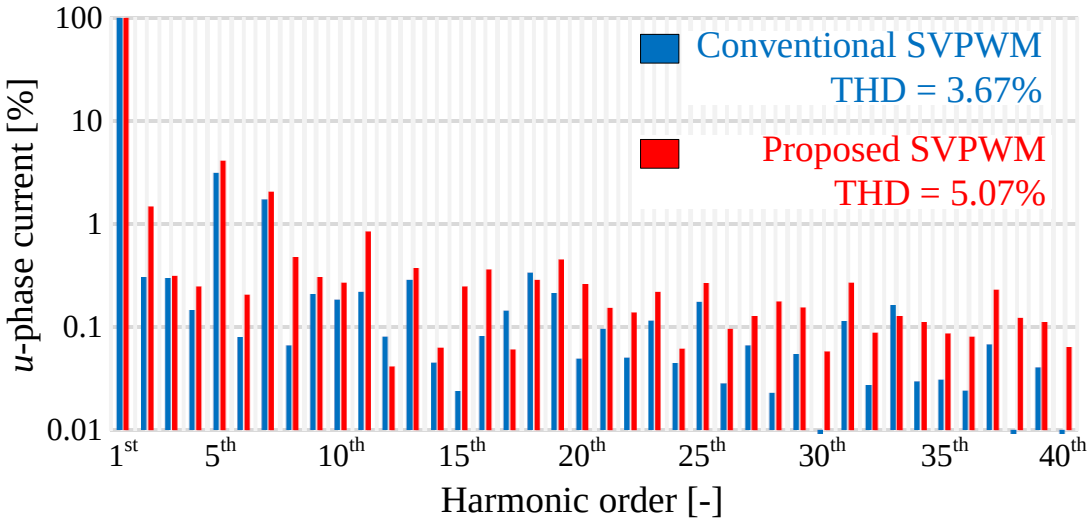
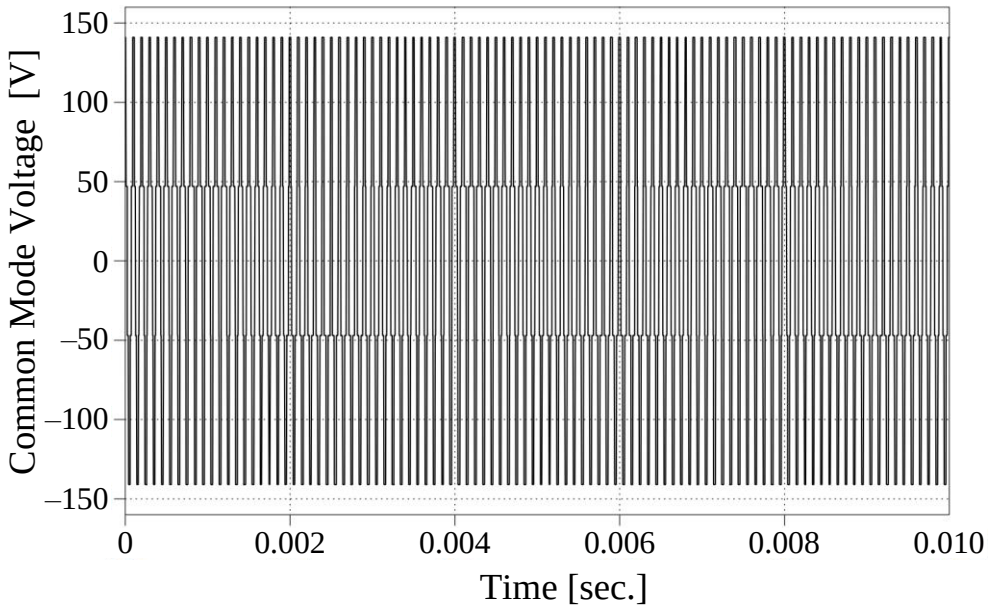
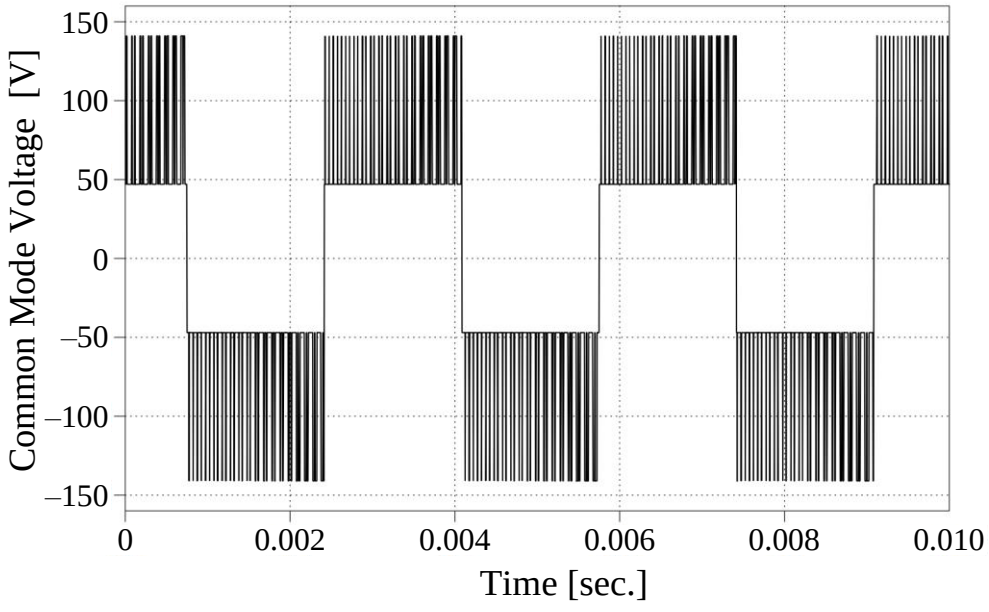


Fig. 3.30. i_u harmonic spectrum and its THD at m = 0.643, cos φ = 0.891 (27° lagging), and P_{inv} = 2.7 kW (under same conditions as in Figs. 3.27–3.28).

Figs. 3.31–3.32 show the PLECS simulation results of common-mode voltage waveforms and the harmonic components at the modulation index of 0.643, the load power factor of 0.891. Note that the fundamental frequency is set to 100 Hz for the simplification of the harmonic analysis, whereas the switching frequency is 10 kHz. Fig. 3.31 demonstrates that the step change of the common-mode voltage is reduced with the proposed SVPWM. Fig. 3.32 also confirms that the switching frequency component of the common-mode voltage is greatly reduced. In terms of higher switching frequency components up to 30 MHz, which are the conducted electromagnetic interference (EMI) frequency band, the proposed SVPWM lead to the reduced common-mode voltage. The proposed SVPWM uses the near switching state voltage vectors with the gate pulse symmetry about the center of the control period. Therefore, the proposed SVPWM improves not only the dc-link capacitor current harmonics but also the common-mode voltage harmonics.

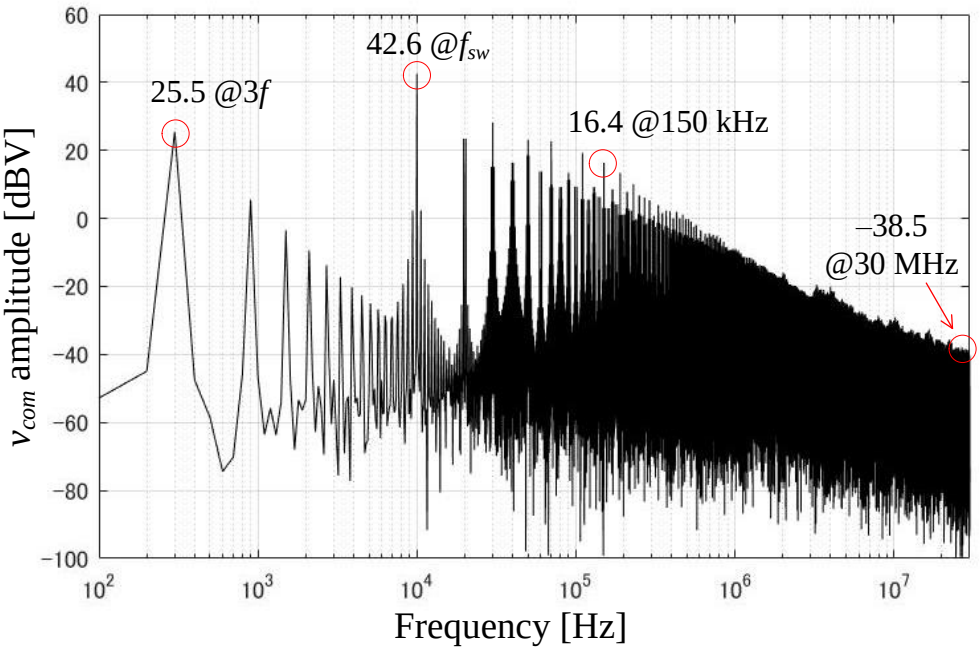


(a) Conventional SVPWM.

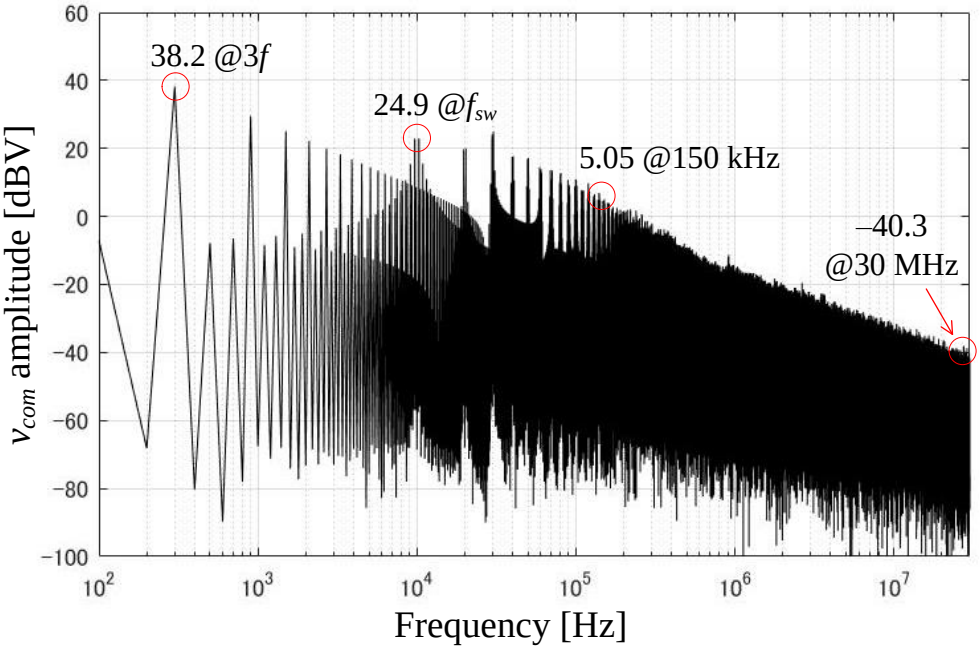


(b) Proposed SVPWM.

Fig. 3.31. PLECS simulation results of common-mode voltage at m = 0.643, cos φ = 0.891 (27° lagging) (under same conditions as in Figs. 3.27–3.28 except for fundamental frequency of 100 Hz).



(a) Conventional SVPWM.



(b) Proposed SVPWM.

Fig. 3.32. v_{com} harmonic spectrum at m = 0.643, cos φ = 0.891 (27° lagging) (under same conditions as in Figs. 3.27–3.28 except for fundamental frequency of 100 Hz).

3.7. Electrolytic Capacitor Lifetime Estimation

The expected lifetime (L_n) of the electrolytic capacitors is calculated as the multiplication of the lifetime (L_o) at maximum operating temperature of the capacitor at rated ripple current and rated voltage, which is specified on datasheet, by three acceleration rates which are dependent on the ambient temperature (F_T), the ripple current (F_I), and the applied voltage (F_V) [3-12]. In order to compare the lifetime expectancy of the electrolytic capacitors, which is influenced by only the ripple current, the following assumption is conducted.

1. The ambient temperature is constant at the maximum operating temperature of the capacitor ($F_T = 1$).
2. The applied voltage (E_{dc}) is constant and below the rated voltage ($F_V = 1$).

Therefore, the expected lifetime of the electrolytic capacitors is calculated as follows:

$$L_n = L_o \times F_I \quad \text{.....(3.7)}$$

where the L_o is 5000 h for the aluminum electrolytic capacitors (NX series, Nichicon Corp. [3-13]).

Table 3.4 lists the frequency coefficient of the rated ripple current flowing through aluminum electrolytic capacitors [3-13]. The lifetime of the electrolytic capacitors decreases because of the heat generated inside electrolyte due to power loss when ripple current flows through ESR of the electrolytic capacitors. Meanwhile, ESR of the electrolytic capacitors varies dependently on the current frequency. It is possible to calculate the normalized dc-link current harmonics ($I_{DC.in.rms.freq(\text{p.u.})}$) considering the frequency dependence of the ESR of aluminum electrolytic capacitor by dividing the dc-link current harmonic components by the frequency coefficient (K_f) as follows:

$$I_{DC.in.rms.\,freq(\text{p.u.})} = \frac{1}{I_m}\sqrt{\sum_{n=1}\left(\frac{1}{\sqrt{2}}\cdot\frac{i_{DC.in.n}}{K_f}\right)^2} \quad \text{.....(3.8)}$$

Fig. 3.33 shows the harmonic components of the dc-link current considering the frequency dependence of the ESR of aluminum electrolytic capacitor at the modulation index of 0.705 and the load power factor of 0.866 (under the same conditions as in Fig. 3.13). The proposed SVPWM reduces the dc-link current harmonics $I_{DC.in.rms.freq(\text{p.u.})}$ by 29.0% when the frequency dependence of the ESR of aluminum electrolytic capacitor is considered. Assuming that the motor is mostly operated at the modulation index of 0.705 and the load power factor of 0.866, and the aluminum electrolytic capacitors in the conventional SVPWM are designed at the worst case of the rated ripple current (i.e., F_I as 1), the lifetime expectancy of the electrolytic capacitor can be given by

$$L_{n\_conv.SVPWM} = L_o \times 1 = 5000\ \text{h.} \quad \text{.....(3.9)}$$

On the other hand, the application of the proposed SVPWM raises F_I to 1.41 due to a current harmonic reduction of 29.0%. So, the lifetime expectancy of the electrolytic capacitor with the proposed SVPWM can be given by

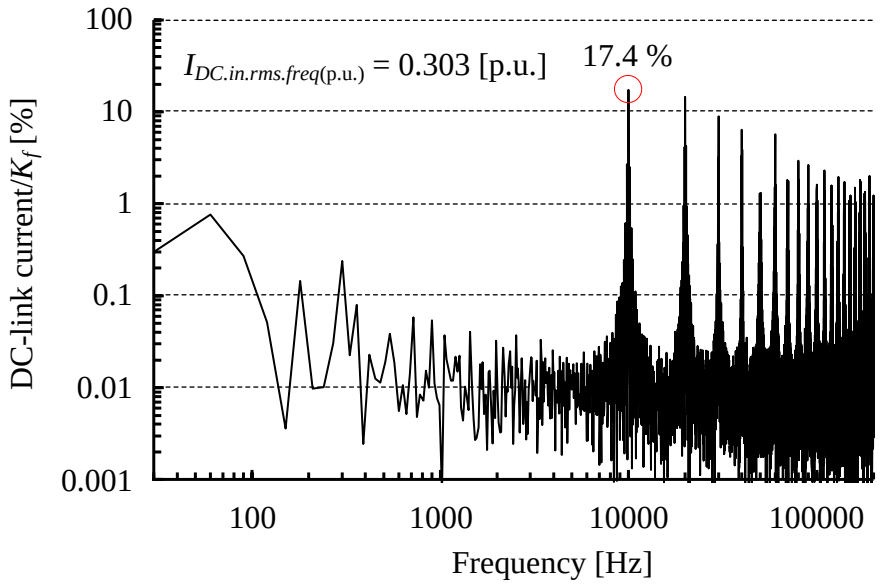
$$L_{n\_prop.SVPWM} = L_o \times 1.41 = 7050\ \text{h.} \quad \text{.....(3.10)}$$

TABLE 3.4.

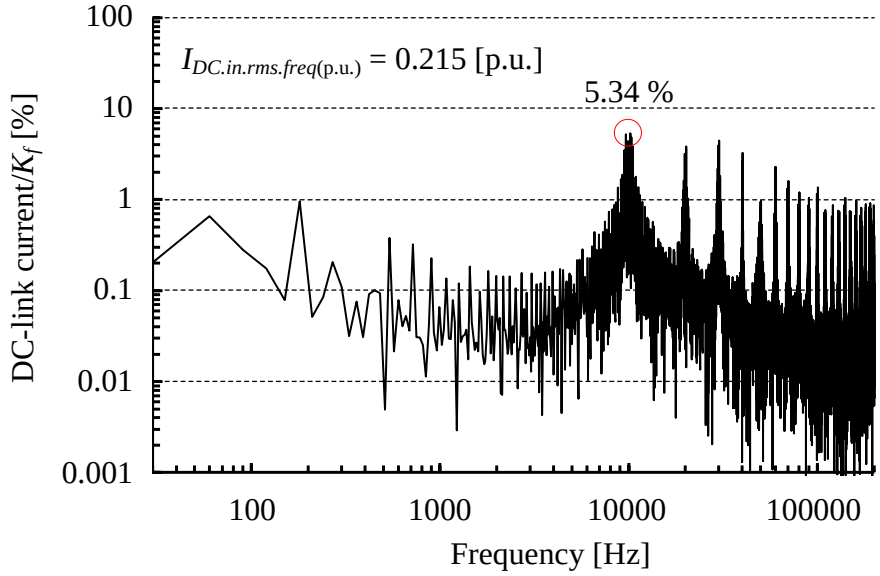
FREQUENCY COEFFICIENT OF RATED RIPPLE CURRENT FLOWING THROUGH ALUMINUM ELECTROLYTIC CAPACITORS (NX SERIES, NICHICON CORP.).

Frequency [Hz]	50	60	120	360	1 k	10 k or more
Coefficient K_f	0.80	0.82	1.00	1.20	1.35	1.40

It is concluded that the application of the proposed SVPWM might extend the lifetime of the electrolytic capacitor about 1.41 times longer at most than that of the conventional SVPWM.



(a) Conventional SVPWM.



(b) Proposed SVPWM.

Fig. 3.33. Harmonic components of dc-link current considering frequency dependence of ESR of aluminum electrolytic capacitor at m = 0.705 and cos φ = 0.866 (φ = 30° lagging) (under same conditions as in Fig. 3.13).

3.8. Conclusion

The proposed SVPWM in this chapter optimized the combinations of the applied voltage space vector depend on the load current sector. This provided the minimization of the rms value of the dc-link capacitor current at any conditions of the modulation index and the load power factor, which is not achieved by the past works. In comparison with the conventional SVPWM, the proposed SVPWM reduces the dc-link current harmonics by 29.0%, might be leading to the 1.41 times lifetime extension of the electrolytic capacitors. Moreover, the proposed SVPWM reduces the capacitor loss by 54.2%, lowering the equilibrium capacitor temperature by 11℃ (18.9%). Consequently, the proposed SVPWM contributes into the reductions of the dc-link capacitor current stress and the dc-link capacitor thermal stress. However, the proposed SVPWM also has following drawbacks:

1. Worse load current THD due to the optimized combinations of the voltage space vectors to reduce the dc-link capacitor current ripple.
2. Switching pattern implementation with the space vector concept, leading to the necessity of FPGA. Specifically, in electric vehicle (EV) applications where the high power density is highly desired, FPGA is not used due to its cost issue. Thus, the proposed SVPWM might not be appropriate to the EV applications.

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Chapter 4

Carrier-based Continuous PWM Strategy for DC-link Capacitor Current Stress Reduction

4.1. Introduction

This chapter presents an implementation method for the PWM switching patterns to reduce the dc-link capacitor current stress in the two-level three-phase VSI based on the carrier-based continuous PWM (CPWM) strategy. The original idea in this research is that the triangular-carrier comparison with the shifted modulating signals is applied to achieve the PWM switching patterns to reduce the dc-link capacitor current stress. Specifically, the proposed shifted modulating signals are generated based on the conventional continuous modulating signals and the load current sector. The advantages of the proposed CPWM is the reduction for the dc-link capacitor current stress only with the low-cost digital hardware such as a general-purpose micro-computer, which is used in the electric vehicle applications where the high power density is highly desired. Furthermore, the less deterioration of the load current quality compared to the proposed SVPWM is also achieved.

This chapter is organized as follows: First, in chapter 4.2, the reduction method of the dc-link current harmonics by using the shifted modulating

signals based on the load current sector is explained in detail. Next, in chapter 4.3 and chapter 4.4, analytical, simulation, and experimental results are presented to verify the effectiveness in terms of the reduction of the dc-link current harmonics, the impact on the output phase current quality, inverter efficiency, and the dc-link capacitor heating. Then, in chapter 4.5, the lifetime of the electrolytic capacitors is estimated and compared. Finally, in chapter 4.6, the conclusion of this chapter will be presented.

4.2. Proposed Continuous Modulating Signals

It should be recalled that the dc-link current is highly influenced by the switching patterns and output phase currents, i.e., the load power factor according to (2.11) and (2.12). Therefore, the proposed CPWM reduces the dc-link current harmonics by shifting modulating signals in every half control period and adjusting the gate pulse timings in the control period. Furthermore, the proposed shifting rule of the modulating signals adapts to the load current conditions based on the combination of the voltage sector and load current sector. In other words, the proposed modulation method reduces the dc-link current harmonics with adaptation to the variation of the load power factor.

4.2.1 Adjustment Method for Gate Pulse Timings

Fig. 4.1 shows the adjustment method for the gate pulse timings with the modulating signal shift. Note that the proposed modulating signals are implemented based on the premise that the references are to be updated at both the positive-peak and negative-peak of the triangular carrier with the general-purpose micro-computer. For RX62T [4-1] as an example, the modulating signals are to be updated at both the positive-peak and the negative-peak of the triangular carrier by changing the setting of general timer control resister. The proposed modulating signals are generated by shifting the original continuous modulating signals v^*_x alternately to positive side and negative side in every half control period. First, the shifting coefficient (A_x) between the original and shifted reference is defined as a value from 1.0 to 2.0. The shifting coefficient A_x of 1.0 indicates that the modulating signal shift is not performed as in Fig. 4.1(a). The coefficient A_x of 2.0 indicates that the modulating signals are shifted maximally in linear-modulation region as in Fig. 4.1(b). When v^*_x is positive as in Fig. 4.1, the maximum shifting amount Δv^*_x at A_x of 2.0 is limited by the positive-peak of carrier and calculated as $1 - v^*_x$. For the negative v^*_x, the maximum Δv^*_x is limited by the negative-peak of the carrier and calculated as $v^*_x + 1$.

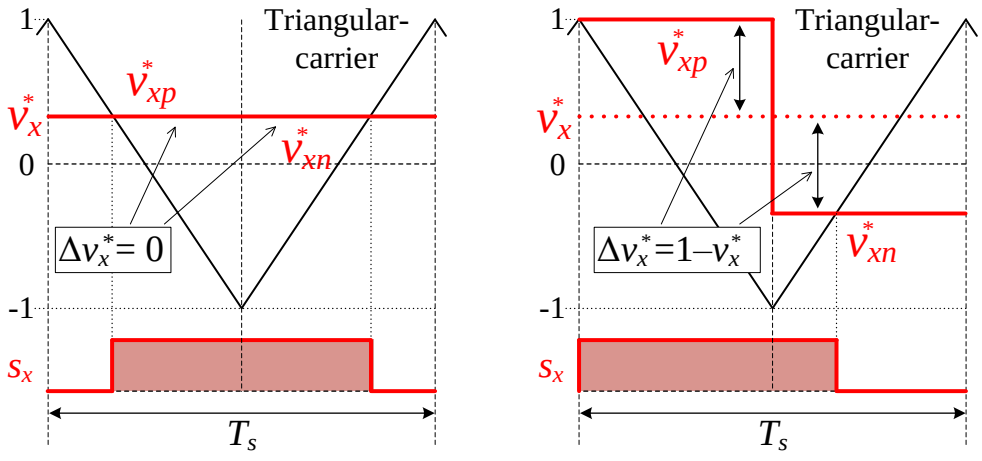
Furthermore, the shifting amount Δv^*_x is defined to be varied from zero at A_x of 1.0 to the maximum shifting amount at A_x of 2.0 linearly with regard to the value of A_x. Then, the positively-shifted modulating signal v^*_{xp} and the negatively-shifted modulating signal v^*_{xn} are calculated as

$$\begin{cases} v^*_{xp} = v^*_x + \Delta v^*_x = (2 - A_x)\cdot v^*_x + A_x - 1 \\ v^*_{xn} = v^*_x - \Delta v^*_x = A_x \cdot (v^*_x - 1) + 1 \end{cases} \quad \text{if } v^*_x \geq 0,$$

$$\begin{cases} v^*_{xp} = v^*_x + \Delta v^*_x = A_x \cdot (v^*_x + 1) - 1 \\ v^*_{xn} = v^*_x - \Delta v^*_x = (2 - A_x)\cdot v^*_x - A_x + 1 \end{cases} \quad \text{if } v^*_x \leq 0. \qquad \text{.....(4.1)}$$

Note that (4.1) is dependent only on the polarities of v^*_x.

The gate pulse timings are adjusted during the control period while maintaining these original pulse widths by shifting the modulating signals as in Fig. 4.1. In particular, the gate pulse adjustment length is determined by the value of A_x. In addition, the timing moves to the left when the modulating signal is shifted to the positive side in anterior half control period as in Fig. 4.1(b); in contrast, the gate pulse timing is shifted to the right when the modulating signal is shifted to the positive side in latter half control period.



(a) A_x = 1.0. (b) A_x = 2.0.

Fig. 4.1. Adjustment method for gate pulse timings with modulating signal shift.

4.2.2 Proposed Modulating Signals for DC-link Current Harmonic Reduction

Fig. 4.2 shows the waveforms of the three-phase modulating signals and the output phase currents at the modulation index of 0.7 and the load power factor of 0.707 (45° lagging). As defined in the previous chapter, the voltage sectors (I–VI) are determined by the polarities of the three-phase modulating signals, whereas the load current sectors (A–F) are determined by the directions of the three-phase output phase currents.

Fig. 4.3 shows the zoomed-in waveforms of the conventional and proposed modulating signals, the switching functions, and the dc-link current at the modulation index of 0.7, the phase angle of 25°, and the load power factor of 0.707. This control period is located within the overlap period between the voltage sector I ($v^*_u > 0$, $v^*_v < 0$, $v^*_w < 0$) and the load current sector A ($i_u > 0$, $i_v < 0$, $i_w < 0$). For the positive load power factor, i.e., driving

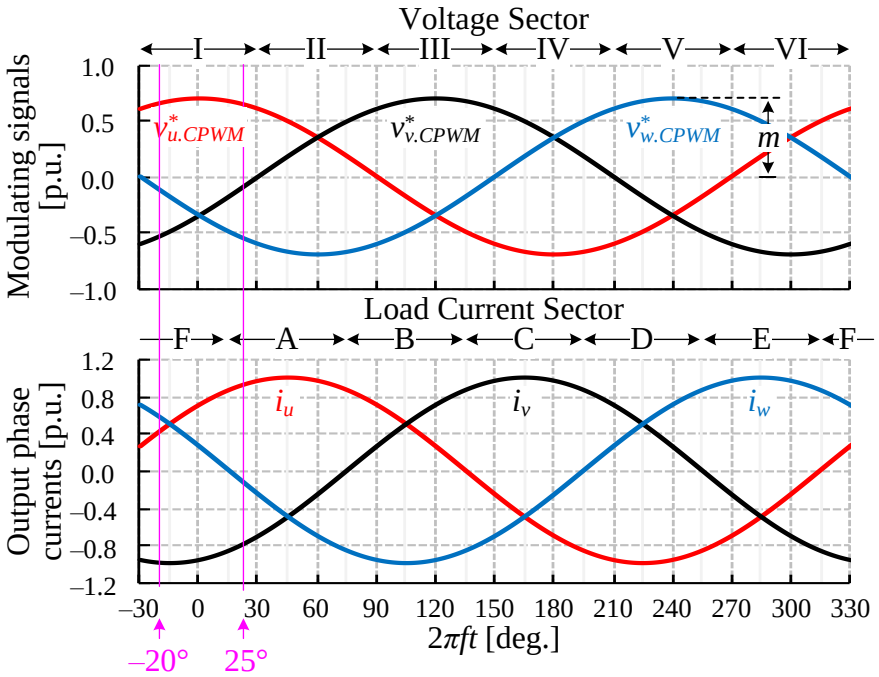
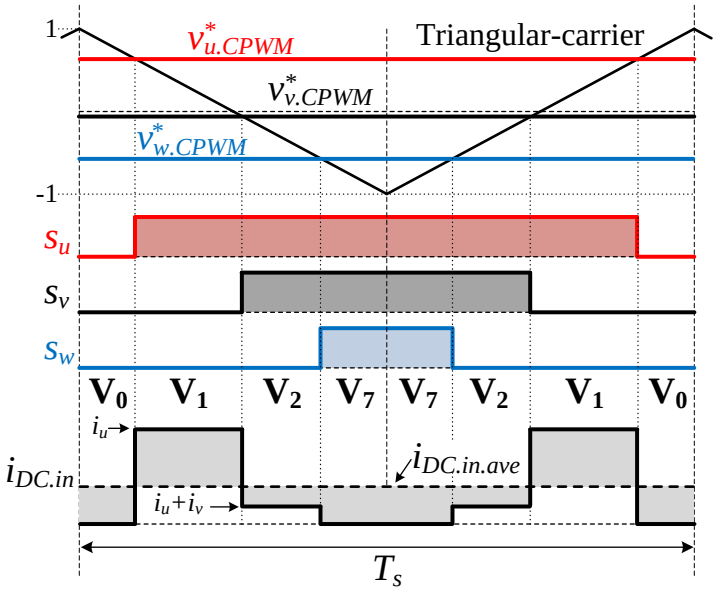


Fig. 4.2. Continuous modulating signals $v^*_{x.CPWM}$ and output phase currents i_x at m = 0.7 and cos φ = 0.707 (45° lagging).

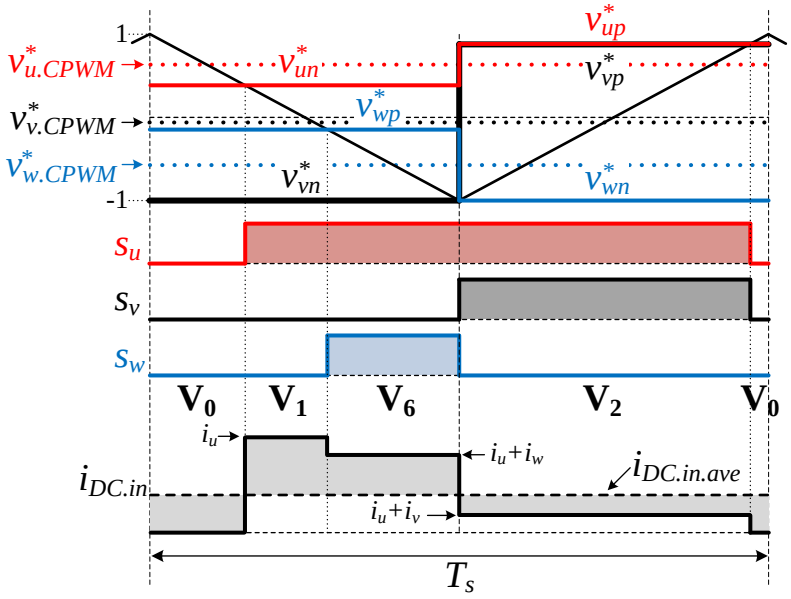
mode, the average value of the dc-link current ($i_{DC.in.ave}$) is also positive according to (2.12). As observed in Fig. 4.2, only i_u is positive at the phase angle of 25° and the load power factor of 0.707. During this control period, *u*-phase modulating signal should become larger than the other two phase modulating signals, and the gate pulse s_u should cover both of s_v and s_w in the time domain to avoid the dc-link current ($i_{DC.in}$) polarity flip compared to the $i_{DC.in.ave}$ polarity. If the above criterion is not satisfied, $i_{DC.in}$ becomes negative, leading to the large $i_{DC.in}$ fluctuations against the positive $i_{DC.in.ave}$. In addition to the above criterion, the overlap of the other two gate pulses s_v and s_w should be shortened to further reduce $i_{DC.in}$ fluctuations around $i_{DC.in.ave}$. With those modified gate pulse timings, the applying duration of the output voltage vector $\mathbf{V_1}$ (1 0 0), which causes the large difference between $i_{DC.in}$ (= i_u) and $i_{DC.in.ave}$, is shortened compared to the conventional CPWM shown in Fig. 4.3(a). In addition, the applying durations of $\mathbf{V_2}$ (1 1 0) and $\mathbf{V_6}$ (1 0 1), which result in the small $i_{DC.in}$ harmonics, are extended and generated with those gate pulses. In order to achieve both the criterion to avoid the $i_{DC.in}$ polarity flip compared to the $i_{DC.in.ave}$ polarity and the criterion to reduce the $i_{DC.in}$ fluctuations,

1. v^*_u, with the positive same-phase current, is shifted to the positive side simultaneously with the larger phase modulating signal between the other two phases, i.e., v^*_v.
2. v^*_v and v^*_w are shifted alternately and maximally to the positive side as long as they do not exceed v^*_{up} and v^*_{un}.

As a result, the proposed shifted modulating signals result in the smaller fluctuations of the dc-link current around its average value and the smaller shaded area in the dc-link current waveform in Fig. 4.3, leading to the smaller rms value of the dc-link capacitor current [4-2].



(a) Conventional CPWM.

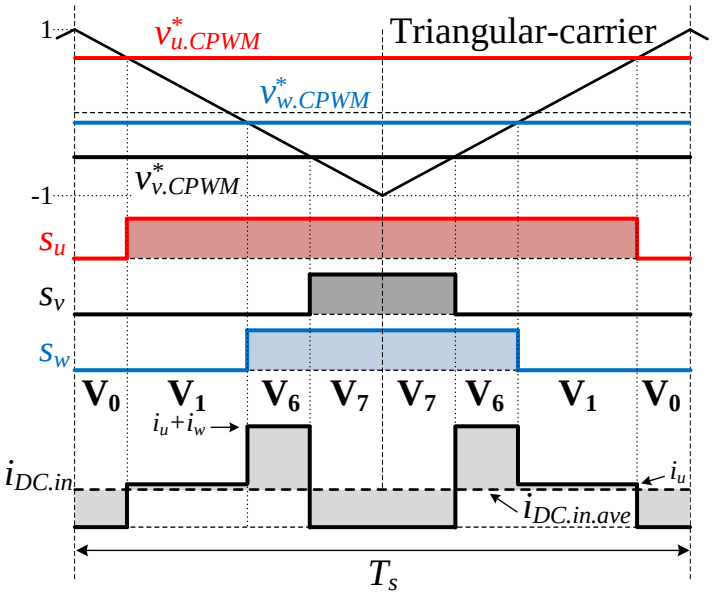


(b) Proposed CPWM with A_u = 1.68, A_v = 2.00, and A_w = 2.00.

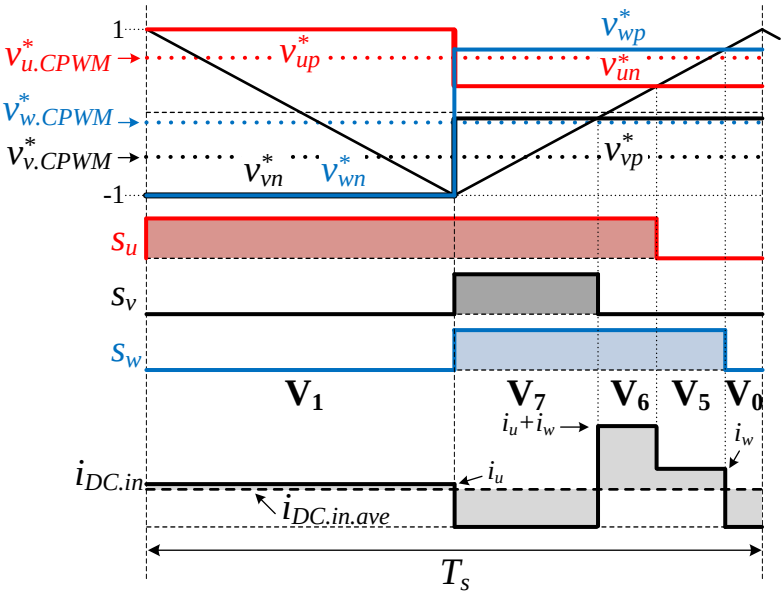
Fig. 4.3. Zoomed-in waveforms of modulating signals, switching functions, and dc-link current at m = 0.7, $2\pi ft$ = 25°, and cos φ = 0.707 (45° lagging).

Fig. 4.4 shows an another example of the zoomed-in conventional and proposed modulating signals at the modulation index of 0.7, the phase angle of –20°, and the load power factor of 0.707. This control period is located within the overlap period between the voltage sector I ($v^*_u > 0$, $v^*_v < 0$, $v^*_w < 0$) and the load current sector F ($i_u > 0$, $i_v < 0$, $i_w > 0$). At the phase angle of –20° and the load power factor of 0.707, only i_v is negative as observed in Fig. 4.2. Note that the only different phase current polarity is negative which is inverse from the case in Fig. 4.3. Even at this case, both of the criterion to avoid the $i_{DC.in}$ polarity flip and the criterion to reduce the $i_{DC.in}$ fluctuations are effective in reducing the harmonics. In order to achieve those criteria,

1. v^*_v, when the negative same-phase current, is shifted to the negative side simultaneously with the smaller phase modulating signal between the other two phases, i.e., v^*_w.
2. v^*_u and v^*_w are shifted alternately and maximally to the negative side as long as they do not become smaller than v^*_{vp} and v^*_{vn}.



(a) Conventional CPWM.



(b) Proposed CPWM with A_u = 2.00, A_v = 2.00, and A_w = 2.00.

Fig. 4.4. Zoomed-in waveforms of modulating signals, switching functions, and dc-link current at m = 0.7, $2\pi ft$ = –20°, and cos φ = 0.707 (45° lagging).

Fig. 4.5 shows the variation of A_x and the proposed modulating signals $v^*_{x.PCPWM}$ during one-cycle operation at m = 0.7 and cos φ = 0.707. As described in Figs 4.3 and 4.4, the modulating signals are shifted in every half control period to satisfy both the criterion to avoid the $i_{DC.in}$ polarity flip and the criterion to reduce the $i_{DC.in}$ fluctuations. Nevertheless, when cos φ is lower than 0.866 (φ > 30°), there are areas where the criterion to avoid the $i_{DC.in}$ polarity flip is not satisfied. In the phase range of 0°–15° in Fig. 4.5, for example, only i_v is negative; thus, v-phase modulating signal should become smaller than the other two-phase modulating signals to avoid the $i_{DC.in}$ polarity flip. However, the original v-phase modulating signal is not the minimum at this phase range and the criterion is not satisfied. At these phase ranges, the proposed modulating signal shift further worsens the dc-link current harmonics. Therefore, the conventional CPWM is applied at these phase ranges.

For the regenerative braking mode (φ > 90°), $i_{DC.in.ave}$ becomes negative according to (2.12). In this case, whether the certain phase modulating signal should be maximized or minimized in the criteria for dc-link current harmonics reduction is reversed against the driving mode. Note that whether the motor operating mode is driving mode or regenerative braking mode is detected from the combinations of modulating signal polarities and the detected output phase-current directions.

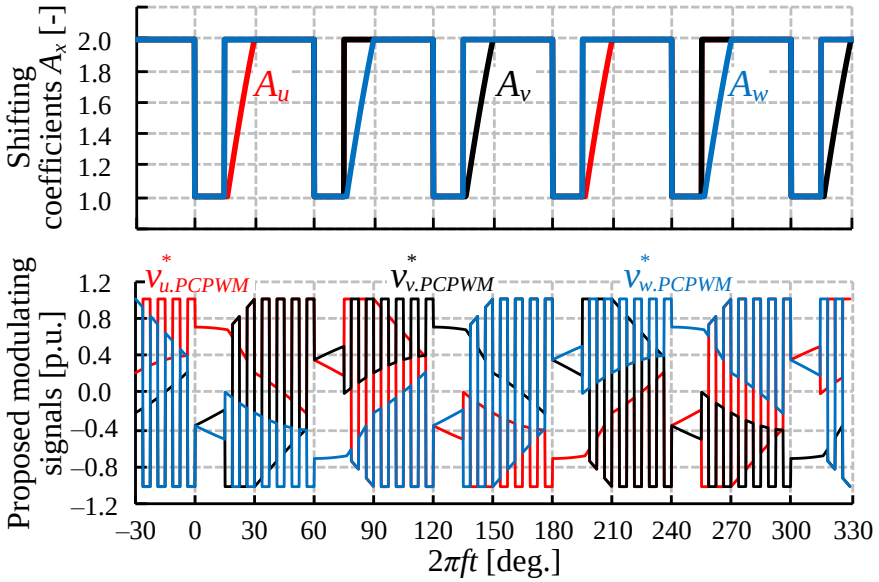


Fig. 4.5. Variation of A_x and proposed modulating signals $v^*_{x.PCPWM}$ during one-cycle operation at m = 0.7 and cos φ = 0.707 (45° lagging). At the phase ranges of 0°–15°, 60°–75°, 120°–135°, 180°–195°, 240°–255°, and 300°–315°, the dc-link current harmonics are not to be reduced, and the conventional CPWM is applied. The switching frequency is set to be low for better illustration.

4.2.3 Design Flowchart of Shifting Coefficient A_x

Fig. 4.6 shows the design flowchart for A_x. First, the conditions of the phase angle and the load current are detected from the voltage sector (I–VI) and the load current sector (A–F). Next, the coefficient A_x is calculated to satisfy the two criteria for the dc-link current harmonics reduction by using (4.1) and the gate pulse widths t_x. The gate pulse widths t_x are calculated from v^*_x as

$$t_x = \frac{v_x^* + 1}{2}, \quad (x = u, v, w). \qquad (4.2)$$

There are four division processes to calculate all shifting coefficients in the worst case, which might result in a heavy computation load. In practical conditions, the calculation of A_x is performed offline and the values of A_x are stored in a look-up table. The offline calculation of A_x provides the same current stress reduction effect as the online calculation because the value of A_x varies only with the phase (u, v, w), the phase angle (0°–360°), the modulation index (0–1.0), and the load current sector (A–F), which is independent from the motor parameters.

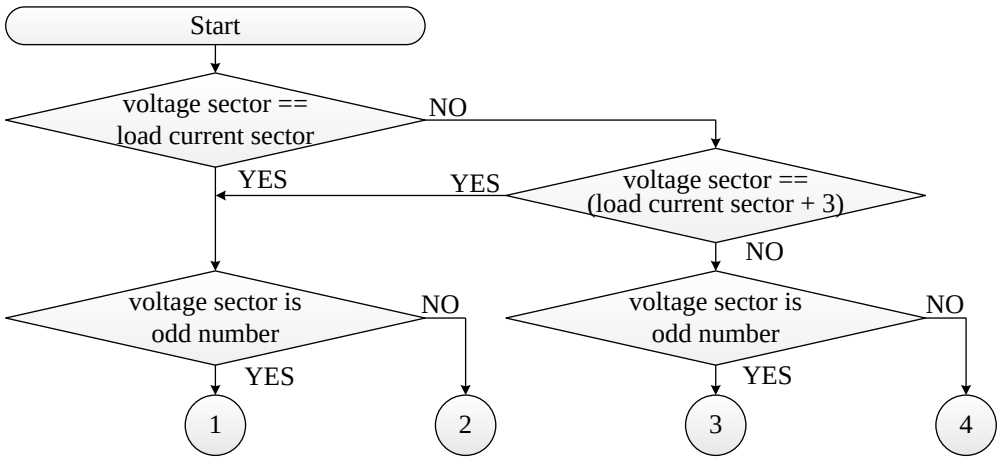


Fig. 4.6. Design flowchart for A_x. The phase with the most positive modulating signals is denoted as phase *a* while the phase with the most negative modulating signal is denoted as phase *c*. The phase which lies between phase *a* and phase *c* is denoted as phase *b*.

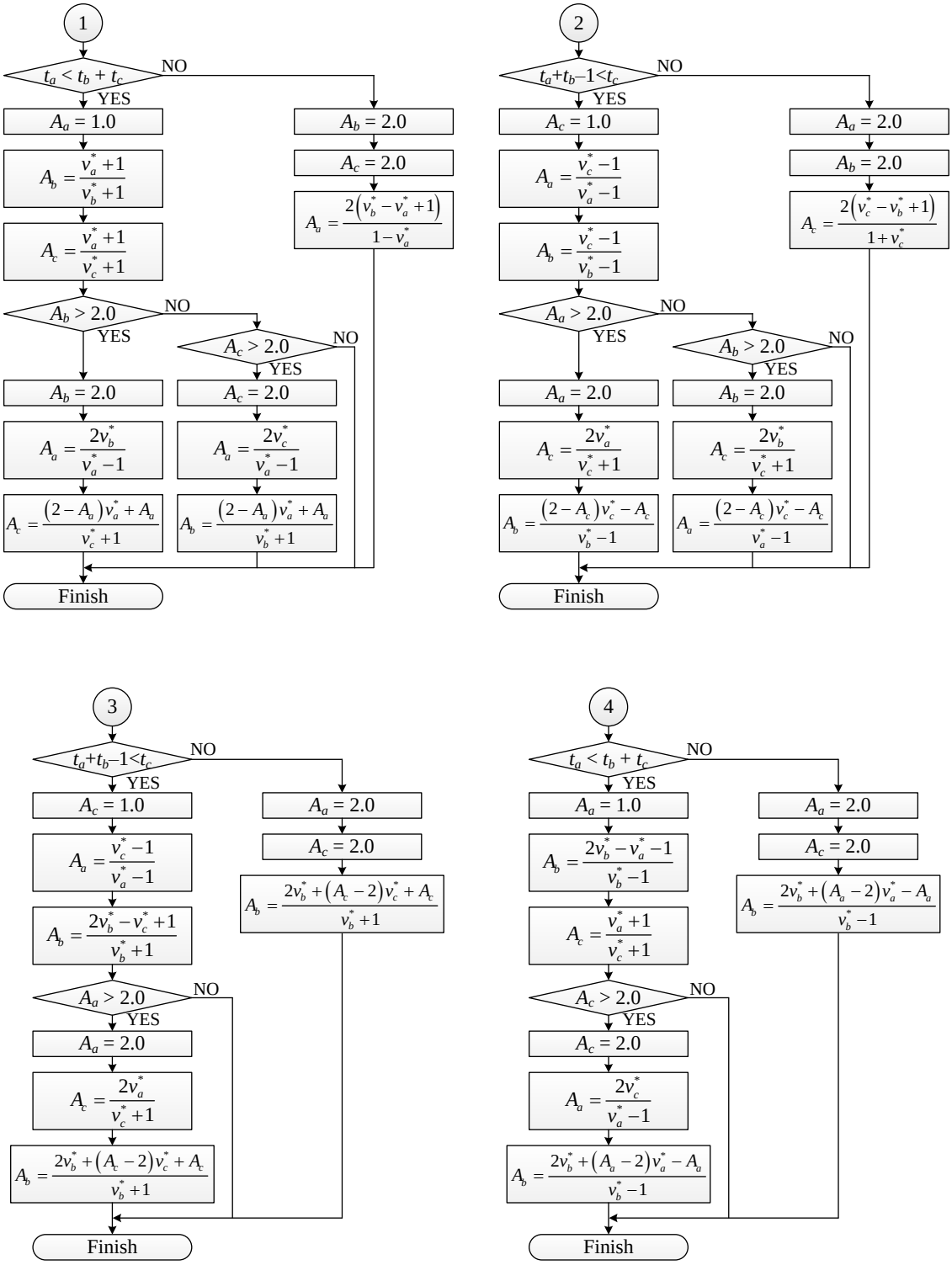


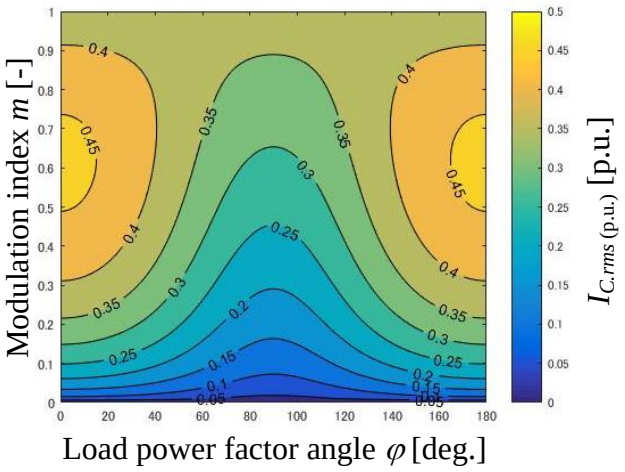
Fig. 4.6. Continued.

4.3. Analytical Evaluations

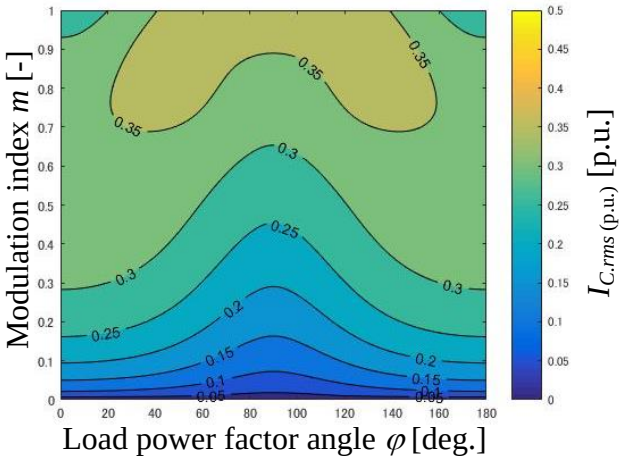
4.3.1 DC-link Capacitor RMS Current

In this chapter, the normalized dc-link capacitor rms current $I_{C.rms(\text{p.u.})}$ which is calculated as (2.13) is used for the evaluation of dc-link capacitor current stress reduction with the proposed CPWM.

Fig. 4.7 shows the analytical results of the dc-link capacitor current with regard to the modulation index and the load power factor angle. Fig. 4.7(a) demonstrates that with the application of the conventional CPWM, $I_{C.rms(\text{p.u.})}$ becomes the maximum at around m = 0.6 and absolute value of the load power factor |cos φ| = 1.0 due to the large difference between $i_{DC.in}$ (= 0 A) and $i_{DC.in.ave}$ at the applying durations of zero vectors $\mathbf{V_0}$ (0 0 0) and $\mathbf{V_7}$ (1 1 1). On the other hand, Fig. 4.7(b) demonstrates that the proposed CPWM reduces $I_{C.rms(\text{p.u.})}$ under any conditions of m and φ. In addition, a higher |cos φ| leads to a greater reduction effect on $I_{C.rms(\text{p.u.})}$. This trend is resulted from the relationship between φ and the application ratio of the shifted modulating signals in the whole phase range. When |cos φ| is higher than 0.866, the two criteria for the dc-link current harmonics reduction are satisfied over the whole phase range. Therefore, the shifted modulating signals are applied over the whole phase range, leading a large reduction of $I_{C.rms(\text{p.u.})}$. Nevertheless, when |cos φ| is lower than 0.866, the conventional CPWM is partially applied in the phase ranges where the criteria are not satisfied. The application ratio of the shifted modulating signals decreases as |cos φ| becomes small, and there is no $I_{C.rms(\text{p.u.})}$ difference between the conventional and proposed CPWM when cos φ = 0.



(a) Conventional CPWM.



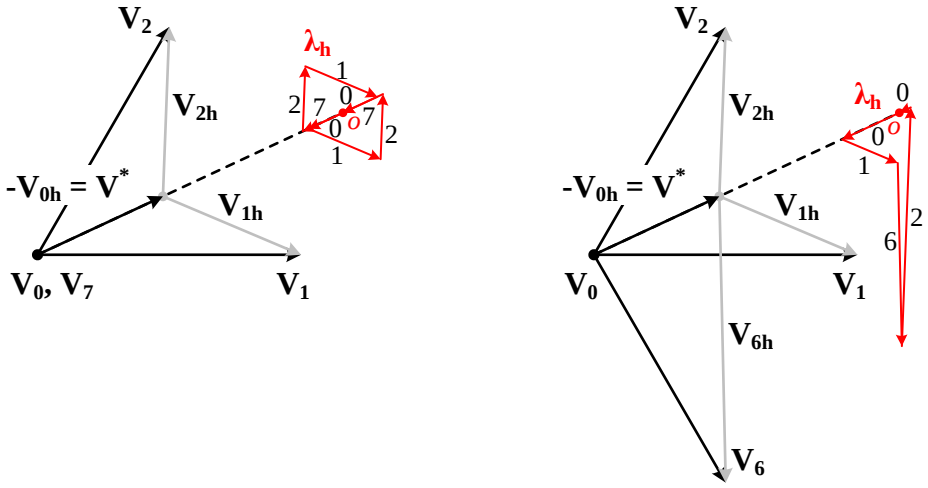
(b) Proposed CPWM.

Fig. 4.7. Analytical results of dc-link capacitor rms current with regard to modulation index m and load power factor cos φ.

4.3.2 Load Current Quality

In this chapter, the rms value of the harmonic flux over fundamental period λ_{rms} which is calculated as (3.4) is used for the evaluation of the load current quality with the proposed CPWM. The concept of harmonic flux [4-3] does not require the calculation of the harmonic spectrum of the VSI output voltage waveform, which is complicated for the proposed CPWM because of its gate pulse asymmetry in the carrier cycle.

Fig. 4.8 shows an example of the harmonic flux trajectories at the modulation index of 0.7 and the phase angle of 25°. These trajectories demonstrate that the proposed CPWM leads to the long distance between the harmonic flux trajectories and the origin *o*. Therefore, the proposed CPWM worsen the load current quality compared to the conventional CPWM.



(a) Conventional CPWM. (b) Proposed CPWM.

Fig. 4.8. Harmonic flux trajectories at m = 0.7 and $2\pi ft$ = 25°. The distance between the origin (o) and the trajectory of $\boldsymbol{\lambda}_{\mathbf{h}}$ is equal to the magnitude of the harmonic flux, and continuously fluctuates.

Fig. 4.9 shows the harmonic flux rms values with the conventional CPWM and the proposed CPWM. These analytical results also confirm that the proposed CPWM worsens the harmonic flux rms values compared to those with the conventional CPWM. The reason is because the proposed shifted modulating signals result in the application of the voltage space vector which is not the closest to $\mathbf{V}^*$, i.e., $\mathbf{V_6}$ in Fig. 4.8.

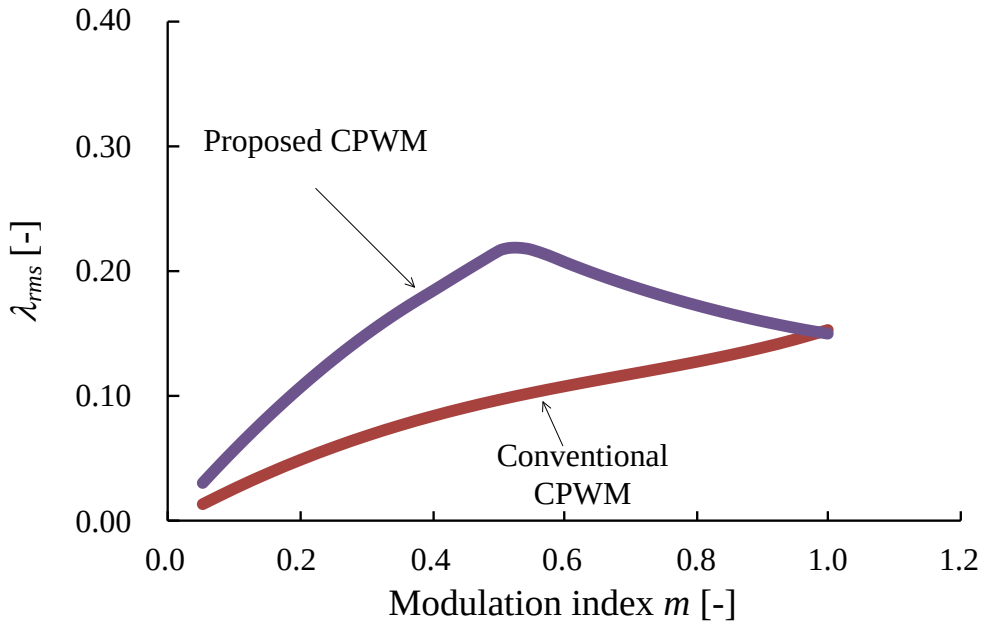


Fig. 4.9. Comparison of harmonic flux rms values with regard to modulation index. In the proposed CPWM calculations, the load power factor is set to 1.

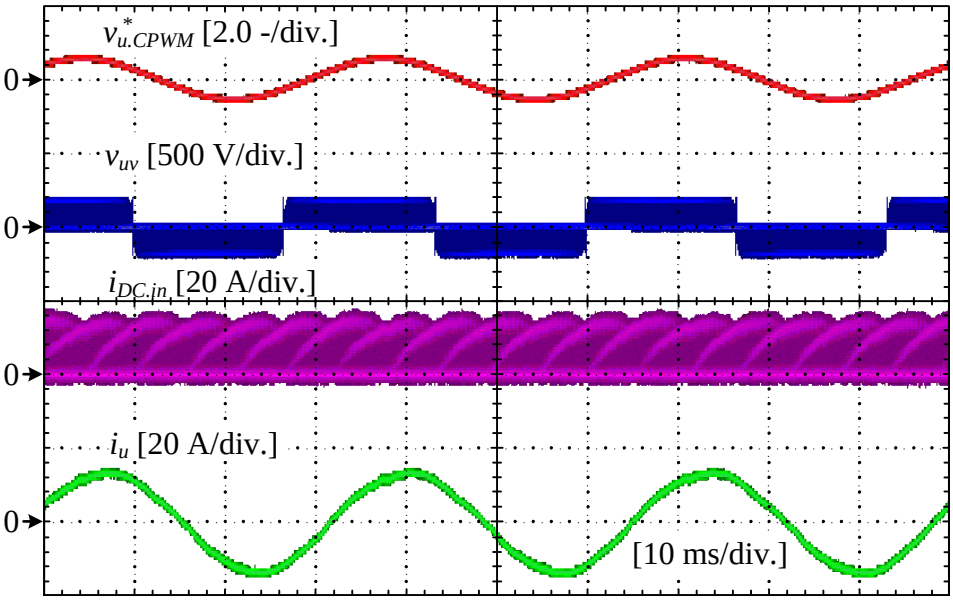
4.4. Simulation and Experimental Results

The effectiveness of the proposed CPWM was verified by the PLECS simulation and the experiment. The experimental setups were same as described in chapter 3.6.

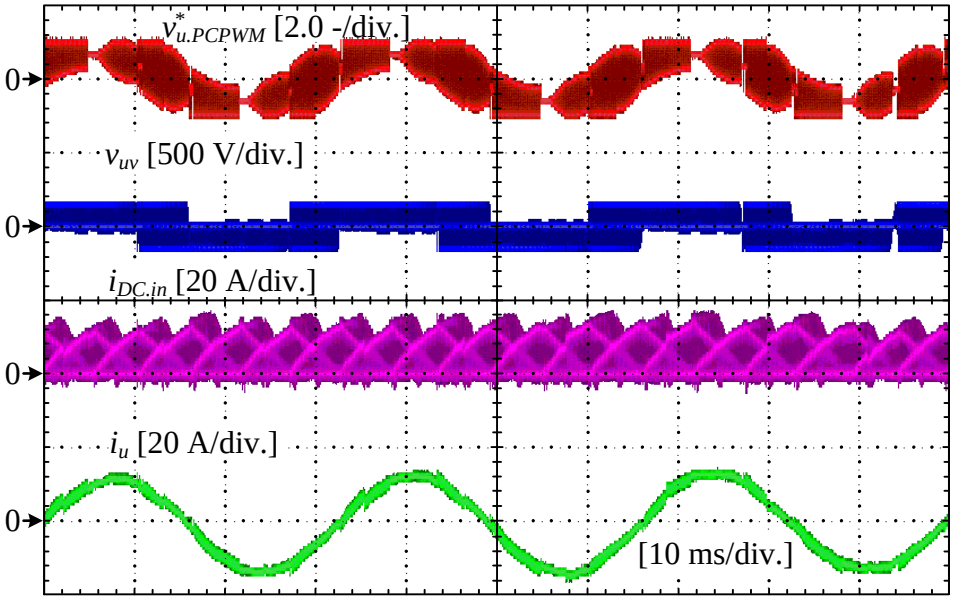
4.4.1. DC-link Current Harmonics

Fig. 4.10 shows the *u*-phase modulating signal, the line-to-line voltage, the dc-link current, and the output *u*-phase current with each modulation method at the modulation index of 0.550 and the load power factor of 0.866 (30° lagging), i.e., high-load power factor condition in driving mode. The modulating signals of the proposed CPWM are shifted in every half control period as shown in Fig. 4.10(b). The results show that the width of the envelope in the dc-link current is reduced. On the other hand, the larger transitions between $+E_{dc}$ and $-E_{dc}$ seem to occur in the line-to-line voltage with the proposed CPWM.

Fig. 4.11 shows the PLECS simulation results with each modulation method at the modulation index of 0.550 and the load power factor of 0.866 (30° lagging), same conditions of the experiments in Fig. 4.10. The zoomed-in waveforms of the dc-link current demonstrate that the width of the step change is reduced by the proposed CPWM. Furthermore, the zoomed-in waveforms of the line-to-line voltage demonstrate that the instantaneous voltage transition between $+E_{dc}$ to $-E_{dc}$ never occurs due to the dead-time period. Therefore, the proposed CPWM does not increase the motor surge voltage in practice compared to the conventional CPWM.

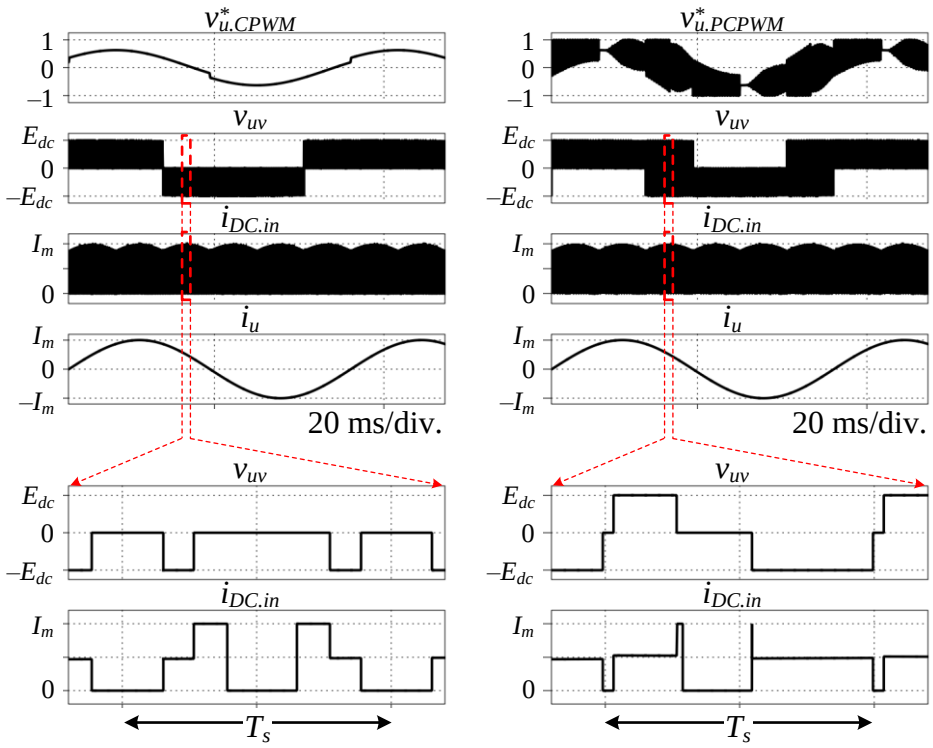


(a) Conventional CPWM.



(b) Proposed CPWM.

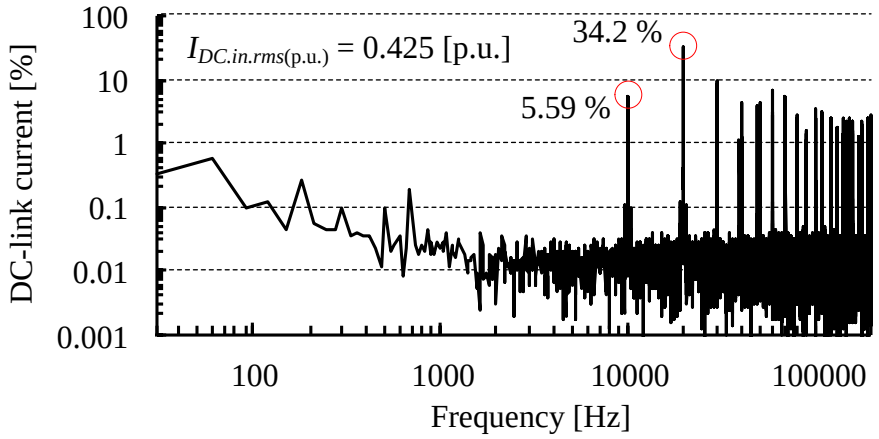
Fig. 4.10. Experimental waveforms at m = 0.550 and cos φ = 0.866 (30° lagging), i.e., driving mode with high-load power factor; u-phase modulating signal, output line-to-line voltage, dc-link current, and u-phase output current.



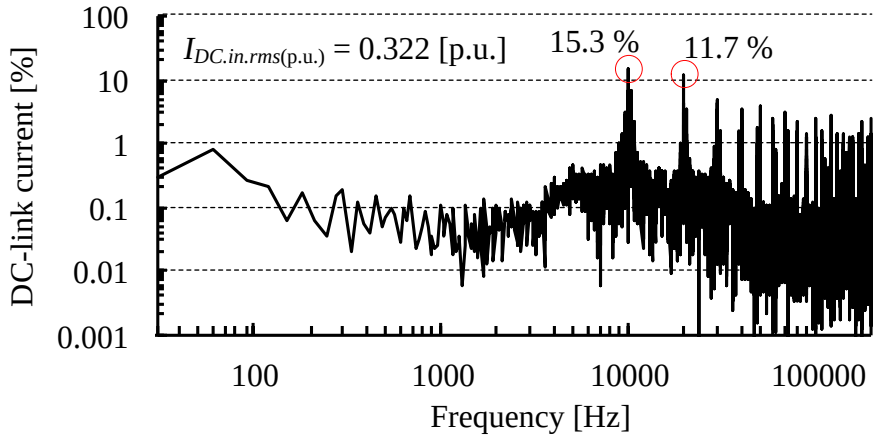
(a) Conventional CPWM. (b) Proposed CPWM.

Fig. 4.11. PLECS simulation results with each modulation method at m = 0.550 and cos φ = 0.866 (30° lagging) (under same conditions of experiments in Fig. 4.10).

Fig. 4.12 shows the harmonic components of the dc-link current under the same conditions as in Fig. 4.10. Even though the employment of the proposed CPWM worsens the first switching-frequency harmonic component of the dc-link current, the integer multiple components of the switching frequency are reduced compared to those with the conventional CPWM. Consequently, the proposed CPWM reduces the dc-link current harmonics $I_{DC.in.rms(\text{p.u.})}$ by 24.2%.



(a) Conventional CPWM.

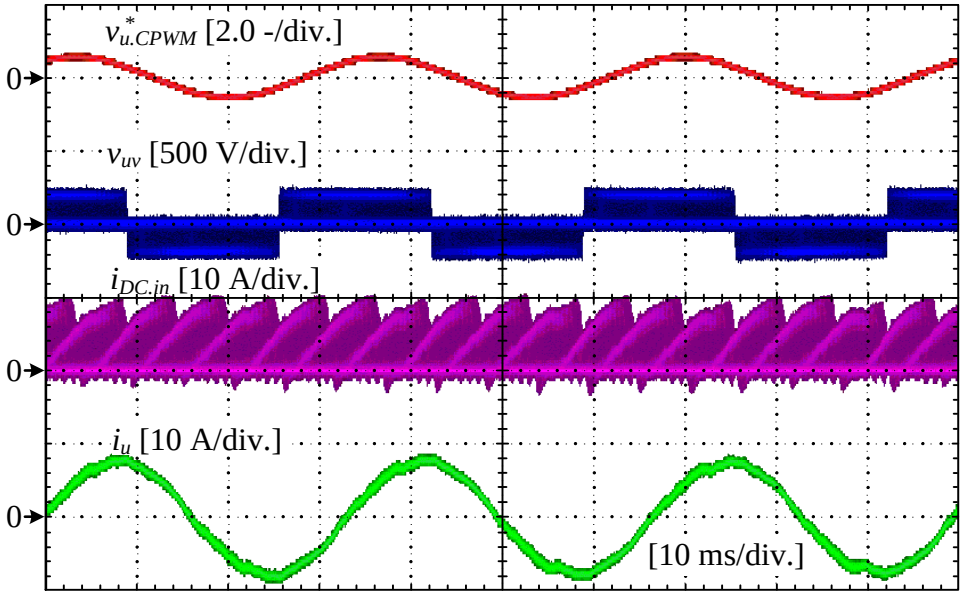


(b) Proposed CPWM.

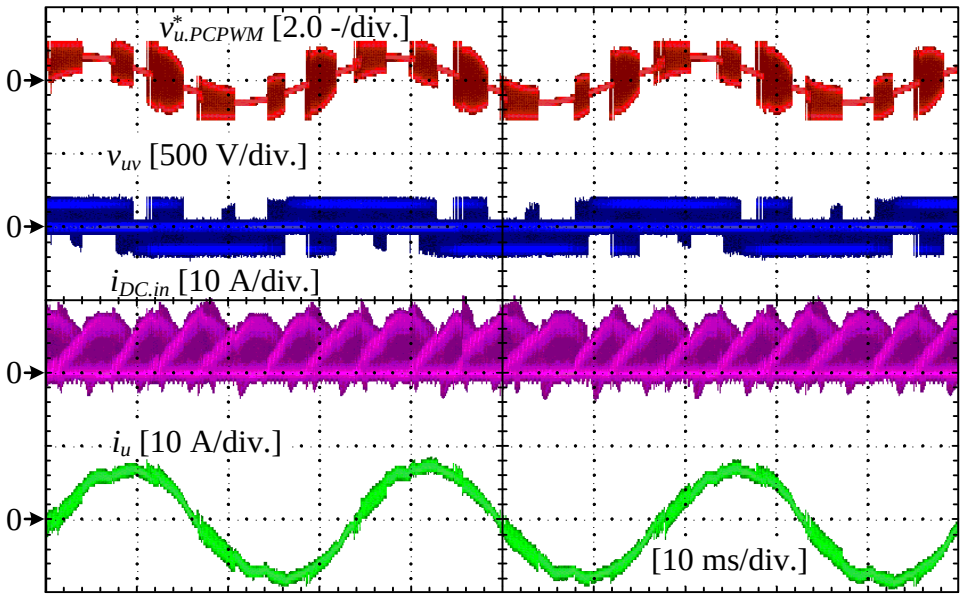
Fig. 4.12. Harmonic components of dc-link current at m = 0.550 and cos φ = 0.866 (30° lagging), i.e., driving mode with high-load power factor (under same conditions as in Fig. 4.10).

Figs. 4.13–4.14 show the VSI operating waveforms and the harmonic components of the dc-link current at the modulation index of 0.550 and the load power factor of 0.643 (50° lagging), i.e., low-load power factor condition in driving mode. When the load power factor is 0.643, the periods where the proposed shifted modulating signals are not adequate for reduction of the dc-link current harmonics arise. Therefore, the sinusoidal modulating signals are partially applied in these periods. The results show that the proposed CPWM reduces the dc-link current harmonics by 10.2%. These results demonstrate that the proposed CPWM is effective in reducing the dc-link current harmonics even when the load power factor is low.

Fig. 4.15 shows the analytic and experimental results of the dc-link current harmonic at the load power factor from 0.259 to 0.866, i.e., driving mode. The proposed CPWM reduces the dc-link current harmonics under any conditions of the modulation index and the load power factor. A higher load power factor enables a greater reduction effect on the dc-link current harmonics to be obtained. This trend is resulted from the relationship between φ and the application ratio of the shifted modulating signals in the whole phase range, observed in Fig. 4.7.

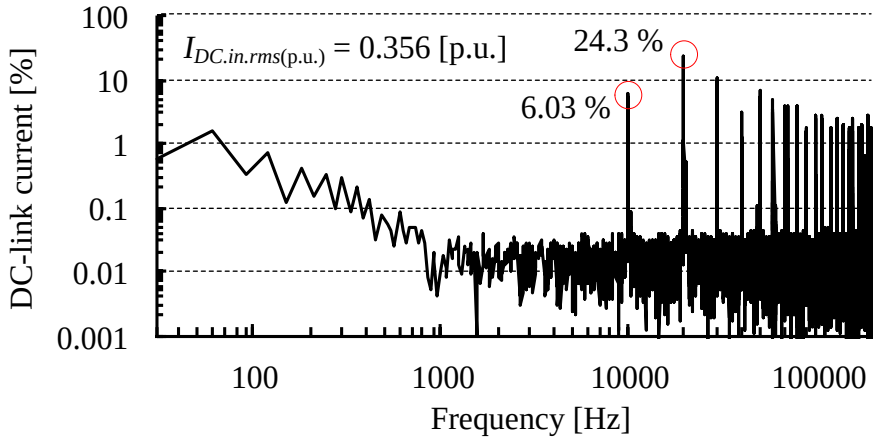


(a) Conventional CPWM.

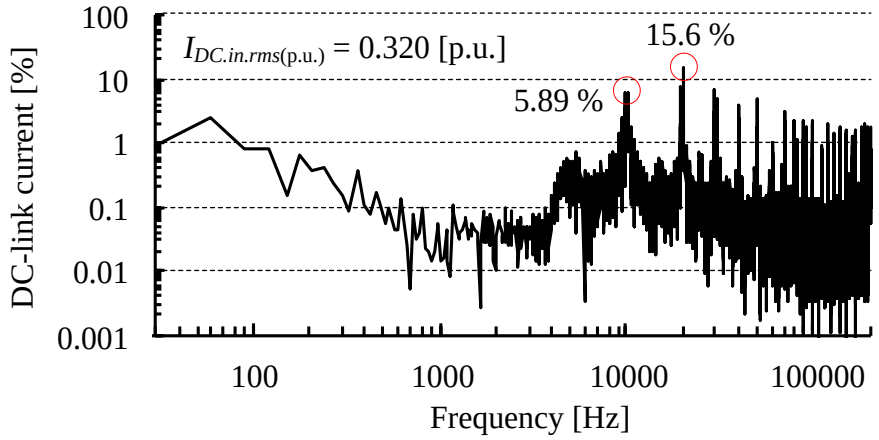


(b) Proposed CPWM.

Fig. 4.13. Experimental waveforms at m = 0.550 and cos φ = 0.643 (50° lagging), i.e., driving mode with low-load power factor; u-phase modulating signal, output line-to-line voltage, dc-link current, and u-phase output current.

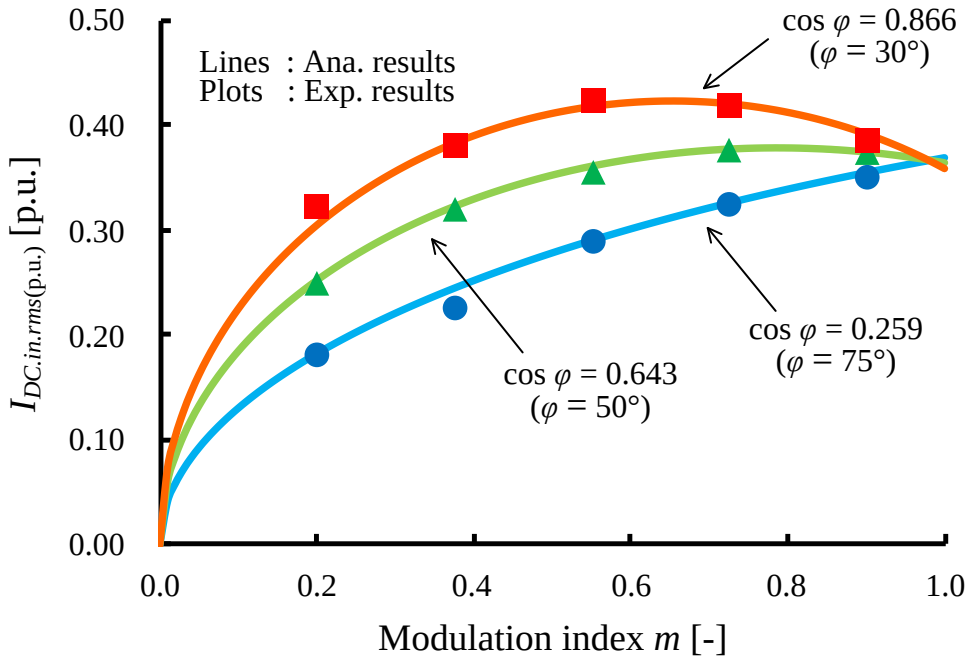


(a) Conventional CPWM.

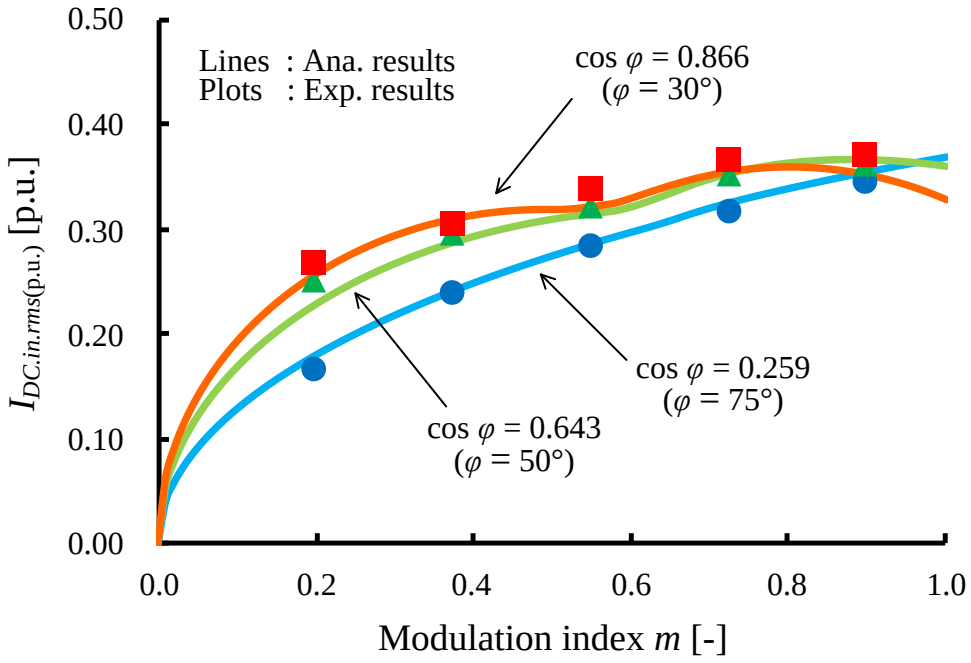


(b) Proposed CPWM.

Fig. 4.14. Harmonic components of dc-link current at m = 0.550 and cos φ = 0.643 (50° lagging), i.e., driving mode with low-load power factor (under same conditions as in Fig. 4.13).



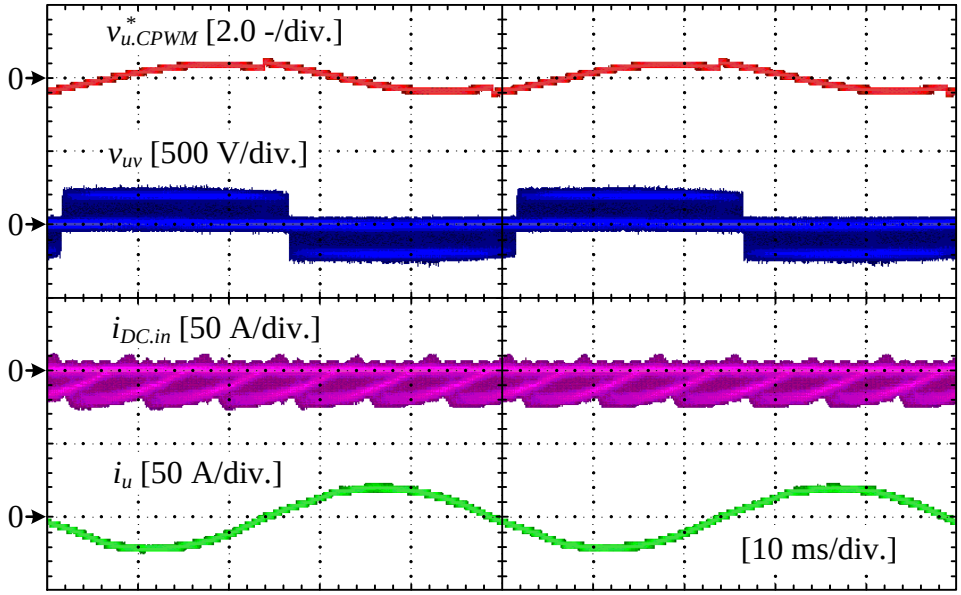
(a) Conventional CPWM.



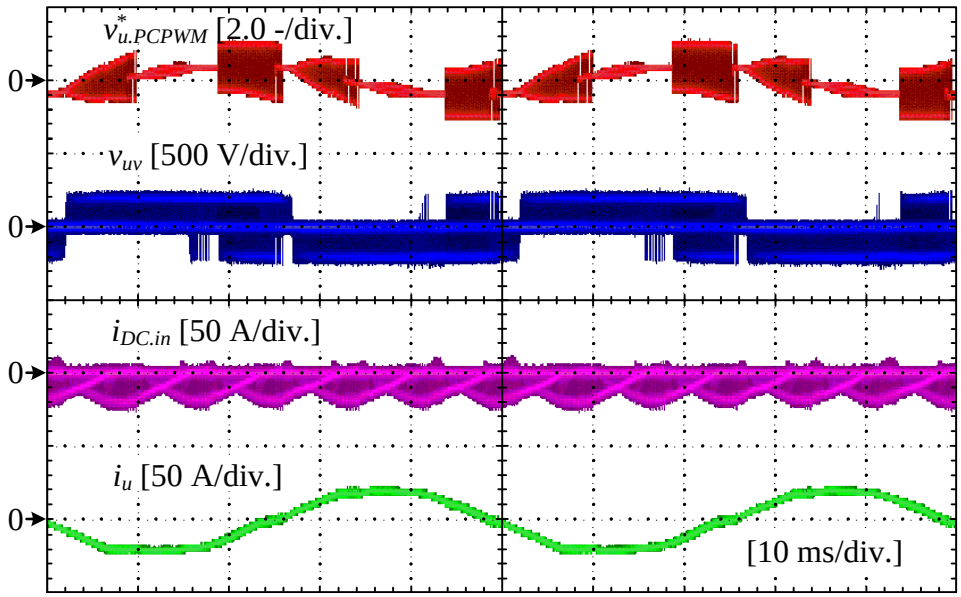
(b) Proposed CPWM.

Fig. 4.15. Measured dc-link current harmonics in driving mode.

Figs. 4.16–4.17 show the VSI operating waveforms and the harmonic components of the dc-link current at the modulation index of 0.445 and the load power factor of –0.766 (140° lagging), i.e., regenerative braking mode. The application of the proposed CPWM reduces the dc-link current harmonics even in the regenerative braking mode. These results verify that the proposed CPWM is effective in reducing the dc-link current harmonics for the AC motor drive system, of which the variation of the load power factor is considerably wide.

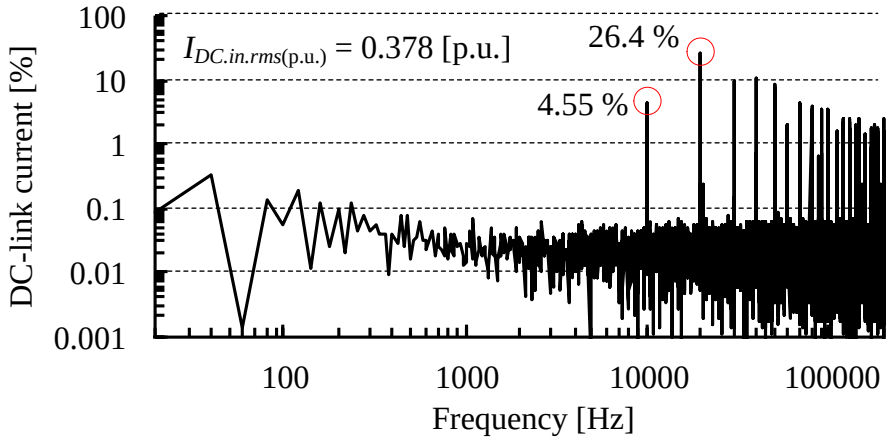


(a) Conventional CPWM.

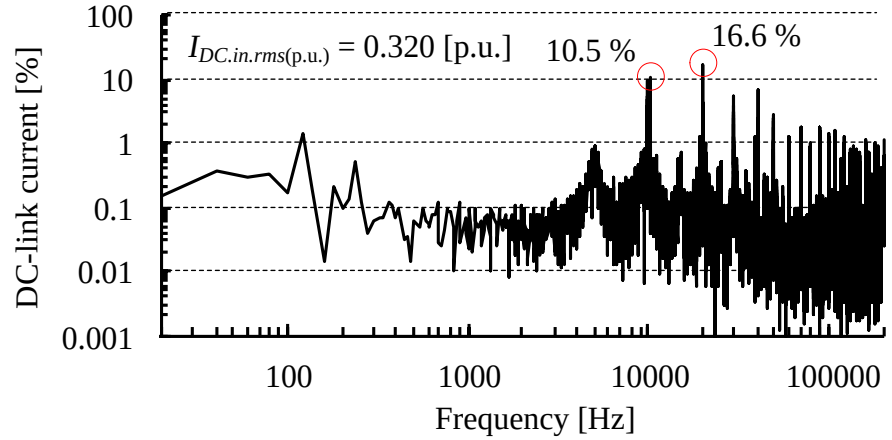


(b) Proposed CPWM.

Fig. 4.16. Experimental waveforms at m = 0.445 and cos φ = –0.766 (140° lagging), i.e., regenerative braking mode; u-phase modulating signal, output line-to-line voltage, dc-link current, and u-phase output current.



(a) Conventional CPWM.



(b) Proposed CPWM.

Fig. 4.17. Harmonic components of dc-link current at m = 0.445 and cos φ = –0.766 (140° lagging), i.e., regenerative braking mode (under same conditions as in Fig. 4.16).

4.4.2. Output Phase Current Harmonics

Fig. 4.18 shows the total harmonic distortion (THD) of the *u*-phase output current at the load power factor of 0.866. These characteristics are similar to the analytic results of the harmonic flux rms value shown in Fig. 4.9. The proposed CPWM increases the distortion of the output phase current compared to those with the conventional CPWM. Therefore, the application of the proposed CPWM results in a trade-off between the improved dc-link current harmonics and the worsened ac current harmonics. However, the worsened output current THD with the proposed CPWM can be improved by increasing the switching frequency when the inductive load is connected. The higher switching frequency leads to the increase of the switching losses; however, these impacts on the inverter efficiency can be reduced by applying wide band gap devices such as SiC or GaN.

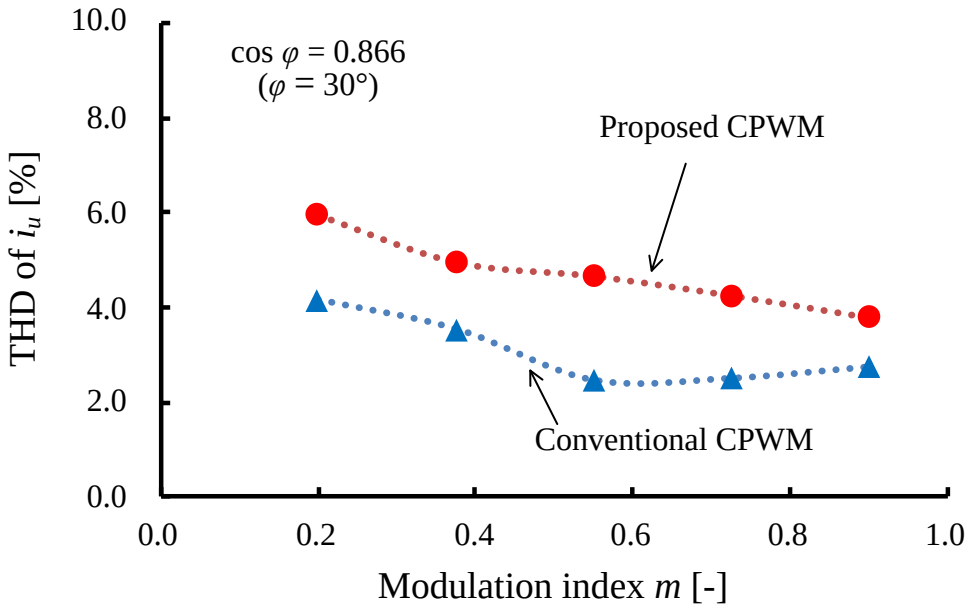


Fig. 4.18. Total harmonic distortion (THD) of *u*-phase output current at cos φ = 0.866 (30° lagging).

4.4.3. Inverter Efficiency

Fig. 4.19 show the VSI efficiency between the conventional and proposed CPWM at the load power factor of 0.866. The application of the proposed CPWM does not influence on the inverter efficiency and the same level efficiency with the conventional CPWM to be obtained due to its same number of switching transitions compared with the conventional CPWM, which is observed from Figs. 4.3–4.4.

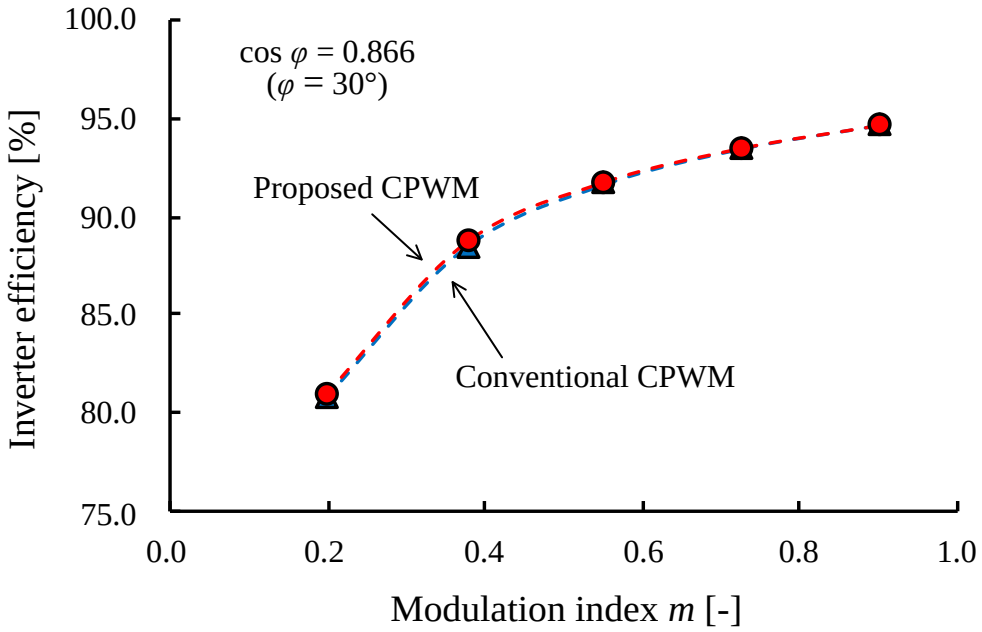
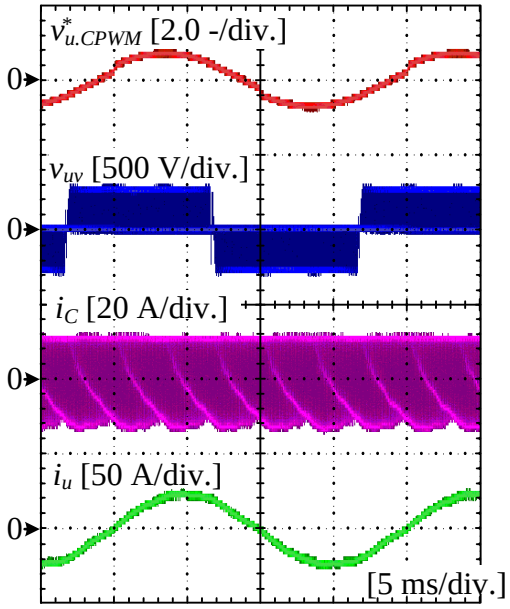


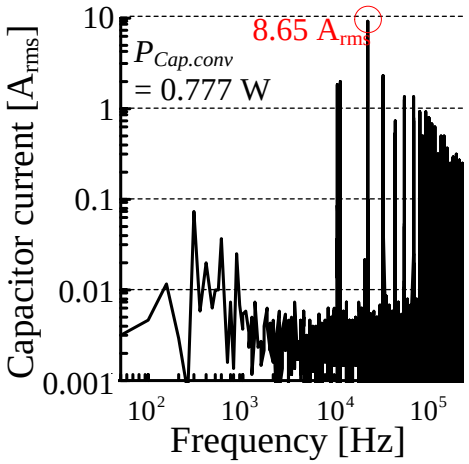
Fig. 4.19. Inverter efficiency comparison between conventional CPWM and proposed CPWM against different modulation index at cos φ = 0.866 (30° lagging).

4.4.4. DC-link Film Capacitor Heating

Figs. 4.20–4.21 show the VSI operating waveforms and the harmonic components of the dc-link capacitor current through the temperature rise test at the modulation index of 0.643, the load power factor of 0.891, and the inverter output power P_{inv} of 2.7 kW. The measured inverter efficiency was 95.27% with the conventional CPWM, whereas the efficiency was 95.17% with the proposed CPWM. The proposed CPWM reduces the capacitor loss by 31.7% compared to those obtained by the conventional CPWM.

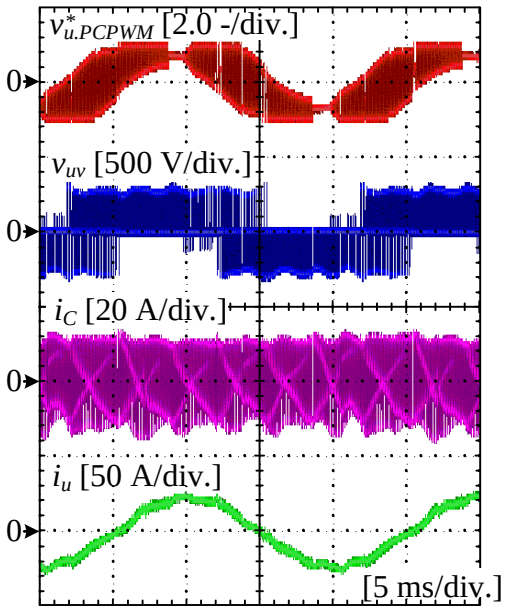


(a) Operating waveforms.

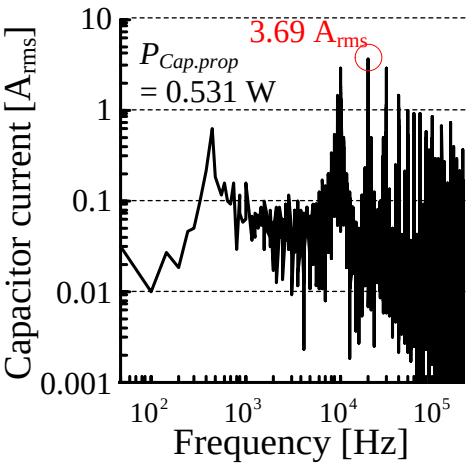


(b) Harmonic spectrum of i_C.

Fig. 4.20. VSI operating waveforms and harmonic components of dc-link capacitor current with conventional CPWM at m = 0.643, cos φ = 0.891 (27° lagging), and P_{inv} = 2.7 kW.



(a) Operating waveforms.



(b) Harmonic spectrum of i_C.

Fig. 4.21. VSI operating waveforms and harmonic components of dc-link capacitor current with proposed CPWM at m = 0.643, cos φ = 0.891 (27° lagging), and P_{inv} = 2.7 kW.

Fig. 4.22 shows the measured capacitor core temperature. These results confirm the capacitor temperature difference of 4.4°C after 7200 seconds. Furthermore, the proposed CPWM lowers the equilibrium capacitor temperature, which is estimated from the test results using the least-square method, by 6.0°C compared to the conventional CPWM. In other words, the proposed CPWM reduces the film capacitor heating by 8.92% compared to the conventional CPWM. However, the capacitor temperature difference with the conventional and proposed CPWM is smaller than those with the SVPWM approach, shown in Fig. 3.28. This is because the reduction effect on the dc-link capacitor current stress with the proposed CPWM is inferior as compared with the proposed SVPWM due to the following constrains of the proposed CPWM:

1. Zero-sequence signal injection into the modulating signals is not applied.
2. Gate pulse generation based on the triangular-carrier comparison with the modulating signals, which are updated twice in each control period.

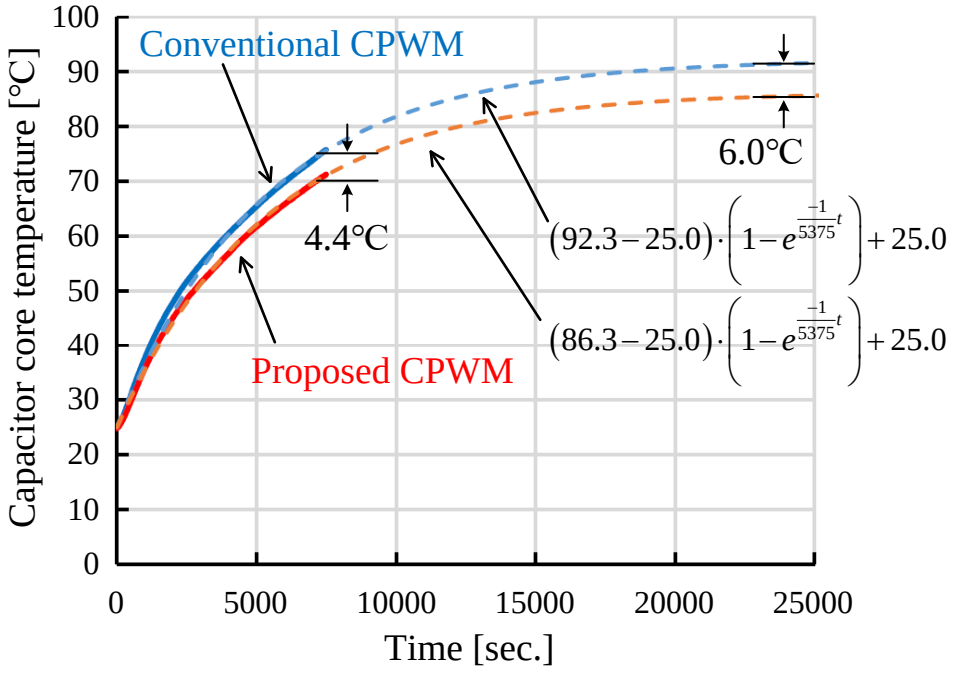


Fig. 4.22. Measured capacitor core temperature and its approximated curve with conventional and proposed CPWM.

Fig. 4.23 shows the harmonic spectrum of *u*-phase output current under the same experimental conditions as in Figs 4.20–4.21. The proposed CPWM worsens the phase current THD compared to the conventional CPWM also in these experimental conditions. However, those THD with the proposed CPWM are superior to those with the proposed SVPWM, shown in Fig. 3.29. This is because the proposed continuous modulating signals does not contain any triplen harmonics, while the proposed SVPWM has the triplen harmonics. This is the big advantage of the proposed CPWM; the dc-link capacitor current stress reduction is achievable with the slight deterioration of the output phase current distortion.

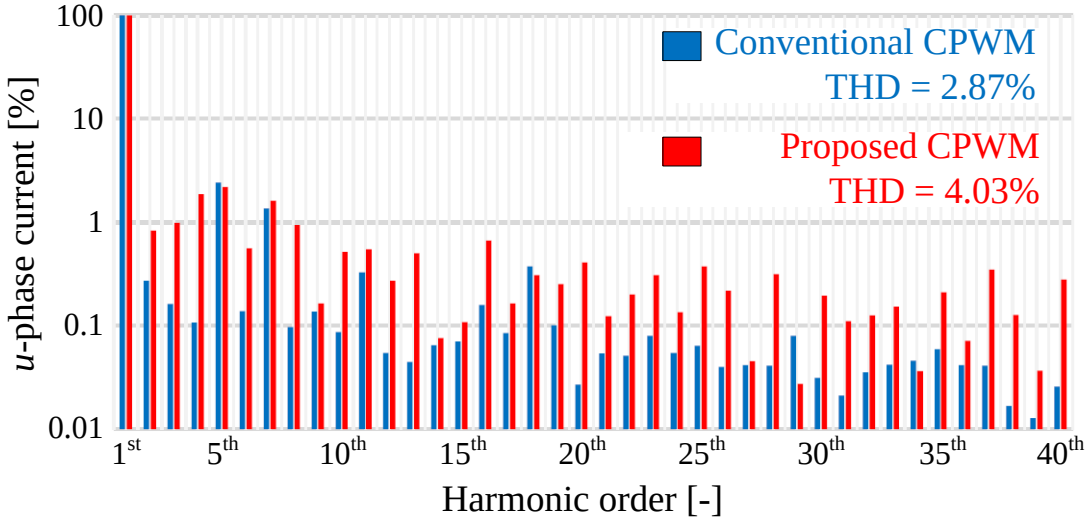
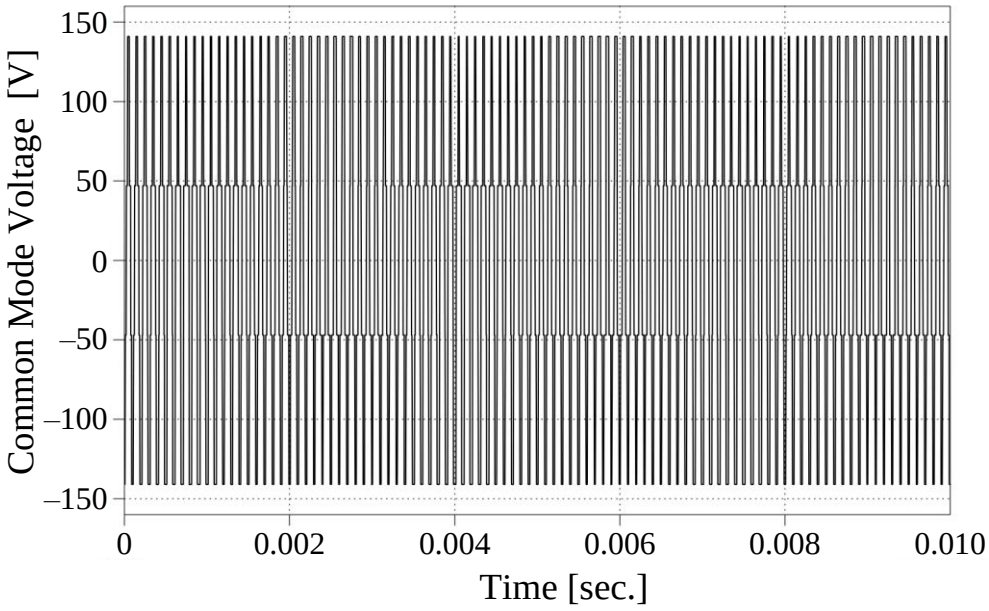
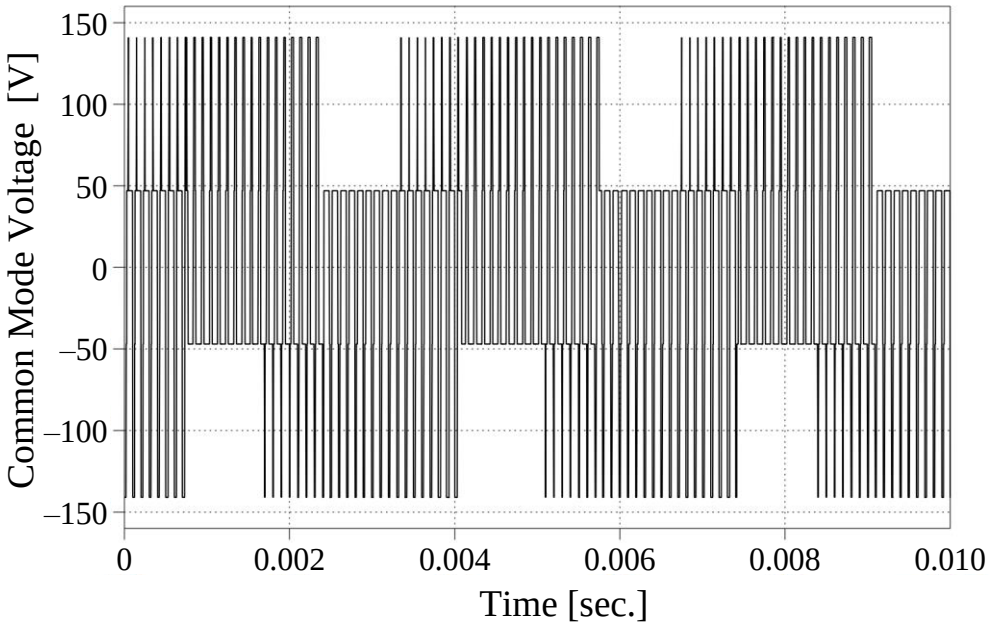


Fig. 4.23. i_u harmonic spectrum and its THD at m = 0.643, cos φ = 0.891 (27° lagging), and P_{inv} = 2.7 kW (under same conditions as in Figs. 4.20–4.21).

Figs. 4.24–4.25 show the PLECS simulation results of common-mode voltage waveforms and the harmonic components at the modulation index of 0.643, the load power factor of 0.891. Note that the fundamental frequency is set to 100 Hz for the simplification of the harmonic analysis, whereas the switching frequency is 10 kHz. Fig. 4.24 demonstrates that the step change of the common-mode voltage is reduced with the proposed CPWM. Fig. 4.25 also confirms that the switching frequency component of the common-mode voltage is reduced with the proposed CPWM. On the other hand, the higher switching frequency components up to 30 MHz are deteriorated with the proposed CPWM due to an absence of the gate pulse symmetry about the center of the control period. This might lead to the bulky common-mode filter compared to those with the conventional CPWM.

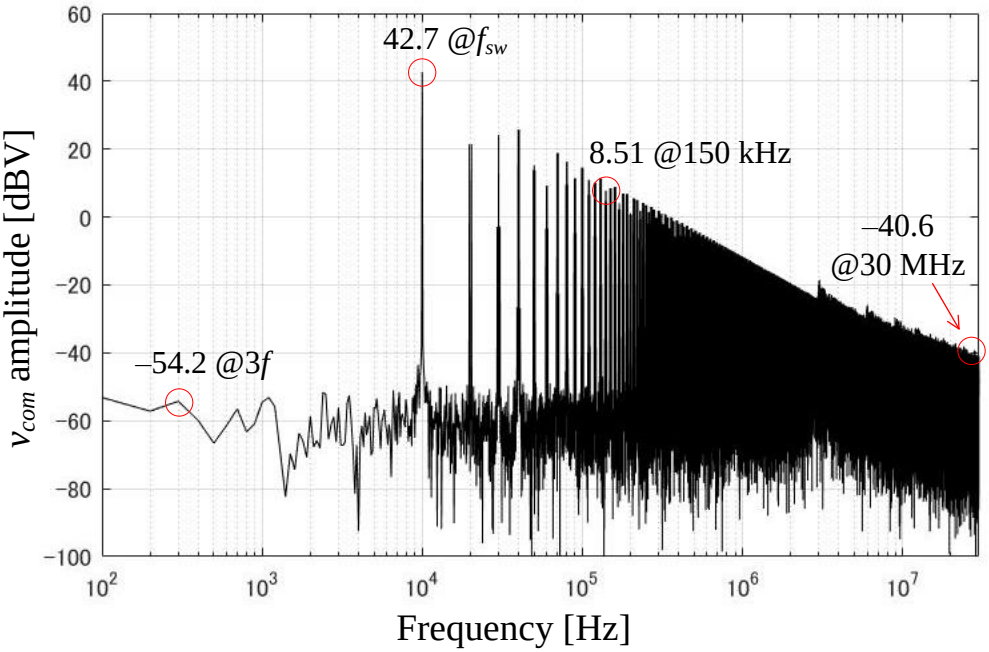


(a) Conventional CPWM.

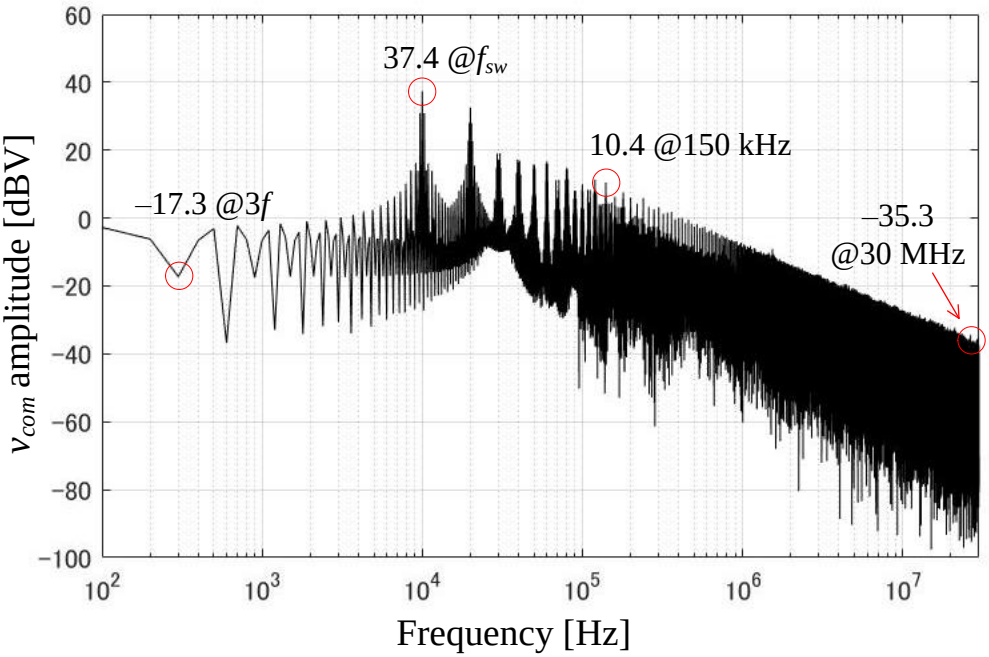


(b) Proposed CPWM.

Fig. 4.24. PLECS simulation results of common-mode voltage at m = 0.643, cos φ = 0.891 (27° lagging) (under same conditions as in Figs. 4.20–4.21 except for fundamental frequency of 100 Hz).



(a) Conventional CPWM.



(b) Proposed CPWM.

Fig. 4.25. v_{com} harmonic spectrum at m = 0.643, cos φ = 0.891 (27° lagging) (under same conditions as in Figs. 4.20–4.21 except for fundamental frequency of 100 Hz).

4.5. Electrolytic Capacitor Lifetime Estimation

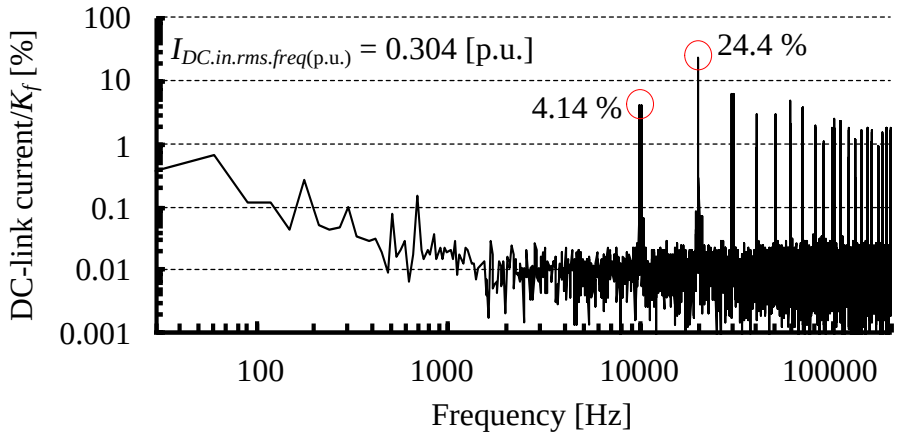
Fig. 4.26 shows the harmonic components of the dc-link current considering the frequency dependence of the ESR of aluminum electrolytic capacitor (NX series, Nichicon Corp. [4-4]) at the modulation index of 0.550 and the load power factor of 0.866 (under the same conditions as in Fig. 4.10). The expected lifetime (L_n) of the electrolytic capacitors is calculated as the same manner as introduced in the chapter 3.6. The proposed CPWM reduces the dc-link current harmonics $I_{DC.in.rms.freq}$(p.u.) by 23.4% when the frequency dependence of the ESR of aluminum electrolytic capacitor is considered. Assuming that the motor is mostly operated at the modulation index of 0.550 and the load power factor of 0.866, and the aluminum electrolytic capacitors in the conventional CPWM are designed at the worst case of the rated ripple current (i.e., F_I as 1), the lifetime expectancy of the electrolytic capacitor can be given by

$$L_{n\_conv.CPWM} = L_o \times 1 = 5000 \text{ h.} \quad \text{.....(4.3)}$$

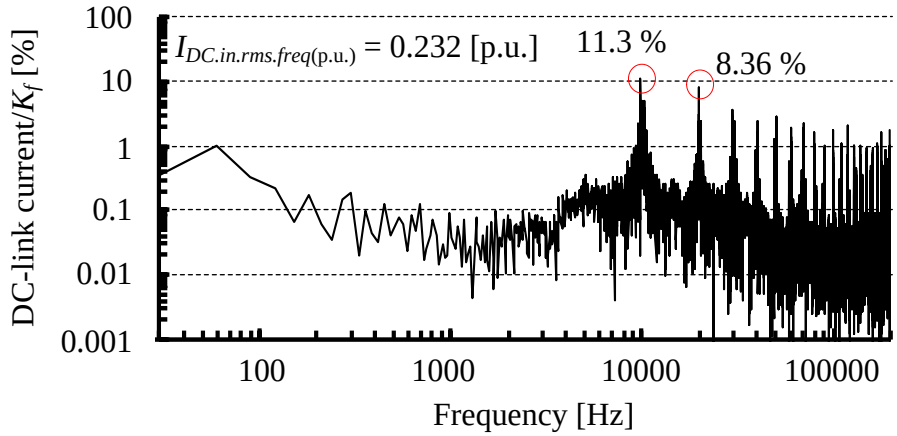
On the other hand, the application of the proposed CPWM raises F_I to 1.33 due to a current harmonic reduction of 23.4%. So, the lifetime expectancy of the electrolytic capacitor with the proposed CPWM can be given by

$$L_{n\_prop.CPWM} = L_o \times 1.33 = 6650 \text{ h.} \quad \text{.....(4.4)}$$

It is concluded that the application of the proposed CPWM might extend the lifetime of the electrolytic capacitor about 1.33 times longer at most than that of the conventional CPWM.



(a) Conventional CPWM.



(b) Proposed CPWM.

Fig. 4.26. Harmonic components of dc-link current considering frequency dependence of ESR of aluminum electrolytic capacitor at m = 0.550 and cos φ = 0.866 (30° lagging) (under same conditions as in Fig. 4.10).

4.6. Conclusion

The proposed CPWM in this chapter achieves the dc-link capacitor current stress reduction by the carrier-based PWM strategy which is available with the general-purpose micro-computer. The dc-link capacitor current rms values were reduced by shifting the classical continuous modulating signals in every half control period based on the load current sector to reduce the dc-link current fluctuates around its average value. In comparison with the conventional CPWM, the proposed CPWM reduced the dc-link current harmonics by 23.4%, might be leading to the 1.33 times lifetime extension of the electrolytic capacitors. Moreover, the proposed CPWM reduced the capacitor loss by 31.7%, lowering the equilibrium capacitor temperature by 6.0℃ (8.92%). Consequently, the proposed CPWM also contributes into the reductions of the dc-link capacitor current stress and the dc-link capacitor thermal stress as well as the proposed SVPWM introduced in chapter 3. The proposed CPWM has following advantages and disadvantage:

1. The dc-link capacitor current stress reduction is achievable with the slight deterioration of the output phase current distortion compared with the proposed SVPWM in chapter 3 (Advantage).
2. The proposed CPWM is achievable only with the low-cost digital hardware such as micro-computer, which is used in the electric vehicle applications where the high power density is highly desired (Advantage).
3. The maximum voltage transfer ratio is limited to 0.866 (Disadvantage).

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Chapter 5

Carrier-based Discontinuous PWM Strategy for DC-link Capacitor Current Stress Reduction

5.1. Introduction

This chapter presents an implementation method for the PWM switching patterns to reduce the dc-link capacitor current stress in the two-level three-phase VSI based on the carrier-based discontinuous PWM (DPWM) strategy. The difference between this DPWM strategy and the proposed CPWM in chapter 4 is that there is degree of freedom of the zero-sequence signal injection with the DPWM approach. Specifically, the injected zero-sequence signal is determined based on the load current sector to adapt to the load power factor variation. The advantages of the proposed DPWM is the greater reduction for the dc-link capacitor current stress compared with those with the proposed CPWM only with the low-cost digital hardware such as a general-purpose micro-computer, which is used in the electric vehicle applications where the high power density is highly desired. Furthermore, the maximum voltage transfer ratio of 1.0 is achieved with this proposed DPWM, extending the available motor operating region, whereas the ratio is limited to 0.866 in the proposed CPWM strategy.

This chapter is organized as follows: First, in chapter 5.2, the reduction methods of the dc-link current harmonics by using the shifted modulating signals and injecting the proper zero-sequence signal based on the load current sector are explained in detail. Next, in chapter 5.3 and chapter 5.4, analytical, simulation, and experimental results are presented to verify the effectiveness in terms of the reduction of the dc-link current harmonics, the impact on the output phase current quality, inverter efficiency, and the dc-link capacitor heating. After that, in chapter 5.5, the lifetime of the electrolytic capacitors is estimated and compared. Finally, in chapter 5.6, the conclusion of this chapter will be presented.

5.2. Proposed Discontinuous Modulating Signals

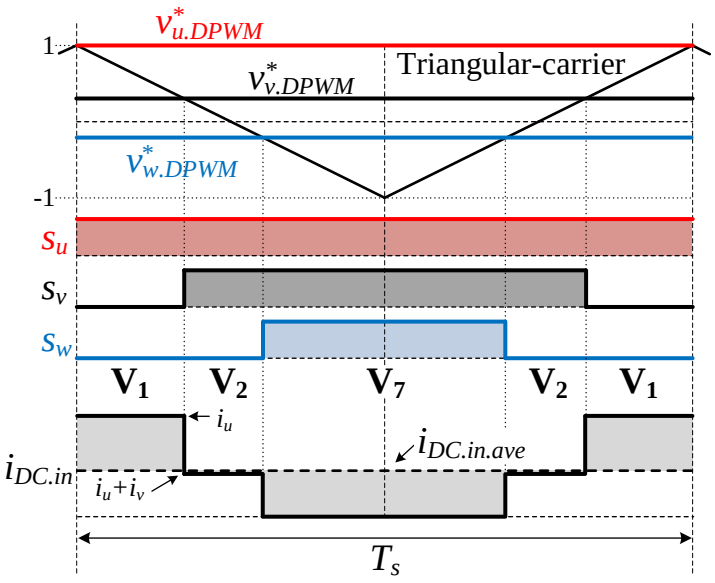
5.2.1 Proposed Modulating Signals for DC-link Current Harmonic Reduction

Fig. 5.1 shows the zoomed-in waveforms of the conventional and proposed discontinuous modulating signals, the switching functions, and the dc-link current at the modulation index of 0.7, the phase angle of 25°, and the load power factor of 0.866. When the conventional DPWM is applied as shown in Fig. 5.1(a), the centers of the three-phase gate pulses are matched to the center of the control period, leading a long overlap period of the gate pulses. As a result, the large difference between the dc-link current $i_{DC.in}$ and its average value $i_{DC.in.ave}$ occurs especially when the voltage space vectors $\mathbf{V_1}$ and $\mathbf{V_7}$ are applied. This results in a large dc-link current fluctuations around its average value, i.e., the large dc-link capacitor current harmonics. Therefore, the basic concept of the proposed DPWM for the dc-link current harmonic reduction is to shorten the duty cycle of zero-vector $\mathbf{V_0}$ or $\mathbf{V_7}$ during the control period, leading to the reduction of the dc-link current fluctuations around its average value. Also in the proposed DPWM, this concept is achieved under the premise that the modulating signals are to be updated at positive-peak and negative-peak of the triangular-carrier with the micro-computer, as well as the proposed CPWM in chapter 4. In order to adjust the gate pulse timings as shown in Fig. 5.1(b), only two unclamped phases' modulating signals $v^*_{v.DPWM}$ and $v^*_{w.DPWM}$ should be updated, whereas the originally clamped modulating signal $v^*_{u.DPWM}$ is not updated. Those modulating signals are generated by shifting the originally unclamped discontinuous modulating signals as

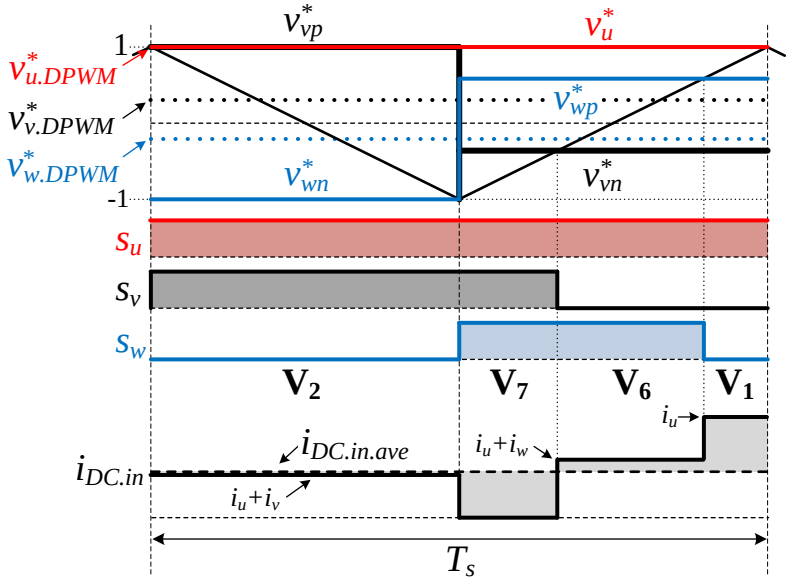
$$\begin{cases} v^*_{xp} = 1 \\ v^*_{xn} = 2 \cdot v^*_{x.DPWM} - 1 \end{cases} \quad \text{if } v^*_{x.DPWM} \geq 0,$$
$$\begin{cases} v^*_{xp} = 2 \cdot v^*_{x.DPWM} + 1 \\ v^*_{xn} = -1 \end{cases} \quad \text{if } v^*_{x.DPWM} \leq 0, \qquad \text{.....(5.1)}$$

where v^*_{xp} ($x = u, v, w$) is the positively-shifted modulating signal, and v^*_{xn} is the negatively-shifted modulating signal. Note that the overlap period between two unclamped phases' switching functions, s_v and s_w in Fig. 5.1, should be shortened to reduce the dc-link current fluctuations around its average value. Therefore, those two phases' modulating signals are shifted alternately to the positive side. Besides, the averaged values of the shifted modulating signals over each control period are same as those of the original signals; thus, the pulse widths of the switching functions are unchanged. Finally, the duty cycles of $\mathbf{V_1}$ and $\mathbf{V_7}$, causing the large dc-link current difference against its average value, are shortened, in contrast, the duty cycles of $\mathbf{V_2}$ and $\mathbf{V_6}$, leading to the quite small dc-link current difference against its average value, are extended and generated with the shifted discontinuous modulating signals as shown in Fig. 5.1(b).

However, note that the reduction effect on the dc-link current harmonics by the use of the shifted modulating signals is dependent on the load power factor because the dc-link current is also dependent on the output phase currents according to (2.11) and (2.12). Thus, it is necessary to deal with the wide variation of the load power factor, which is a typical requirement of the AC motor drive system.



(a) Conventional DPWM.



(b) Proposed DPWM.

Fig. 5.1. Zoomed-in waveforms of modulating signals, switching functions, and dc-link current at m = 0.7, $2\pi ft$ = 25°, and cos φ = 0.866 (30° lagging).

5.2.2 Zero-sequence Signal Injection to Adapt to Load Power Factor Variation based on Load Current Sector

In order to recognize the load current conditions, the load current sectors (A–F), defined in Table 3.2, are used also in the proposed DPWM. In a carrier-based discontinuous PWM, the zero-sequence signal is injected into the sinusoidal modulating signals to achieve the voltage transfer ratio extension and the reduction for the number of total switching transitions [5-1]–[5-3]. Since the neutral current path in the AC motor load is absence, there is a degree of freedom in determining the zero-sequence signal. The proposed DPWM uses the degree of freedom in order to reduce the dc-link capacitor current harmonics in wide range of the load power factor.

Table 5.1 lists the modulating signal to be clamped and its optimized clamped value K_{OCV} at each load current sector for the reduction of the dc-link current harmonics. In each load currents' condition, the phase, with the clamped modulating signal, is important to achieve the dc-link current harmonics reduction by shifting the other two unclamped phases' modulating signals in every half control period. In addition, the clamped value (1 or –1) of the clamped modulating signal is also important.

TABLE 5.1.
MODULATING SIGNAL TO BE CLAMPED AND ITS OPTIMIZED CLAMPED VALUE AT EACH LOAD CURRENT SECTOR.

Load current sector	Current directions (P: Positive, N: Negative)			Driving mode		Reg. braking mode	
	i_u	i_v	i_w	Mod. Signal to be clamped	K_{OCV}	Mod. Signal to be clamped	K_{OCV}
A	P	N	N	$v_{u.DPWM}$	1	$v_{u.DPWM}$	–1
B	P	P	N	$v_{w.DPWM}$	–1	$v_{w.DPWM}$	1
C	N	P	N	$v_{v.DPWM}$	1	$v_{v.DPWM}$	–1
D	N	P	P	$v_{u.DPWM}$	–1	$v_{u.DPWM}$	1
E	N	N	P	$v_{w.DPWM}$	1	$v_{w.DPWM}$	–1
F	P	N	P	$v_{v.DPWM}$	–1	$v_{v.DPWM}$	1

Fig. 5.2 shows the conventional and proposed discontinuous modulating signals at the modulation index of 0.7 and the load power factor of 0.966 (15° lagging), i.e., high-load power factor. In order to reduce the dc-link current harmonics at any condition of the load power factor, first, three conventional modulating signals $v^*_{x.DPWM}$ are added with the zero-sequence signal $v^*_{offset.2}$ to obtain the modulating signals with the offset $v^*_{x.PDPWM}$ as

$$v^*_{x.PDPWM} = v^*_{x.DPWM} + v^*_{offset.2},$$

$$v^*_{offset.2} = \begin{cases} K_{OCV} - v^*_{u.DPWM} & \text{if load current sector = A, D} \\ K_{OCV} - v^*_{w.DPWM} & \text{if load current sector = B, E} \\ K_{OCV} - v^*_{v.DPWM} & \text{if load current sector = C, F} \end{cases} \quad \text{.....(5.2)}$$

where K_{OCV} is the optimized clamped value of the modulating signal in each load current sector, listed in Table 5.1. The injected zero-sequence signal $v^*_{offset.2}$ is optimized according to the conditions of the load currents and the clamped phase of the modulating signals. For the load current sector A as an example, where i_u is positive and i_v and i_w are negative, u-phase gate pulse s_u should cover the other two phase gate pulses s_v and s_w in the time domain to

avoid the $i_{DC.in}$ polarity flip compared to the $i_{DC.in.ave}$ polarity. If s_u becomes 0 during the load current sector A, the dc-link current $i_{DC.in}$ becomes negative value according to the fact that i_v and i_w are negative, whereas its average value $i_{DC.in.ave}$ is positive, which leads to a large $i_{DC.in}$ fluctuations against $i_{DC.in.ave}$. Next, two unclamped zero-sequence signal-added modulating signals $v^*_{v.PDPWM}$ and $v^*_{w.PDPWM}$ at the load current sector A are shifted alternately based on (5.1), resulting in the proposed discontinuous modulating signals v^*_x. With this optimization for the clamped phase and its value of the modulating signal based on the load current conditions, the dc-link current harmonics is reduced even when the load power factor varies.

For the regenerative braking mode, the average value of the dc-link current become a negative value. Therefore, the optimized clamped value K_{OCV} of the modulating signal for the reduction of the dc-link current fluctuations around its average value in each load current sector is reversed between driving and regenerative braking modes as listed in Table 5.1. Note that whether the motor operating mode is driving or regenerative braking is to be detected from the combinations of the voltage sector and the load current sector as listed in Table 3.3. In addition, the shifting of the other two unclamped zero-sequence signal-added modulating signals in every half control period is also performed for the regenerative braking mode as well as the driving mode.

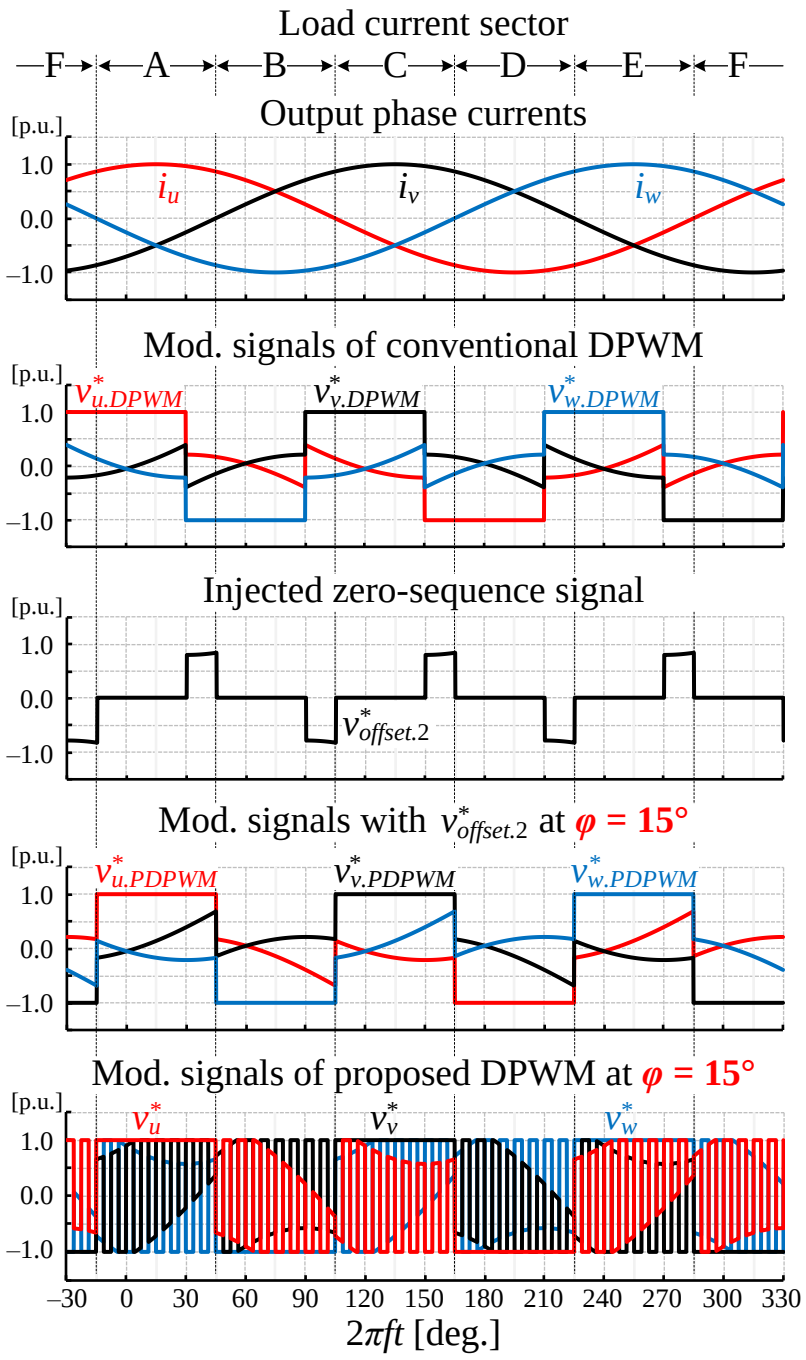


Fig. 5.2. Proposed modulating signals at m = 0.7 and cos φ = 0.966 (15° lagging), i.e., high-load power factor. $v^*_{x.PDPWM}$ is generated by adding $v^*_{offset.2}$ to $v^*_{x.DPWM}$ to maintain the clamped period of the modulating signal at each load current sector. The proposed modulating signals v^*_x are then generated by shifting two unclamped modulating signals in every half control period. The switching frequency is set to be low for better illustration.

Fig. 5.3 shows an another example of the conventional and proposed discontinuous modulating signals at the modulation index of 0.7 and the load power factor of 0.707 (45° lagging), i.e., low-load power factor. When the load power factor is lower than 0.866 ($\varphi < 30°$), the proposed zero-sequence signal-added modulating signals $v^*_{x.PDPWM}$ might be more than 1 or lower than –1 due to the addition of the zero-sequence signal $v^*_{offset.2}$ in each load current sector, leading an overmodulation operation. Therefore, the conventional DPWM is applied in these periods as shown in the gray-colored periods in Fig. 5.3. Accordingly, the phase of the clamped modulating signal is not optimized for the reduction of the DC-link current harmonics; thus, the modulating signal shift in every half control period are not performed in these periods.

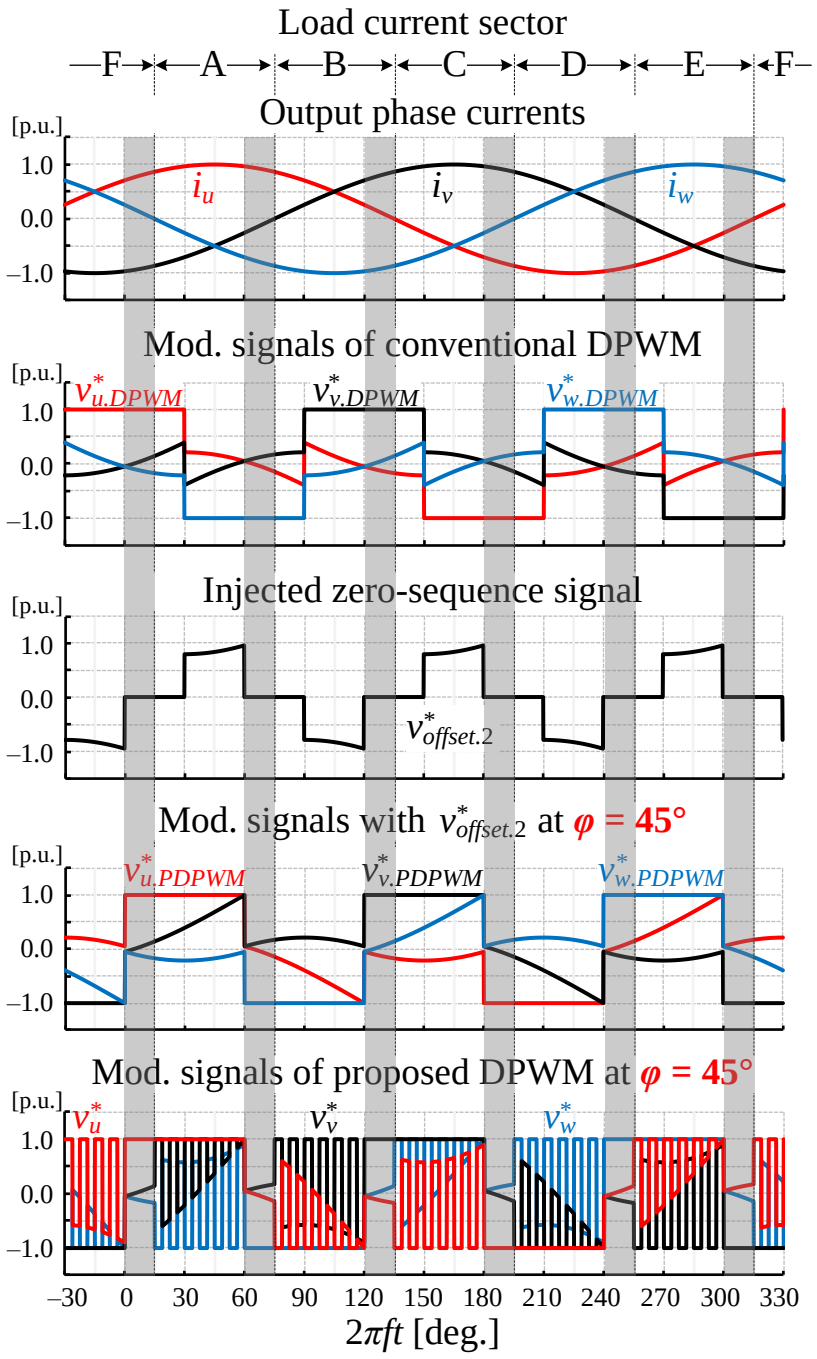


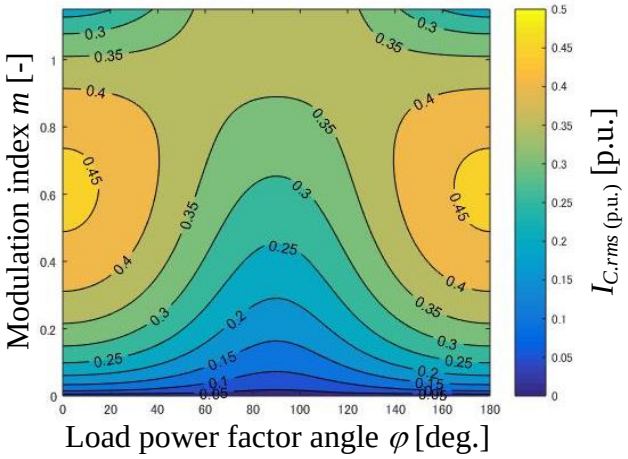
Fig. 5.3. Proposed modulating signals at m = 0.7 and cos φ = 0.707 (45° lagging), i.e., low-load power factor. At the phase ranges of 0°–15°, 60°–75°, 120°–135°, 180°–195°, 240°–255°, and 300°–315°, which are shown as gray-colored periods, the conventional DPWM is applied to avoid the overmodulation operation due to the addition of $v^*_{offset.2}$. The switching frequency is set to be low for better illustration.

5.3. Analytical Evaluations

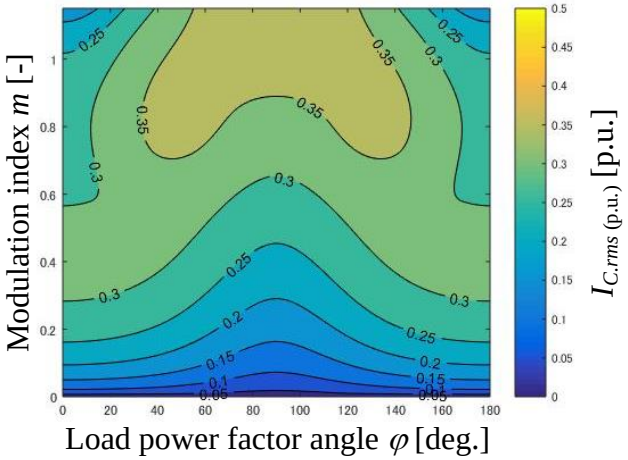
5.3.1 DC-link Capacitor RMS Current

In this chapter, the normalized dc-link capacitor rms current $I_{C.rms(\text{p.u.})}$ which is calculated as (2.13) is used for the evaluation of dc-link capacitor current harmonics reduction with the proposed DPWM.

Fig. 5.4 shows the analytical results of the dc-link capacitor current with regard to the modulation index m and the load power factor angle φ. It is demonstrated from Fig. 5.4 that the proposed DPWM provides good performance in terms of the dc-link capacitor rms current compared to the conventional DPWM under any cases of m and φ. The characteristic to reduce the harmonic components in the dc-link capacitor current is same between driving and regenerative braking modes. In addition, a higher load power factor absolute value $|\cos \varphi|$ leads to a greater reduction effect on the dc-link capacitor rms current because the application ratio of the proposed discontinuous modulating signals becomes higher as the $|\cos \varphi|$ is higher. The power factor variation range of the motor loads is dependent on the applications; e.g., the rated speed and rated torque conditions are mainly used in the fan or pump applications, whereas any speed and torque conditions should be considered in the traction applications such as train and electric vehicle. Furthermore, the load power factor is also dependent on the motor type such as induction motor (IM) or permanent magnet synchronous motor (PMSM). The actual effect on the dc-link capacitor rms current reduction could be estimated by using these analytic results with the consideration of the expected operating conditions and their occurrence frequencies in each certain application.



(a) Conventional DPWM.



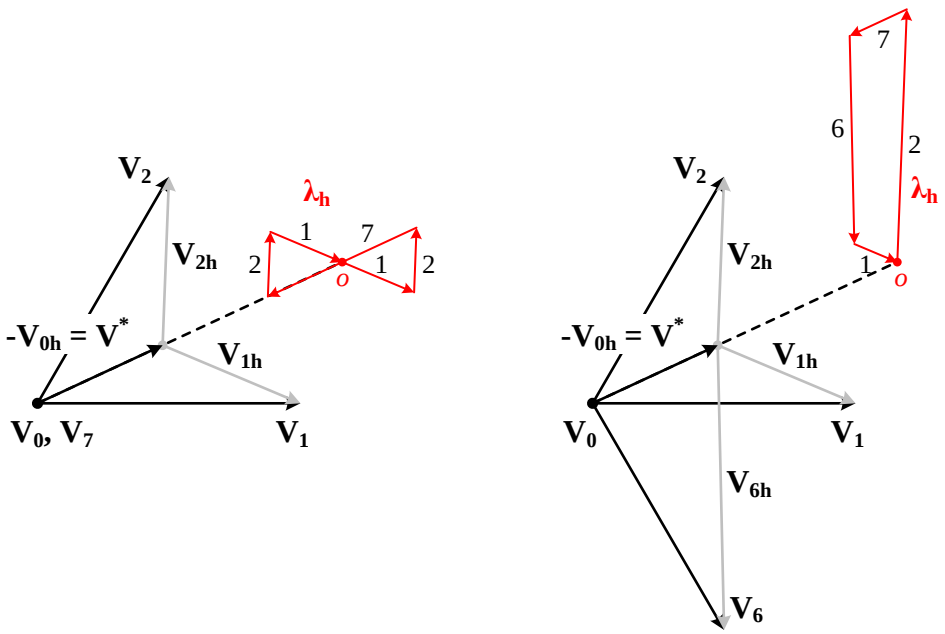
(b) Proposed DPWM.

Fig. 5.4. Analytical results of dc-link capacitor rms current with regard to modulation index m and load power factor cos φ.

5.3.2 Load Current Quality

In this chapter, the rms value of the harmonic flux over fundamental period λ_{rms} which is calculated as (3.4) is used for the evaluation of the load current quality with the proposed DPWM as well as chapter 3.4.2 and 4.3.2.

Fig. 5.5 shows an example of the harmonic flux trajectories at the modulation index of 0.7 and the phase angle of 25°, under the same analytical conditions as in Figs. 5.1. These trajectories demonstrate that the proposed DPWM leads to the longer distance between the harmonic flux trajectories and the origin *o*. Therefore, the proposed DPWM worsen the load current quality compared to the conventional DPWM.



(a) Conventional DPWM. (b) Proposed DPWM.

Fig. 5.5. Harmonic flux trajectories at m = 0.7 and $2\pi ft$ = 25°. The distance between the origin (o) and the trajectory of $\boldsymbol{\lambda_h}$ is equal to the magnitude of the harmonic flux, and continuously fluctuates.

Fig. 5.6 shows the harmonic flux rms values with the conventional DPWM and the proposed DPWM. These analytical results also confirm that the proposed DPWM increases the harmonic flux rms values compared to those with the conventional CPWM. The reason is because the proposed shifted modulating signals result in the application of the voltage space vector which is not the closest to $\mathbf{V}^*$, i.e., $\mathbf{V_6}$ in Fig. 5.5. On the other hand, only voltage space vectors which are the closest to $\mathbf{V}^*$ are employed in the conventional DPWM. Therefore, the proposed DPWM leads to worse λ_{rms}.

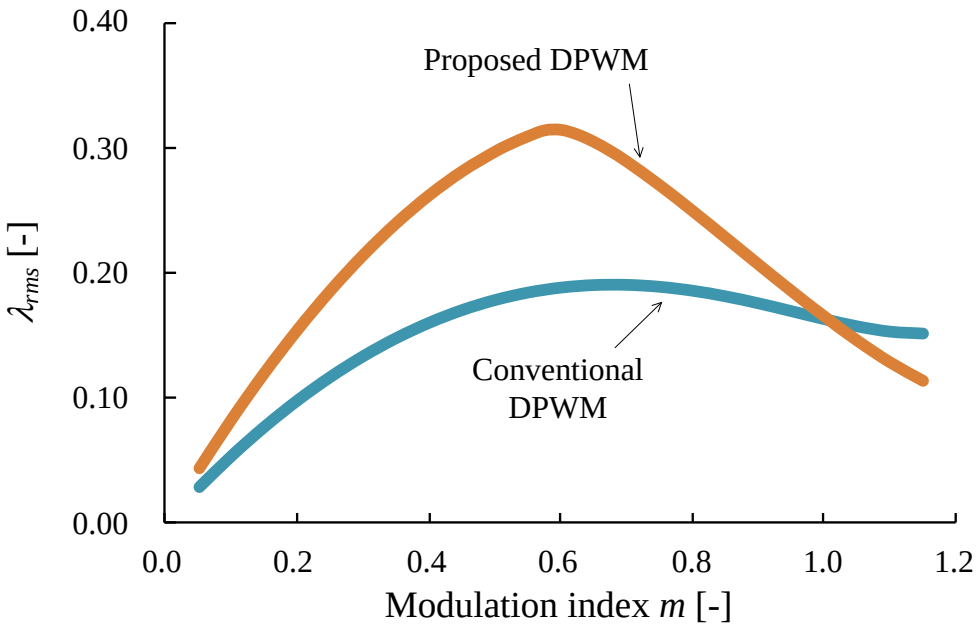


Fig. 5.6. Comparison of harmonic flux rms values with regard to modulation index. In the proposed DPWM calculations, the load power factor is set to 1.

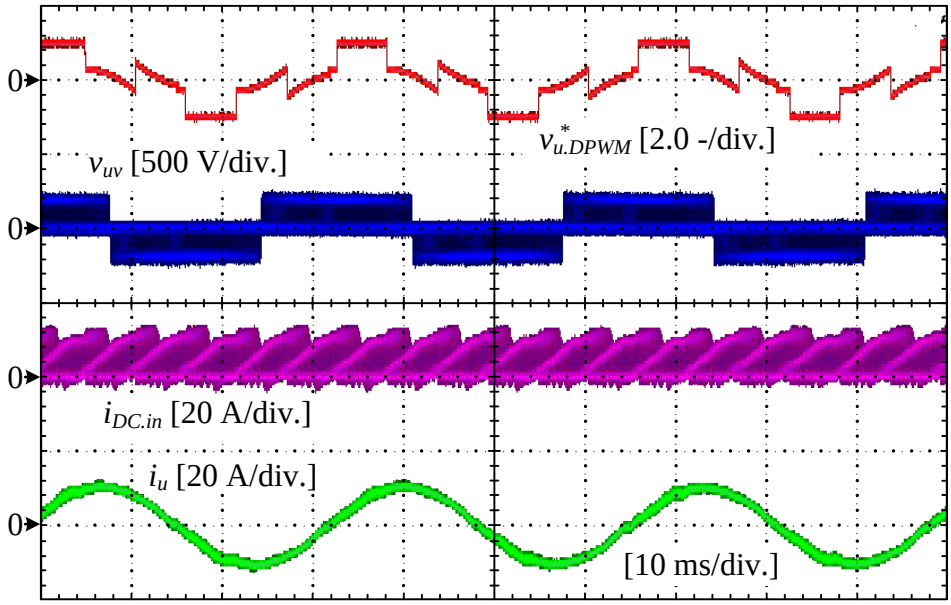
5.4. Simulation and Experimental Results

The effectiveness of the proposed DPWM was verified by the PLECS simulation and the experiment. The experimental setups were same as described in chapter 3.6.

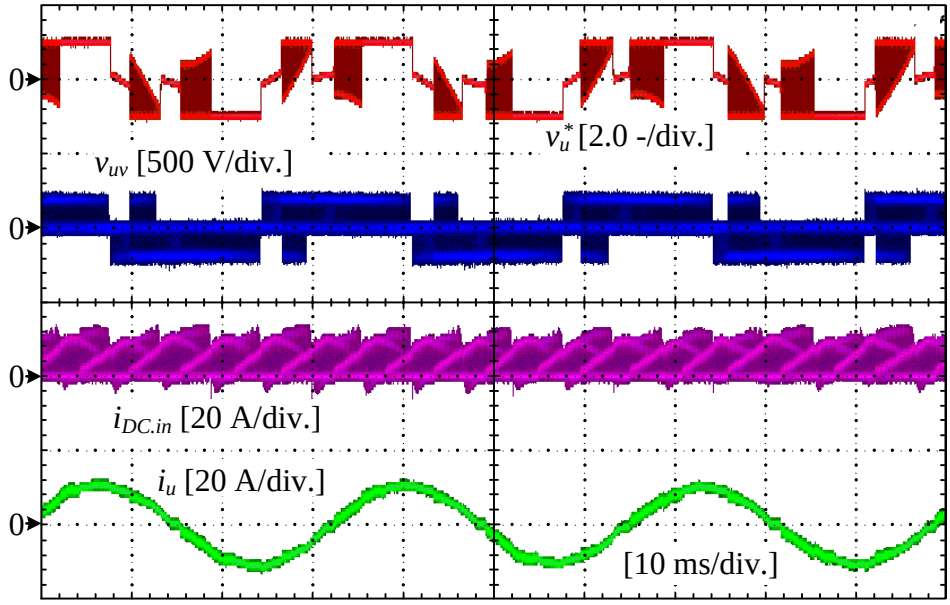
5.4.1. DC-link Current Harmonics

Fig. 5.7 shows the *u*-phase modulating signal, the line-to-line voltage, the dc-link current, and the output *u*-phase current with each modulation method at the modulation index of 0.705 and the load power factor of 0.819 (35° lagging), i.e., high-load power factor condition in driving mode. Under this load power factor condition, the application interval of the proposed DPWM is long; however, the conventional DPWM is also partially applied. Fig. 5.7 demonstrates that the width of the envelope in the dc-link current is reduced. On the other hand, the larger transitions between $+E_{dc}$ and $-E_{dc}$ seem to occur in the line-to-line voltage with the proposed DPWM.

Fig. 5.8 shows the PLECS simulation results with each modulation method at the modulation index of 0.705 and the load power factor of 0.819 (35° lagging), same conditions of the experiments in Fig. 5.7. The zoomed-in waveforms of the dc-link current demonstrate that the width of the step change is reduced by the proposed DPWM. Furthermore, the zoomed-in waveforms of the line-to-line voltage demonstrate that the instantaneous voltage transition between $+E_{dc}$ to $-E_{dc}$ does not occur when the proposed DPWM is applied. Therefore, the proposed DPWM does not increase *dv/dt* of the motor terminal voltage in practice, which causes the motor surge voltage, compared to the conventional DPWM.

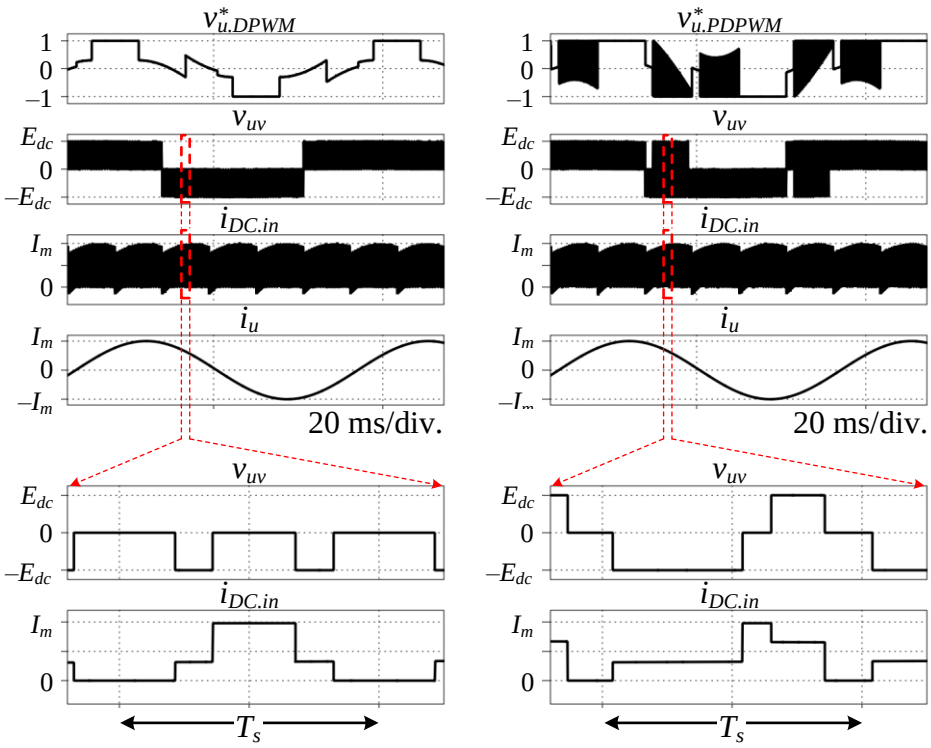


(a) Conventional DPWM.



(b) Proposed DPWM.

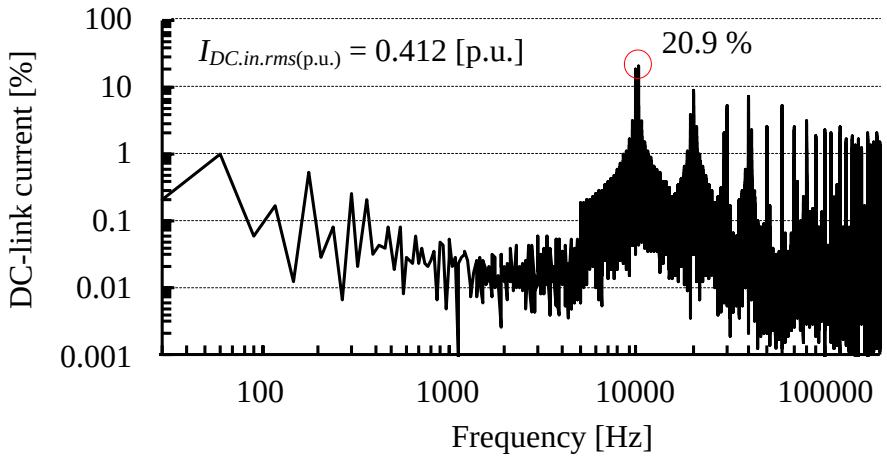
Fig. 5.7. Experimental waveforms at m = 0.705 and cos φ = 0.819 (35° lagging), i.e., driving mode with high-load power factor; u-phase modulating signal, output line-to-line voltage, dc-link current, and u-phase output current.



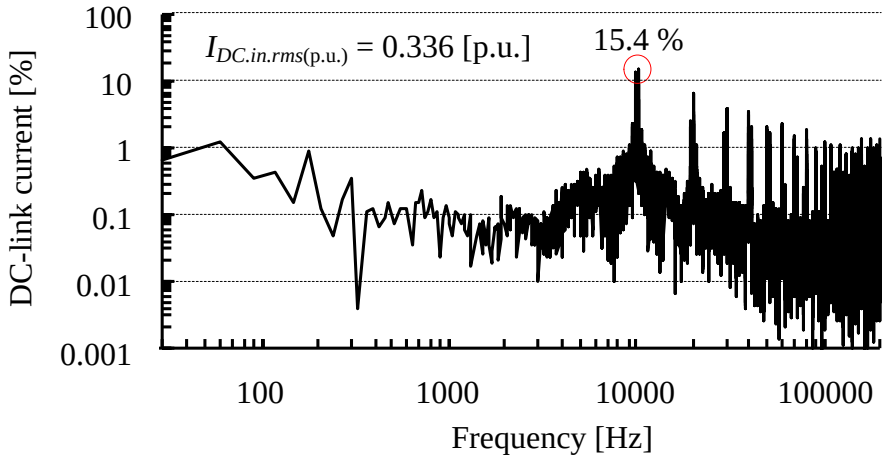
(a) Conventional DPWM. (b) Proposed DPWM.

Fig. 5.8. PLECS simulation results with each modulation method at m = 0.705 and cos φ = 0.819 (35° lagging) (under same conditions of experiments in Fig. 5.7).

Fig. 5.9 shows the harmonic components of the dc-link current under the same conditions as in Fig. 5.7. The proposed DPWM reduces the switching frequency component of the dc-link current by 5.49 points. Furthermore, the proposed DPWM reduces the dc-link current harmonics $I_{DC.in.rms(\text{p.u.})}$ by 18.4%.



(a) Conventional DPWM.

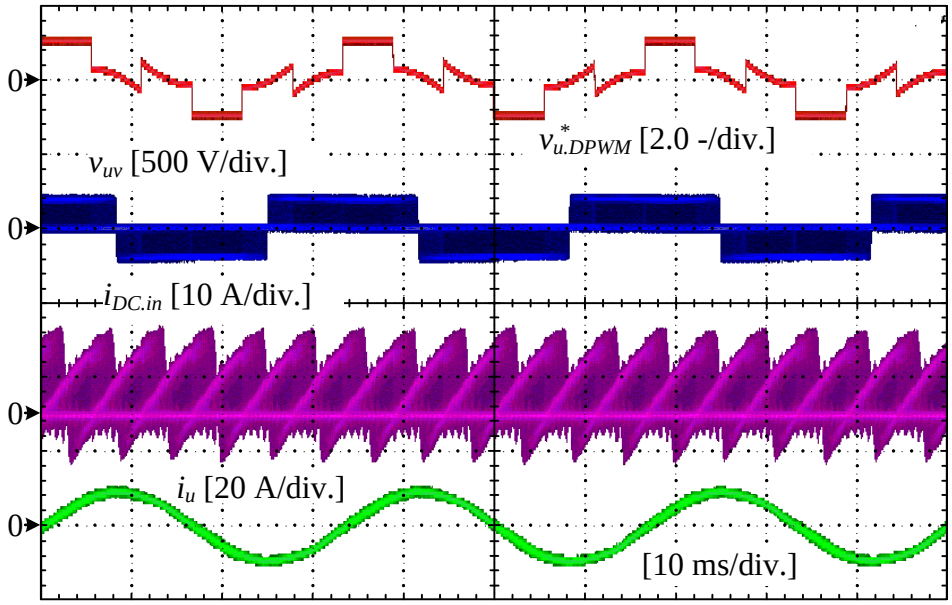


(b) Proposed DPWM.

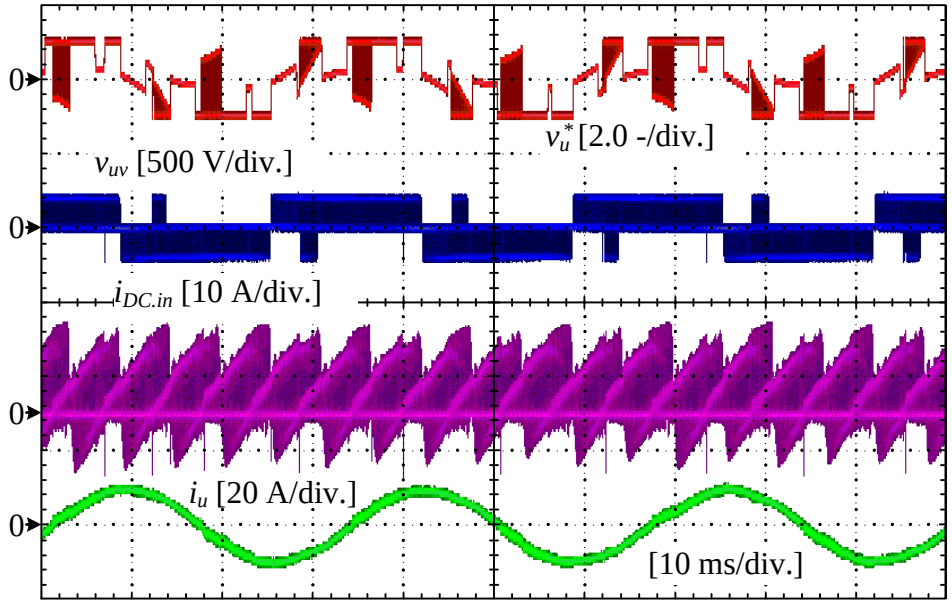
Fig. 5.9. Harmonic components of dc-link current at m = 0.705 and cos φ = 0.819 (35° lagging), i.e., driving mode with high-load power factor (under same conditions as in Fig. 5.7).

Figs. 5.10–5.11 show the VSI operating waveforms and the harmonic components of the dc-link current at the modulation index of 0.705 and the load power factor of 0.707 (45° lagging), i.e., low-load power factor condition in driving mode. These results demonstrate that the proposed CPWM is effective in reducing the dc-link current harmonics even when the load power factor is low.

Fig. 5.12 shows the analytic and experimental results of the dc-link current harmonic at the load power factor from 0.259 to 0.819, i.e., driving mode. The proposed DPWM reduces the dc-link current harmonics under any conditions of the modulation index and the load power factor. A higher load power factor enables a greater reduction effect on the dc-link current harmonics to be obtained. This trend is resulted from the relationship between φ and the application ratio of the shifted modulating signals in the whole phase range, observed in Fig. 5.4.

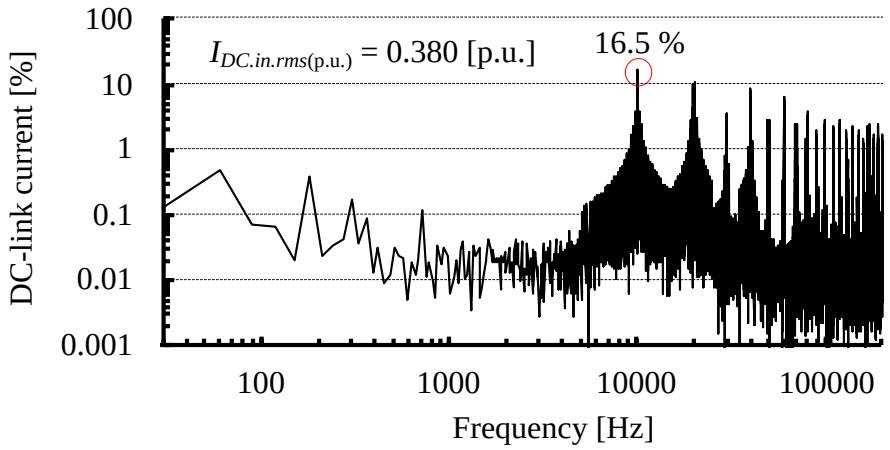


(a) Conventional DPWM.

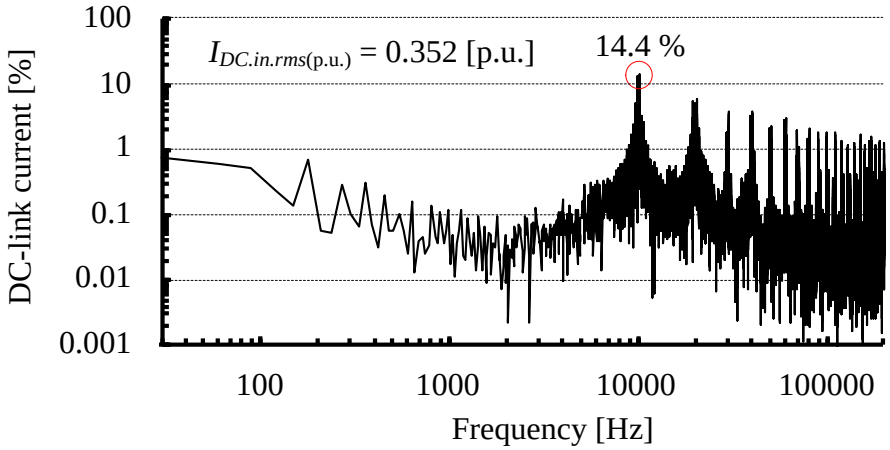


(b) Proposed DPWM.

Fig. 5.10. Experimental waveforms at m = 0.705 and cos φ = 0.707 (45° lagging), i.e., driving mode with low-load power factor; u-phase modulating signal, output line-to-line voltage, dc-link current, and u-phase output current.

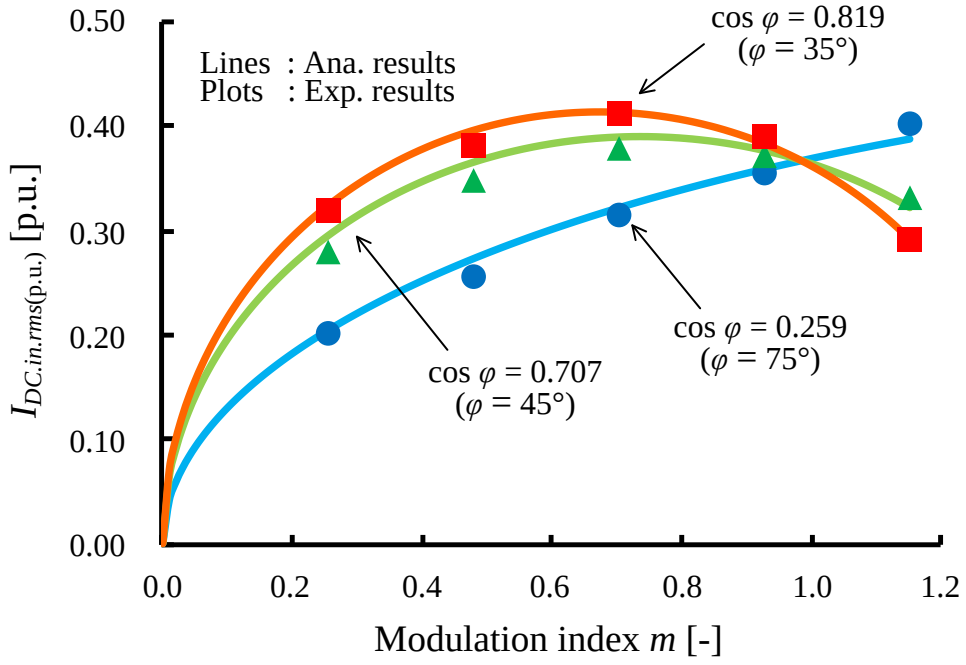


(a) Conventional DPWM.

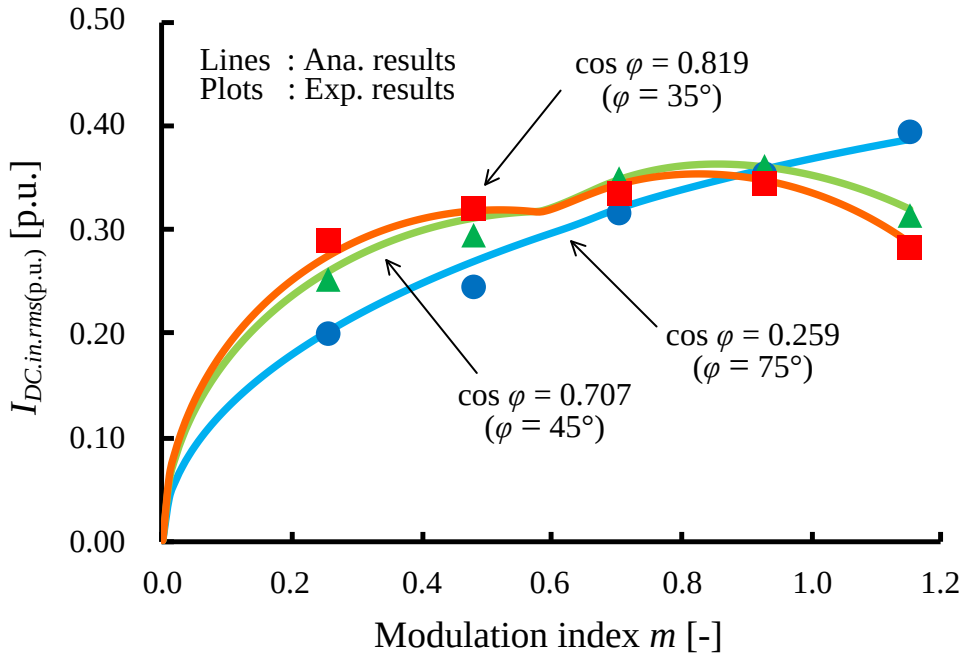


(b) Proposed DPWM.

Fig. 5.11. Harmonic components of dc-link current at m = 0.705 and cos φ = 0.707 (45° lagging), i.e., driving mode with low-load power factor (under same conditions as in Fig. 5.10).



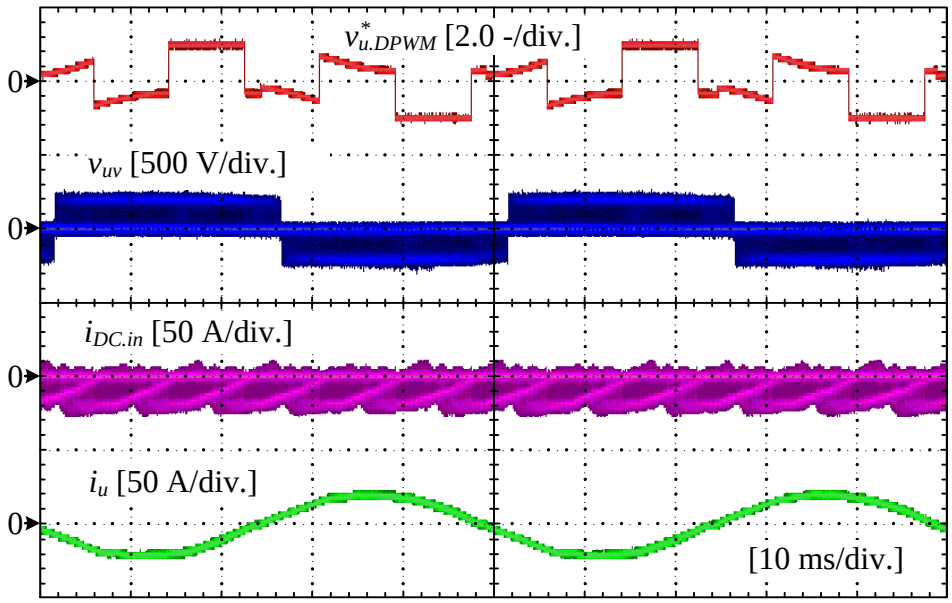
(a) Conventional DPWM.



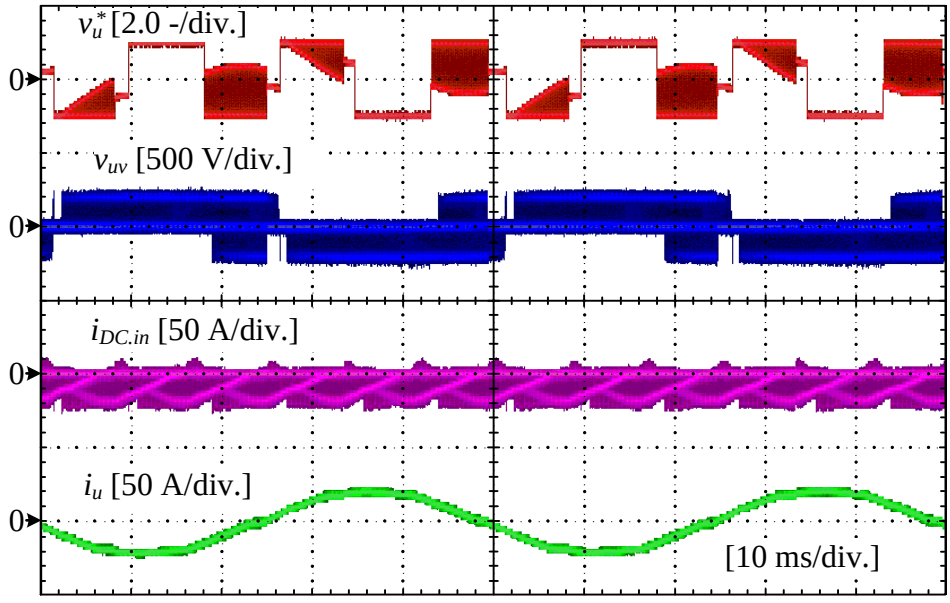
(b) Proposed DPWM.

Fig. 5.12. Measured dc-link current harmonics in driving mode.

Figs. 5.13–5.14 show the VSI operating waveforms and the harmonic components of the dc-link current at the modulation index of 0.445 and the load power factor of –0.766 (140° lagging), i.e., regenerative braking mode. The application of the proposed DPWM reduces the dc-link current harmonics even in the regenerative braking mode. These results verify that the proposed DPWM is effective in reducing the dc-link current harmonics for the AC motor drive system, of which the variation of the load power factor is considerably wide.

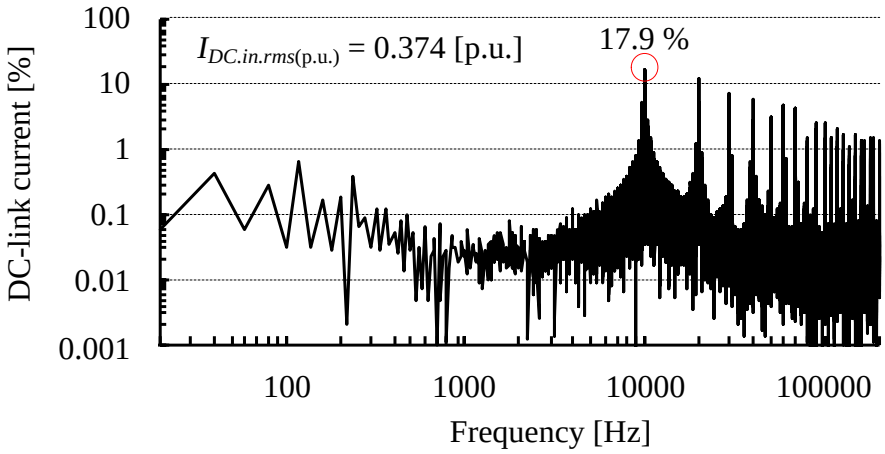


(a) Conventional DPWM.

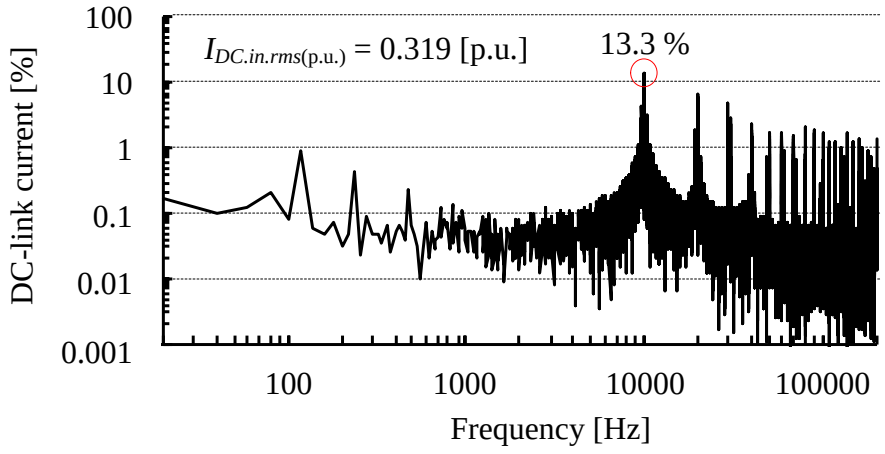


(b) Proposed DPWM.

Fig. 5.13. Experimental waveforms at m = 0.445 and cos φ = –0.766 (140° lagging), i.e., regenerative braking mode; u-phase modulating signal, output line-to-line voltage, dc-link current, and u-phase output current.



(a) Conventional DPWM.



(b) Proposed DPWM.

Fig. 5.14. Harmonic components of dc-link current at m = 0.445 and cos φ = –0.766 (140° lagging), i.e., regenerative braking mode (under same conditions as in Fig. 5.13).

5.4.2. Output Phase Current Harmonics

Fig. 5.15 shows the total harmonic distortion (THD) of the *u*-phase output current at the load power factor of 0.866. Even though the analytic criterion of λ_{rms}, explained in chapter 3.4.2, and output phase current THD are different, both of them are used to evaluate the output current quality, which characterizes the harmonic losses and the torque ripple in the test motor. Fig. 5.15 confirms the analytical results shown in Fig. 5.6 except for the high-modulation index area; in other words, the measured THD of the output phase current obtained with the proposed DPWM is higher than those obtained with the conventional DPWM. A reason for the increase of the current THD with the proposed DPWM is the current detection error around zero-current crossing points. These errors cause the incorrect selection of the load current sector (A–F) and increase the output phase current distortion, especially around the output phase current zero-crossing. This worse output phase current distortion might cause an increase of the iron loss in the load motor.

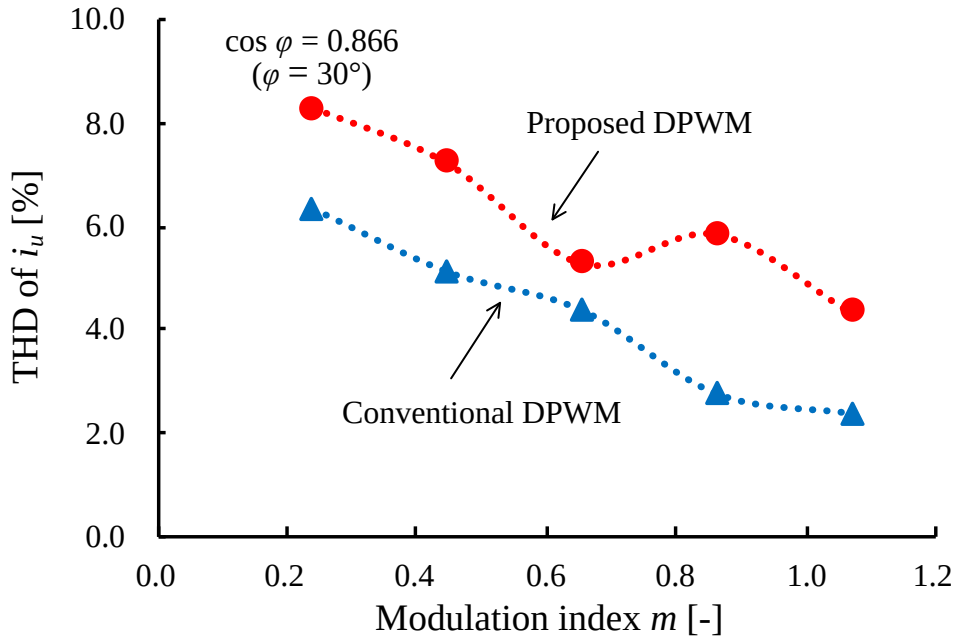


Fig. 5.15. Total harmonic distortion (THD) of *u*-phase output current at cos φ = 0.866 (30° lagging).

5.4.3. Inverter Efficiency

Fig. 5.16 shows the VSI efficiency between the conventional and proposed DPWM at the load power factor of 0.866. The inverter efficiency was measured using Yokogawa WT1800 power analyzer. The application of the proposed DPWM slightly improves the inverter efficiency. In terms of the number of switching transitions, those number are same between the conventional and proposed DPWM, which is observed from Fig. 5.1. In addition, the proposed DPWM always clamps the phase of which flowed current's absolute value is the maximum among three-phase currents due to the adaption process to the load power factor range, which is observed from Fig. 5.2. In other words, the proposed DPWM enables to avoid the larger current chopping, leading to the small switching loss compared to those with the conventional DPWM under conditions where the load power factor is not unity.

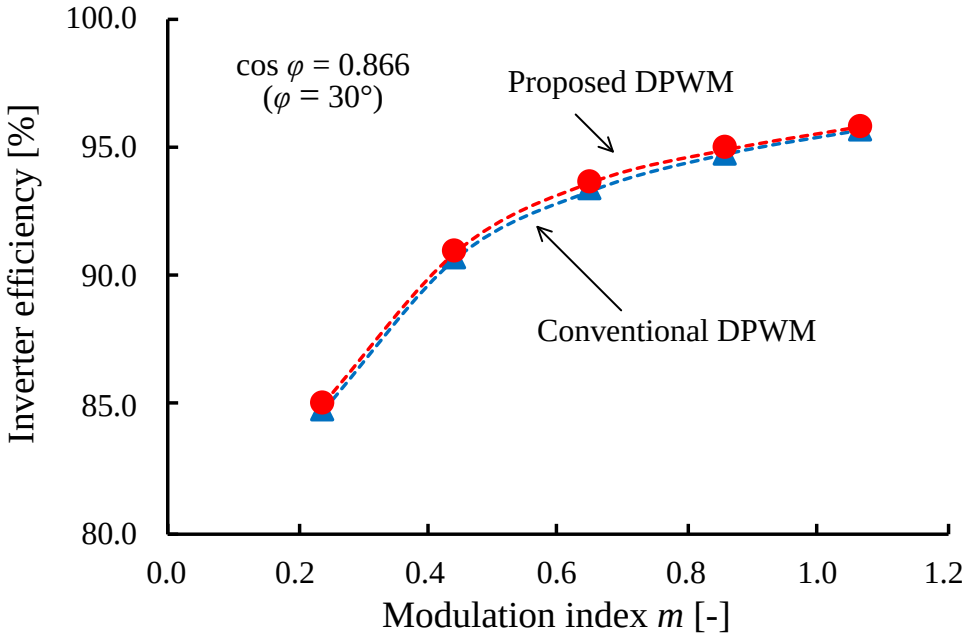
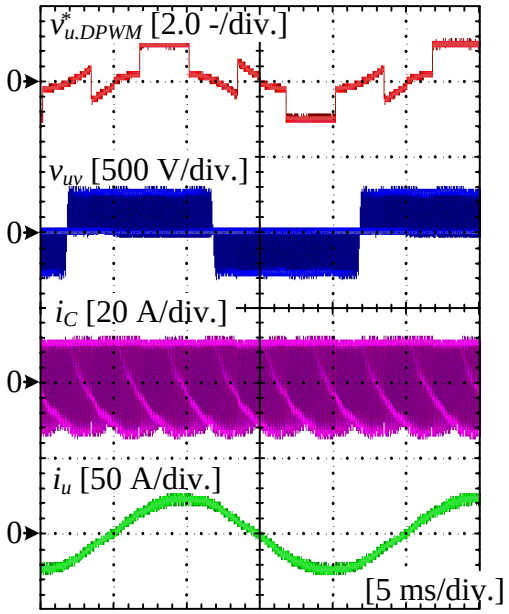


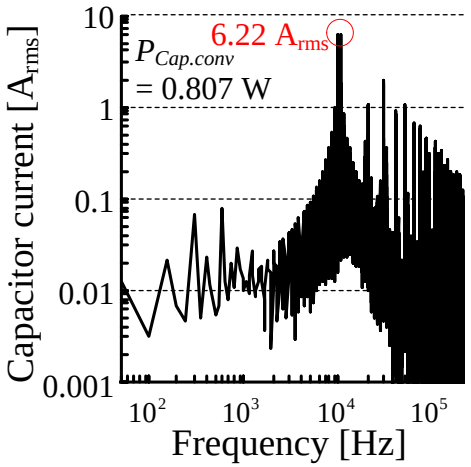
Fig. 5.16. Inverter efficiency comparison between conventional DPWM and proposed DPWM against different modulation index at cos φ = 0.866 (30° lagging).

5.4.4. DC-link Film Capacitor Heating

Figs. 5.17–5.18 show the VSI operating waveforms and the harmonic components of the dc-link capacitor current through the temperature rise test at the modulation index of 0.643, the load power factor of 0.891, and the inverter output power P_{inv} of 2.7 kW. The measured inverter efficiency was 96.30% with the conventional DPWM, whereas the efficiency was 96.22% with the proposed DPWM. The proposed DPWM reduces the capacitor loss by 51.1% compared to those obtained by the conventional DPWM.

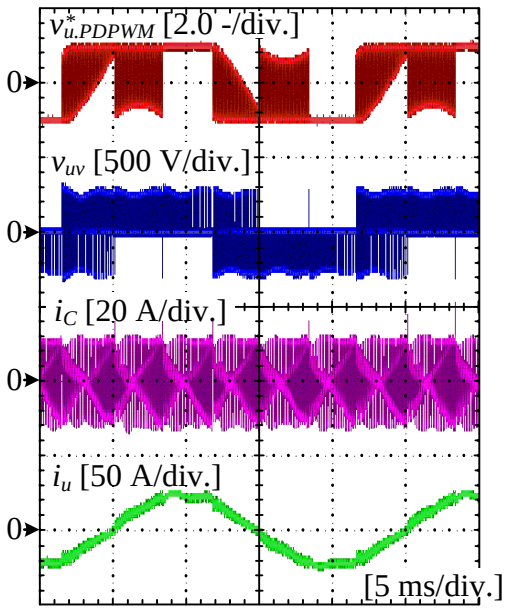


(a) Operating waveforms.

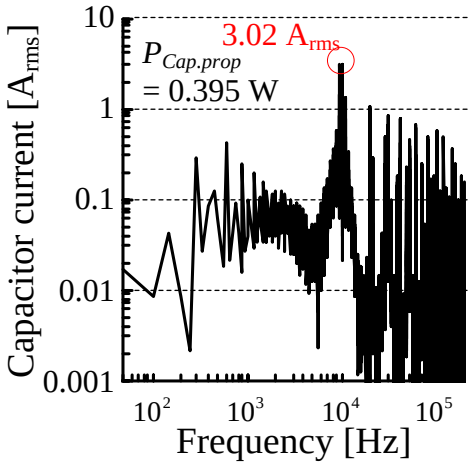


(b) Harmonic spectrum of i_C.

Fig. 5.17. VSI operating waveforms and harmonic components of dc-link capacitor current with conventional DPWM at m = 0.643, cos φ = 0.891 (27° lagging), and P_{inv} = 2.7 kW.



(a) Operating waveforms.



(b) Harmonic spectrum of i_C.

Fig. 5.18. VSI operating waveforms and harmonic components of dc-link capacitor current with proposed DPWM at m = 0.643, cos φ = 0.891 (27° lagging), and P_{inv} = 2.7 kW.

Fig. 5.19 shows the measured capacitor core temperature. These results confirm the capacitor temperature difference of 8.0℃ after 10800 seconds. Furthermore, the proposed DPWM lowers the equilibrium capacitor temperature, which is estimated from the test results using the least-square method, by 9.3℃ compared to the conventional DPWM. In other words, the proposed DPWM reduces the film capacitor heating by 17.5% compared to the conventional DPWM. However, the capacitor temperature difference with the conventional and proposed DPWM is smaller than those with the SVPWM approach, shown in Fig. 3.28. This is because the reduction effect on the dc-link capacitor current stress with the proposed DPWM is slightly inferior as compared with the proposed SVPWM due to the constrain of the proposed DPWM; Gate pulse generation based on the triangular-carrier comparison with the modulating signals, which are updated twice in each control period. On the other hand, in comparison with the capacitor temperature difference with the CPWM approach, shown in Fig. 4.22, the DPWM approach leads to greater reduction of the dc-link capacitor temperature rise. This is because the dc-link capacitor current stress is more reduced with the proposed DPWM due to the application of the degree of freedom of the zero-sequence signal injection.

Fig. 5.20 shows the harmonic spectrum of *u*-phase output current under the same experimental conditions as in Figs 5.17–5.18. The proposed DPWM worsens the phase current THD compared to the conventional DPWM also in these experimental conditions. However, those THD with the proposed DPWM are superior to those with the proposed SVPWM, shown in Fig. 3.29. This is because the proposed discontinuous modulating signals contain the smaller triplen harmonics than those of the proposed SVPWM, leading to the smaller harmonic flux. On the other hand, in comparison with the output current THD with the proposed CPWM, shown in Fig. 4.23, the proposed DPWM leads to slightly worse output current THD due to the injected zero-sequence signal.

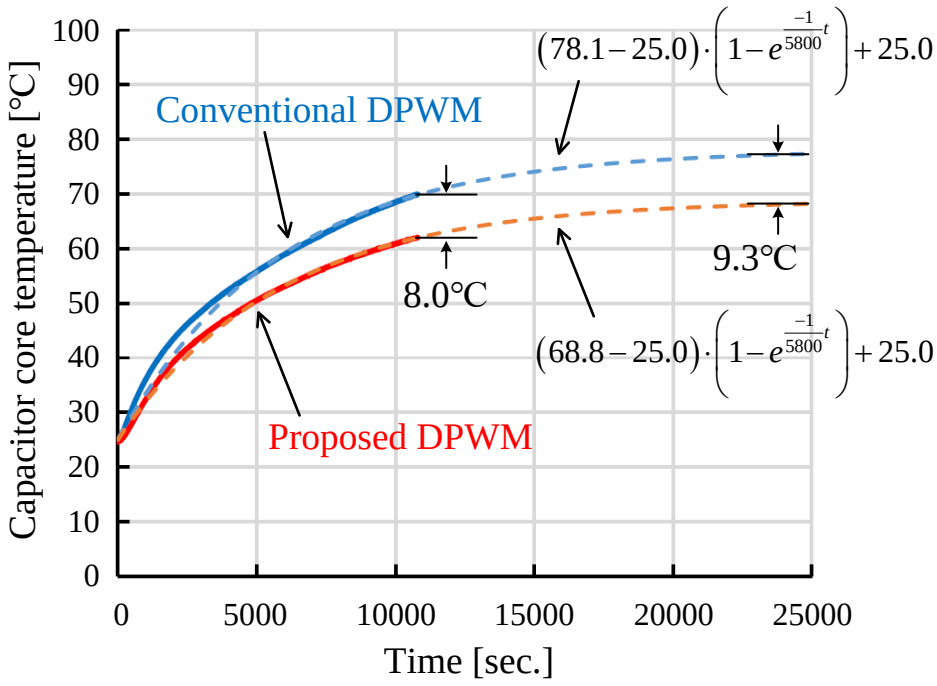


Fig. 5.19. Measured capacitor core temperature and its approximated curve with conventional and proposed DPWM.

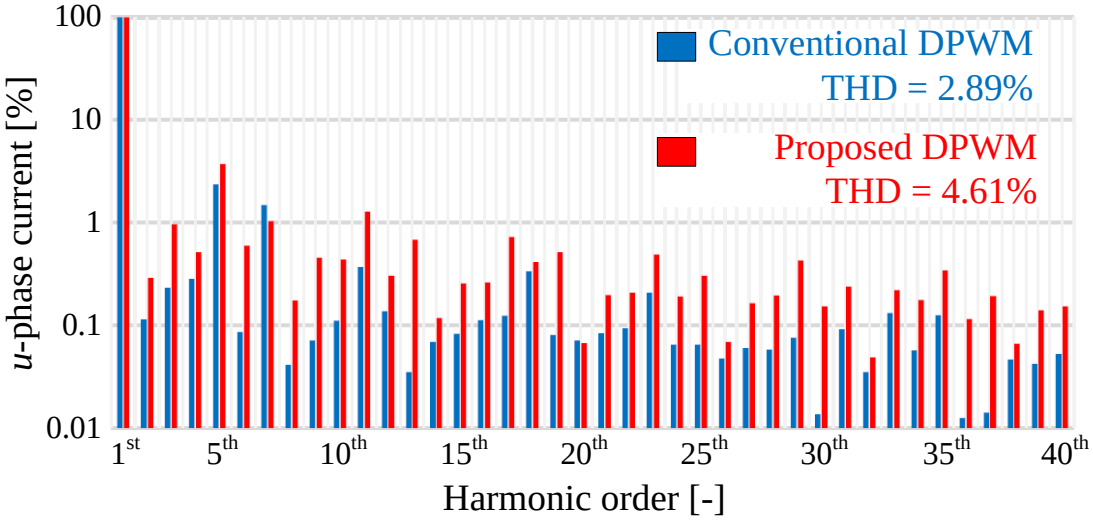
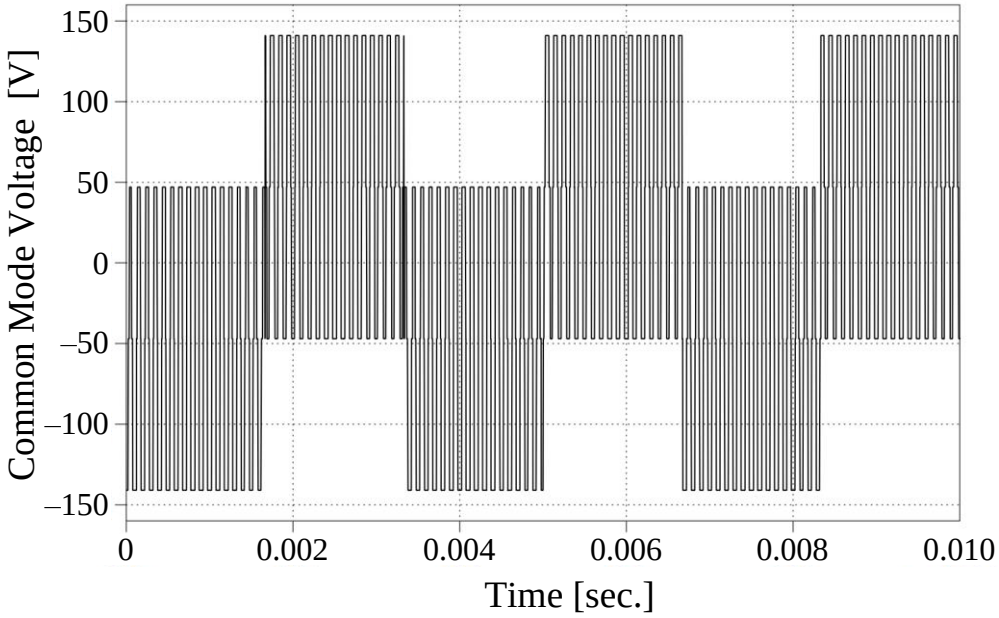
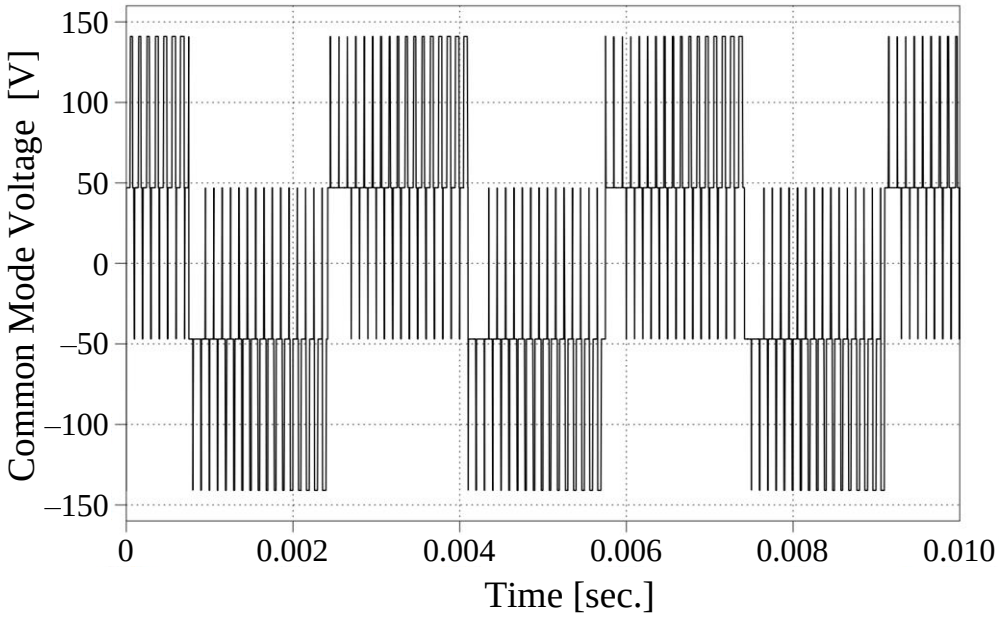


Fig. 5.20. i_u harmonic spectrum and its THD at m = 0.643, cos φ = 0.891 (27° lagging), and P_{inv} = 2.7 kW (under same conditions as in Figs. 5.17–5.18).

Figs. 5.21–5.22 show the PLECS simulation results of common-mode voltage waveforms and the harmonic components at the modulation index of 0.643, the load power factor of 0.891. Note that the fundamental frequency is set to 100 Hz for the simplification of the harmonic analysis, whereas the switching frequency is 10 kHz. Fig. 5.21 demonstrates that the step changes of the common-mode voltage are same between the conventional and proposed DPWM. Fig. 5.22 demonstrates that the switching frequency component of the common-mode voltage is reduced with the proposed DPWM. On the other hand, the higher switching frequency components up to 30 MHz are deteriorated with the proposed DPWM due to an absence of the gate pulse symmetry about the center of the control period. This might lead to the bulky common-mode filter compared to those with the conventional DPWM as well as the proposed CPWM in chapter 4.

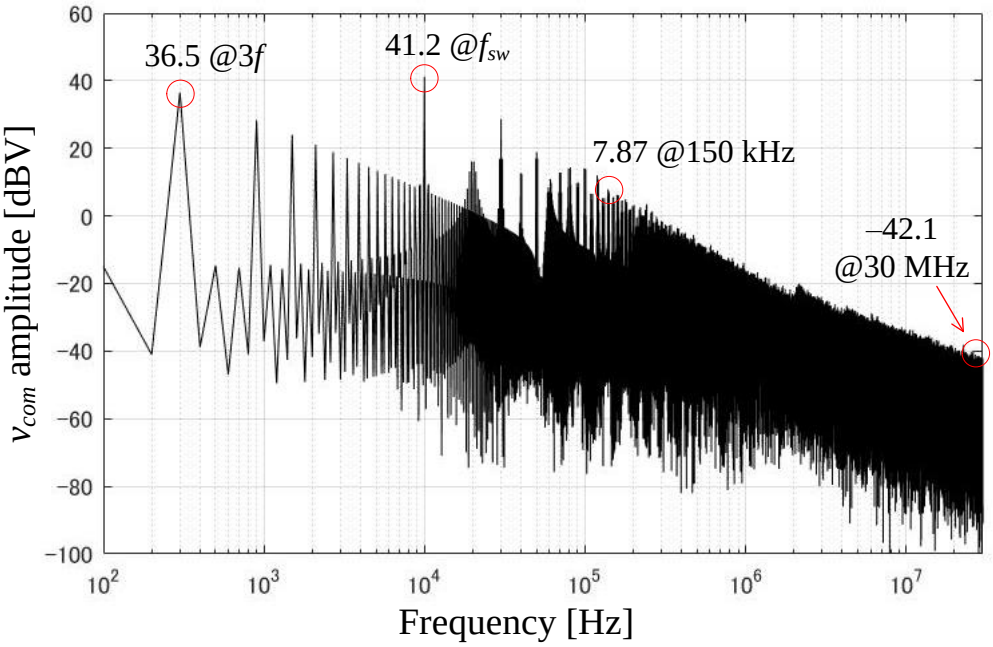


(a) Conventional DPWM.

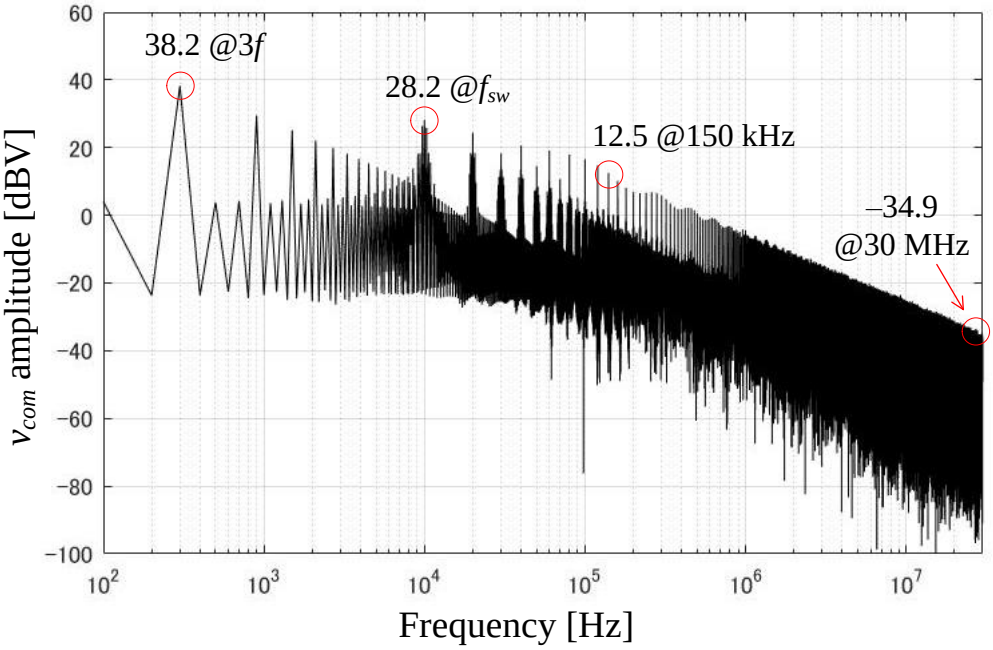


(b) Proposed DPWM.

Fig. 5.21. PLECS simulation results of common-mode voltage at m = 0.643, cos φ = 0.891 (27° lagging) (under same conditions as in Figs. 5.17–5.18 except for fundamental frequency of 100 Hz).



(a) Conventional DPWM.



(b) Proposed DPWM.

Fig. 5.22. v_{com} harmonic spectrum at m = 0.643, cos φ = 0.891 (27° lagging) (under same conditions as in Figs. 5.17–5.18 except for fundamental frequency of 100 Hz).

5.5. Electrolytic Capacitor Lifetime Estimation

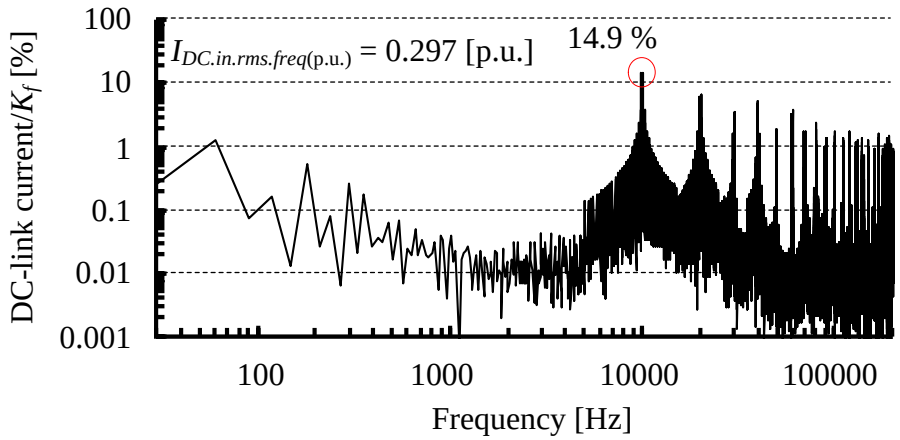
Fig. 5.23 shows the harmonic components of the dc-link current considering the frequency dependence of the ESR of aluminum electrolytic capacitor (NX series, Nichicon Corp. [5-4]) at the modulation index of 0.705 and the load power factor of 0.819 (under the same conditions as in Fig. 5.7). The expected lifetime (L_n) of the electrolytic capacitors is calculated as the same manner as introduced in the chapter 3.6. The proposed DPWM reduces the dc-link current harmonics $I_{DC.in.rms.freq}$(p.u.) by 18.2% when the frequency dependence of the ESR of aluminum electrolytic capacitor is considered. Assuming that the motor is mostly operated at the modulation index of 0.705 and the load power factor of 0.819, and the aluminum electrolytic capacitors in the conventional DPWM are designed at the worst case of the rated ripple current (i.e., F_I as 1), the lifetime expectancy of the electrolytic capacitor can be given by

$$L_{n\_conv.DPWM} = L_o \times 1 = 5000 \text{ h.} \quad \text{.....(5.3)}$$

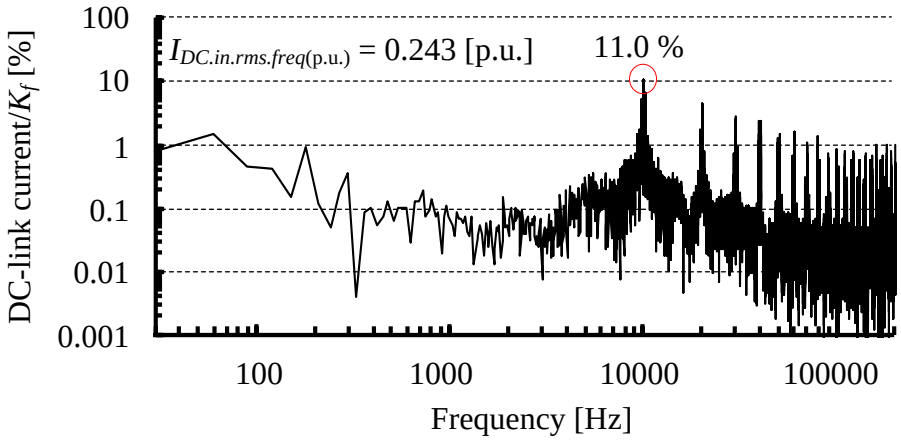
On the other hand, the application of the proposed DPWM raises F_I to 1.26 due to a current harmonic reduction of 18.2%. So, the lifetime expectancy of the electrolytic capacitor with the proposed DPWM can be given by

$$L_{n\_prop.DPWM} = L_o \times 1.26 = 6300 \text{ h.} \quad \text{.....(5.4)}$$

It is concluded that the application of the proposed DPWM might extend the lifetime of the electrolytic capacitor about 1.26 times longer at most than that of the conventional DPWM.



(a) Conventional DPWM.



(b) Proposed DPWM.

Fig. 5.23. Harmonic components of dc-link current considering frequency dependence of ESR of aluminum electrolytic capacitor at m = 0.705 and cos φ = 0.819 (35° lagging) (under same conditions as in Fig. 5.7).

5.6. Conclusion

The proposed DPWM in this chapter achieves the dc-link capacitor current stress reduction by the carrier-based PWM strategy, as well as the proposed CPWM in chapter 4, which is available with the general-purpose micro-computer. The dc-link capacitor current rms values were reduced by shifting the two unclamped discontinuous modulating signals in every half control period. In addition, the injection of the optimized zero-sequence signal to the classic discontinuous modulating signals based on the load current sector achieved the adaptation to the load power factor variation. In comparison with the conventional DPWM, the proposed DPWM reduced the dc-link current harmonics by 18.2%, might be leading to the 1.26 times lifetime extension of the electrolytic capacitors. Moreover, the proposed DPWM reduced the capacitor loss by 51.1%, lowering the equilibrium capacitor temperature by 9.3℃ (17.5%). Consequently, the proposed DPWM also contributes into the reductions of the dc-link capacitor current stress and the dc-link capacitor thermal stress as well as the proposed SVPWM in chapter 3 and the proposed CPWM chapter 4. The proposed DPWM has following advantages and disadvantage:

1. The dc-link capacitor current stress reduction is achievable with the slight deterioration of the output phase current distortion compared with the proposed SVPWM in chapter 3. However, the deterioration of the output phase current is larger than those with the proposed CPWM in chapter 4 (Advantage in comparison with the proposed SVPWM/Disadvantage in comparison with the proposed CPWM).
2. The proposed DPWM is achievable only with the low-cost digital hardware such as micro-computer, which is used in the electric vehicle applications where the high power density is highly desired (Advantage).
3. The maximum voltage transfer ratio of 1.0 is achievable (Advantage).

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Chapter 6

Application to Three-level Three-phase DC–AC Power Converters

6.1. Introduction

This chapter presents a new SVPWM strategy for three-level VSI using the optimization method of the PWM switching patterns for the current harmonics reduction of the dc-link capacitors. The original idea in the proposed SVPWM for two-level VSI, optimized selection of the voltage space vectors based on the load current sector, has been applied to the three-level VSI. The advantages of the proposed three-level SVPWM is the minimization for the dc-link capacitor current harmonics for the three-level neutral-point-clamped (NPC) VSI, which is necessary for the high-voltage AC motor drive system.

This chapter is organized as follows: First, in chapter 6.2, the three-level VSIs are reviewed and its dc-link current harmonics are analyzed with the classic PWM strategy. Next, in chapter 6.3, the optimized selection method for the voltage space vectors with the considerations of dc-link current harmonics and the load current quality is then presented. In chapter 6.4, the adaptation method to the variations of the load power factor, of which basic concept is same as the proposed two-level SVPWM with the load current sector, is presented. In chapter 6.5 and 6.6, analytic, simulation, and

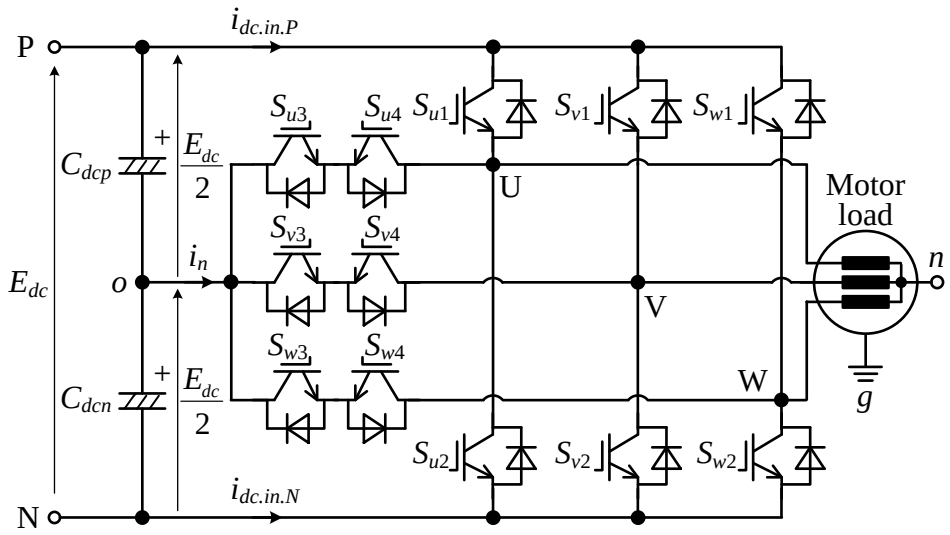
experimental results are presented to verify the effectiveness in terms of the reduction of the dc-link current harmonics, the impact on the output phase current quality, inverter efficiency, and the common mode voltage. After that, in chapter 6.7, the lifetime of the electrolytic capacitors is estimated and compared. Finally, in chapter 6.8, the conclusion of this chapter will be presented.

6.2. Three-level Inverter Input Current Harmonics

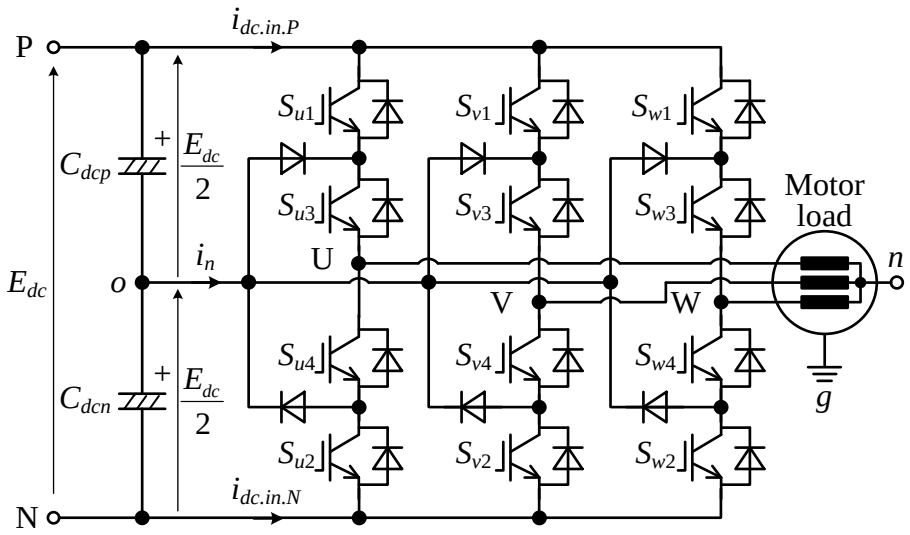
6.2.1 Configuration of Three-level Inverter

Fig. 6.1 shows the two common three-level VSI (3LVSI) configurations: T-type-3LVSI (T-3LVSI) and NPC-3LVSI [6-1]. These two topologies have both the advantages and disadvantages. The T-3LVSI has lower conduction losses due to the fact that there is only one device in the current path when the output voltage level is positive or negative. Nevertheless, the upper and lower devices in T-3LVSI have to block the whole dc-link voltage, resulting higher switching losses. In contrast, NPC-3LVSI has lower switching losses because two series-connected devices split the blocking voltage. However, it has higher conduction losses because there are two devices in the current path regardless of the output voltage level. Furthermore, NPC-3LVSI suffers from an increased number of semiconductors compared to those of the T-3LVSI. With the consideration of these aspects of the two topologies, it can be concluded that T-3LVSI is more beneficial in the low-voltage and medium-frequency applications, while NPC-3LVSI becomes more efficient in the medium-voltage and high-frequency applications [6-2].

For the above reason, NPC-3LVSI have been applied to medium-voltage high-power AC motor drive application [6-3]. For example AC-electrified railway systems are generally composed of traction transformers, single-phase NPC rectifier, three-phase NPC-3LVSI, and induction motors [6-4]. In the dc-link part of this system, two filter capacitors with the high-voltage capacity are implemented in series to decouple the unbalance between the instantaneous input and output power. Heretofore, oil-filled capacitors have been generally used as filter capacitors; however, these oil-filled capacitors require a periodic maintenance due to theirs low resistance for moisture and heat shock. Consequently, the oil-filled capacitors have been replaced by the film capacitors recently [6-5]. Nevertheless, the film capacitors may degrade or damage themselves with the self-heating due to the capacitor ripple current [6-6]. The inverter dc-link current contains numerous high-order



(a) T-type three-level VSI.



(b) NPC three-level VSI.

Fig. 6.1. Three-level voltage source inverter configurations.

switching-frequency harmonics because the current is a superposition summation of the switched current pulses from each phase leg of 3LVSI [6-7]–[6-8]. Therefore, it is necessary to reduce NPC-3LVSI input current harmonics. For AC-electrified railway applications, note that the dc-link capacitors are mainly designed to fulfill the capacitance requirement to

absorb the power ripple due to the single-phase AC grid; thus, the harmonic reduction does not achieve the capacitor size reduction. In addition, the VSI operates in the non-linear region such as over-modulation region. So, the capacitor ripple current reduction by modifying the PWM switching pattern is not to be directly applied to AC-electrified railway applications. However, the input current harmonic reduction might be effective in reducing the capacitor heating when VSI operates in linear modulation region.

Table 6.1 lists the relationships between the switching functions and the phase voltage of the NPC inverter. The switching function is defined as

$$s_{xj}(t)=\begin{cases}1, & (S_{xj}:ON)\\ 0, & (S_{xj}:OFF)\end{cases},\quad (x=u,v,w),(j=1-4) \qquad .....(6.1)$$

where j is the number of switching device defined in Fig. 6.1. There are three switching states in each leg of 3LVSI, and the three-level phase voltages are available.

TABLE 6.1.
SWITCHING STATES OF T-TYPE AND NPC THREE-LEVEL VSIS.

Switching state	v_{xo} [V]	Switching functions (x = u, v, w)			
		s_{x1}	s_{x2}	s_{x3}	s_{x4}
P (+)	$+E_{dc}/2$	1	0	1	0
0	0	0	0	1	1
N (–)	$-E_{dc}/2$	0	1	0	1

6.2.2 Classical PWM Strategy

Fig. 6.2 shows the available output voltage space vectors of 3LVSI in the $\alpha\beta$ reference frame. These voltage space vectors are illustrated on the basis of the *Clarke transform* of 3LVSI three-phase output voltages. The switching functions of each phase results in three different values; therefore, there are $3^3 = 27$ switching states in the 3LVSIs. On the other hand, there are nineteen voltage space vectors ($\mathbf{V_0}$–$\mathbf{V_{18}}$) in total due to the switching state redundancies.

Fig. 6.3 shows the principle of the conventional three-level SVPWM at the voltage sector I. Each sector of the conventional three-level SVPWM is regarded as the space vector diagram of the two-level SVPWM. Therefore, the classic two-level SVPWM is to be applied in each sector of the three-level SVPWM with an inner voltage reference vector $\mathbf{V^*_{in}}$. The inner vector is obtained by decomposing the voltage reference vector $\mathbf{V}^*$ by the equivalent zero vector of the two-level SVPWM in each sector (e.g., $\mathbf{V_7}$ in the voltage sector I) as

$$\mathbf{V}^*_{\mathbf{in}} = \mathbf{V}^* - \mathbf{V}_{\mathbf{6+i}} = \left|\mathbf{V}^* - \mathbf{V}_{\mathbf{6+i}}\right| \angle\gamma \quad \text{.....(6.2)}$$

where γ is the phase angle of the inner voltage reference vector $\mathbf{V^*_{in}}$ and i is the number of voltage sector of 3-level SVPWM where the voltage reference vector $\mathbf{V}^*$ exists. Note that the definitions of voltage sector of 3-level SVPWM are different from those of 2-level SVPWM shown in Fig. 2.3. The voltage sector I of 3-level SVPWM starts from the phase angle of –30°, whereas the voltage sector I of 2-level SVPWM starts from the phase angle of 0°. The voltage sector I area is also divided into six sub-sectors 1–6 in the same manner as the two-level SVPWM. Then, the three voltage space vectors surrounding the sub sector where the inner vector exists are selected. The inner voltage reference vector sampled in each control period T_s is generated by synthesizing the three voltage space vectors on the volt-second balance principle as [6-9]

$$\mathbf{V}_{\mathbf{in}}^{*} = \frac{t_a}{T_s}\mathbf{V_a} + \frac{t_b}{T_s}\mathbf{V_b} + \frac{t_c}{T_s}\mathbf{V_c} \quad \text{.....(6.3)}$$
$$T_s = t_a + t_b + t_c$$

where t_a–t_c are the duty cycles of each selected voltage space vector, and a–c represent the number of selected voltage space vectors, defined in Fig. 6.2.

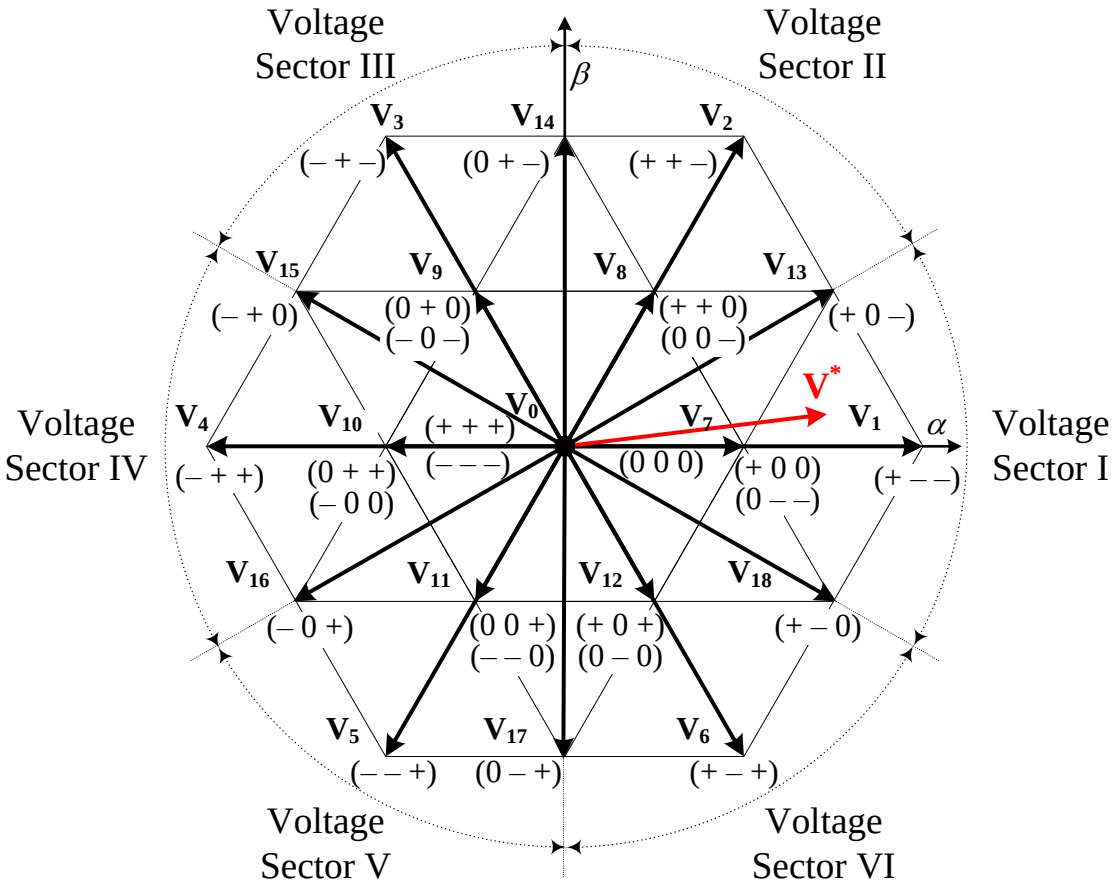
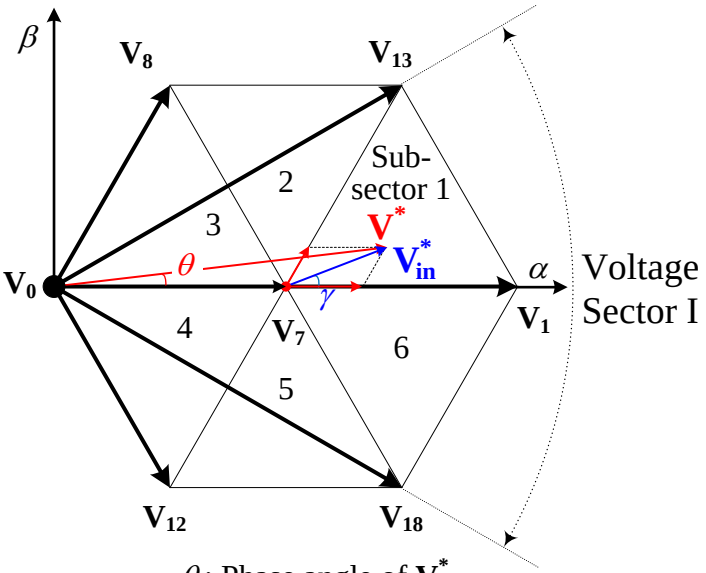


Fig. 6.2. Available output voltage space vectors of 3LVSI in $\alpha\beta$ reference frame.



θ: Phase angle of $\mathbf{V}^*$

γ: Phase angle of inner vector $\mathbf{V}_{in}^*$

Fig. 6.3. Principle of conventional three-level SVPWM at voltage sector I.

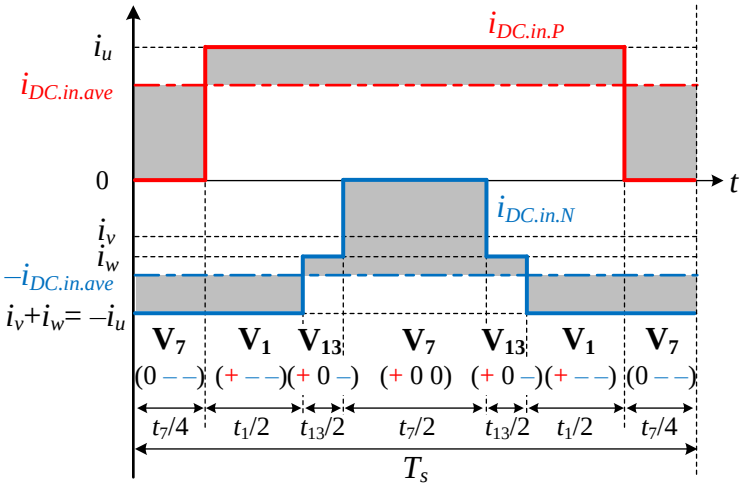


Fig. 6.4. Zoomed-in waveforms of the 3LVSI input current at m = 0.7, $2\pi ft$ = 5°, and cos φ = 1 when conventional SVPWM is applied.

Fig. 6.4 shows the zoomed-in waveforms of the 3LVSI input current at the modulation index of 0.7, the phase angle of 5°, and the unity load power factor when the conventional SVPWM is applied. The voltage reference vector $\mathbf{V}^*$ is sampled at sub-sector 1 in the voltage sector I as shown in Fig. 6.3. The instantaneous values of the P-side and N-side input current of the both T-type and NPC 3LVSIs are the superposition summation of the switched current pulses from each phase leg and calculated as

$$i_{DC.in.P} = \sum_{x=u,v,w} \left(s_{x1} \times i_x\right),$$
$$i_{DC.in.N} = \sum_{x=u,v,w} \left(s_{x2} \times i_x\right). \quad \text{.....(6.4)}$$

Although this chapter focus on NPC-3LVSI, note that the relationships between 3LVSIs input currents and those switching states are same for both T-type and NPC. Thus, the proposed modulation strategy, explained from following chapter, is also effective in reducing the capacitor current ripple in the T-type 3LVSI.

In order to analyze the optimized combination of the voltage space vectors for the minimum rms value of the 3LVSI input current, the rms value of the 3LVSI input current in the N cycle of the carrier period is used, as well

as the 2-level PWM strategies introduced in chapter 2.3,

$$i_{DC.in.rms}(T_s) = \sqrt{\frac{1}{2T_s}\int_{NT_s}^{(N+1)T_s}\left(i_{DC.in.P}^2 + i_{DC.in.N}^2\right)dt} = \sqrt{\sum_{k=a,b,c}\frac{t_k}{2T_s}\left(i_{DC.in.P.k}^2 + i_{DC.in.N.k}^2\right)}. \quad \text{.....(6.5)}$$

where t_k is the duty cycle of the selected voltage space vector, $i_{DC.in.P.k}$ and $i_{DC.in.N.k}$ are the instantaneous values of the P-side and N-side input current when the selected voltage space vector $\mathbf{V_k}$ is applied.

The average value of the 3LVSI input current over the fundamental period is calculated as

$$i_{DC.in.ave} = \frac{1}{2\pi}\int_0^{2\pi}\left(\sum_{k=a,b,c}\frac{t_k}{T_s}i_{DC.in.P.k}\right)d\theta = \frac{3}{4}m\cdot I_m\cos\varphi. \quad \text{.....(6.6)}$$

Note that the average value of the input current over the fundamental period is not dependent on the choice of the voltage space vectors, but the modulation index, load current, and load power factor.

The instantaneous rms value of the dc-link capacitor current is derived by the difference between the instantaneous RMS value of the 3LVSI input current (6.5) and the average value over the fundamental period (6.6) as

$$i_{C.rms}(T_s) = \sqrt{i_{DC.in.rms}^2(T_s) - i_{DC.in.ave}^2}. \quad \text{.....(6.7)}$$

Since only the instantaneous rms value of the 3LVSI input current is dependent on the choice of the voltage space vectors, the instantaneous rms value of the dc-link capacitor current is also dependent these choices. Thus, the lifetime of the dc-link capacitors, which is affected by the instantaneous rms value of the dc-link capacitor current (6.7), can be extended by the selection of the voltage space vectors that minimize the instantaneous rms value of 3LVSI input current (6.5).

Note that a small difference between the instantaneous values of $i_{DC.in.P}$ and $i_{DC.in.N}$, and these average values of the 3LVSI input current $i_{DC.in.ave}$

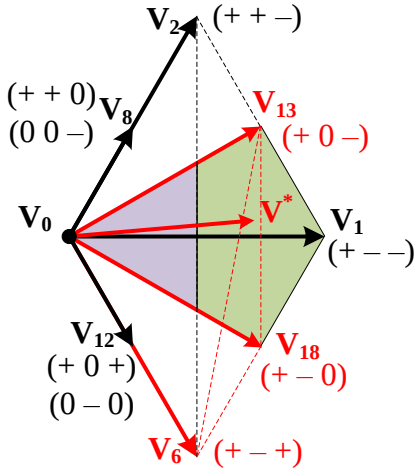
results in a small instantaneous RMS value of 3LVSI input current, as well as two-level PWM strategies [6-10]. These fluctuations of $i_{DC.in.P}$ and $i_{DC.in.N}$ are expressed as the shaded areas in Fig. 6.4. When the conventional three-level SVPWM is applied, the equivalent zero vectors $\mathbf{V_7}$, of which switching states are (+ 0 0) and (0 – –), are equally used during each control period in the sector I. In particular, when the equivalent zero vector $\mathbf{V_7}$ (0 – –) is applied, the instantaneous value of the P-side input current $i_{DC.in.P}$ becomes zero, which leads to the large P-side input current $i_{DC.in.P}$ fluctuations around its average value. Another equivalent zero vector $\mathbf{V_7}$ (+ 0 0) worsens the N-side input current $i_{DC.in.N}$ fluctuations around its average value in the same manner.

6.3. Optimal Selection for Voltage Space Vector

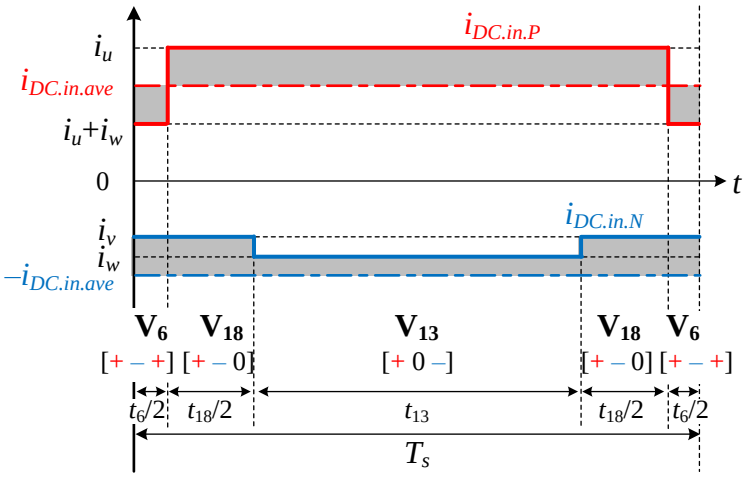
6.3.1 Combinations of Voltage Space Vectors for Minimum RMS value of 3LVSI Input Current

Fig. 6.5 shows an example of optimized combination of the voltage space vectors to minimize the rms value of the 3LVSI input current at high-modulation indices, and when the phase currents i_u is positive, and i_v and i_w are negative. The fluctuations of $i_{DC.in.P}$ and $i_{DC.in.N}$ around its average value expressed as the shaded area in Fig. 6.5(b) become small with the selection of the voltage space vectors $\mathbf{V_6}$–$\mathbf{V_{18}}$–$\mathbf{V_{13}}$ compared to that of the conventional three-level SVPWM shown in Fig. 6.4, resulting in the minimization of the rms value of the 3LVSI input current. Note that there are errors between the average value of 3LVSI input current over the fundamental period ($i_{DC.in.ave}$) and the average values over the control period. This is because the average value of the 3LVSI input current over the control period fluctuates at three-fold fundamental frequency due to the dc-bus neutral point potential variation. In order to optimize the combination of the voltage space vectors for the minimum rms value of the 3LVSI input current, first, the instantaneous values of the 3LVSI input current with all possible voltage space vectors are calculated off-line based on (6.4). Then, the three voltage space vectors, which make the instantaneous values become close to the average value of the 3LVSI, are selected. Note that the triangle formed by the tips of these selected three voltage space vectors must contain the tip of the voltage reference vector. As a result of these off-line calculations and selections, the voltage vectors for the minimum rms value of the 3LVSI input current at unity load power factor are $\mathbf{V_2}$, $\mathbf{V_{13}}$, $\mathbf{V_1}$, $\mathbf{V_{18}}$, and $\mathbf{V_6}$ in the high-modulation index region shown as the green area in Fig. 6.5(a). On the other hand, the voltage vectors in the low-modulation index region shown as the purple area in Fig. 6.5(a) at unity load power factor are $\mathbf{V_2}$, $\mathbf{V_8}$, $\mathbf{V_0}$, $\mathbf{V_{12}}$, and $\mathbf{V_6}$. In other words, there are some optimized combinations of the voltage

space vectors for the minimum rms value of the 3LVSI input current. In the proposed three-level SVPWM, the final combination of the applied voltage space vectors is selected from these optimized combinations for the minimum rms value of the 3LVSI input current, considering the 3LVSI output current quality.



(a) Combination of voltage space vectors ($\mathbf{V_6}$, $\mathbf{V_{18}}$, $\mathbf{V_{13}}$).



(b) Zoomed-in waveform of 3LVSI input current.

Fig. 6.5. One example of optimized combination of voltage space vectors ($\mathbf{V_6}$–$\mathbf{V_{18}}$–$\mathbf{V_{13}}$) for minimum rms value of 3LVSI input current at m = 0.7, $2\pi ft$ = 5°, and cos φ = 1, and when i_u is positive, i_v and i_w are negative.

6.3.2 Load Current Quality Consideration

In order to evaluate the 3LVSI output current quality, the concept of a harmonic [6-11] is used as an evaluation function of the load current quality characterized by the modulation method as well as chapter 3.4.2.

Fig. 6.6 shows the harmonic flux trajectories of all vector patterns to achieve the minimum rms value of the 3LVSI input current at the modulation index of 1.0, and the phase angle of 5 degrees. Within the carrier cycle the trajectories are drawn according to the selected switching sequence. In Fig. 6.6(a) as an example, two triangles are formed as the harmonic flux trajectory according to the selected switching sequence ($\mathbf{V_7}$–$\mathbf{V_1}$–$\mathbf{V_{13}}$–$\mathbf{V_7}$–$\mathbf{V_7}$–$\mathbf{V_{13}}$–$\mathbf{V_1}$–$\mathbf{V_7}$). Since the distance between the origin and the trajectory is equal to the magnitude of the harmonic flux, Fig. 6.6 demonstrates that the optimized vector combinations for the minimum rms value of 3LVSI input current worsen the load current quality compared to those with the conventional three-level SVPWM. The rms value of the harmonic flux over each control period is calculated as

$$\lambda_{rms}\left(T_s\right)=\sqrt{\int_{NT_s}^{(N+1)T_s}\left\|\boldsymbol{\lambda}_{\mathbf{h}}\right\|^2\cdot dt}. \quad \text{.....(6.8)}$$

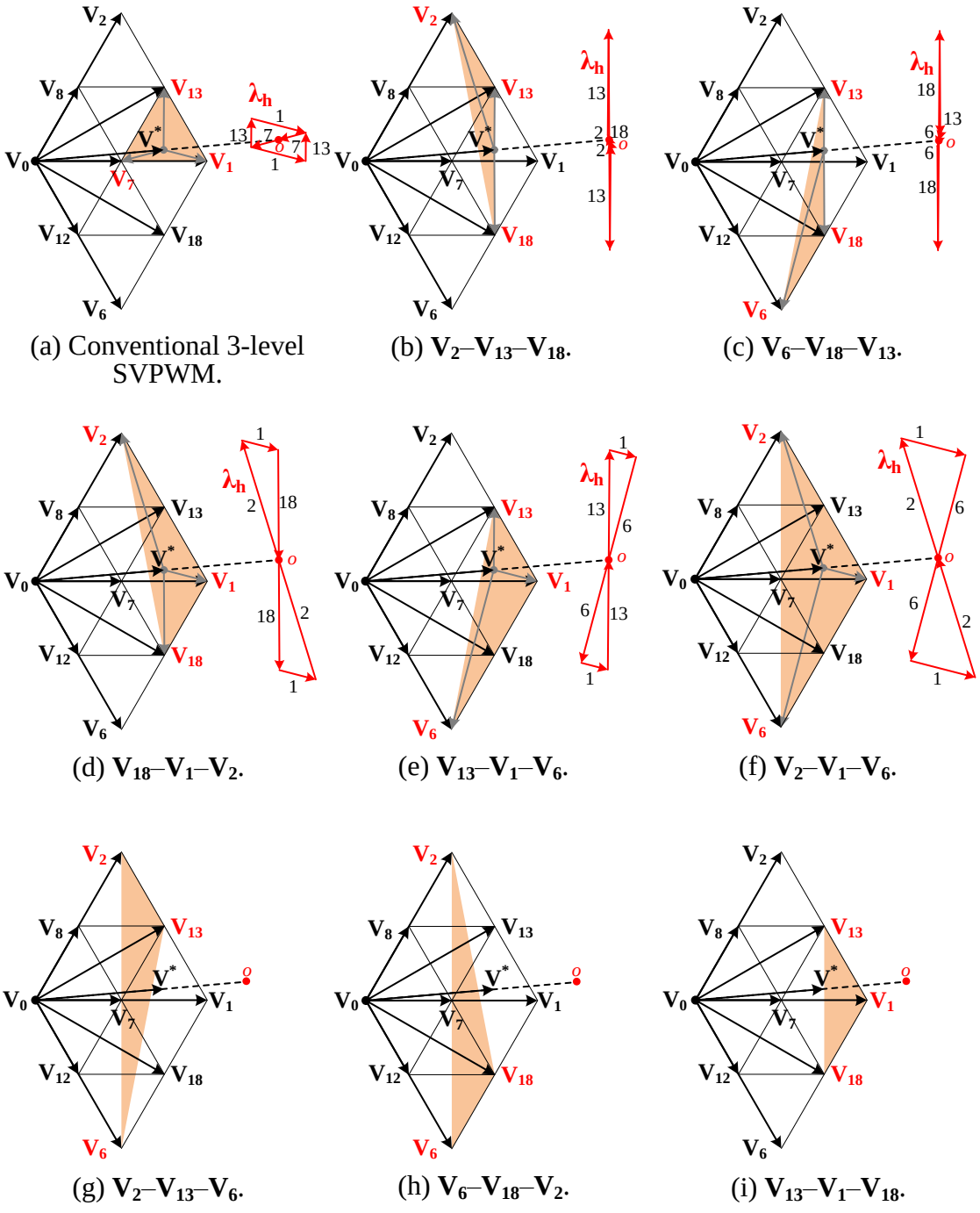


Fig. 6.6. Harmonic flux trajectories of all vector patterns to achieve minimum rms value of 3LVSI input current at m = 1.0 and $2\pi ft$ = 5°. Figs. (b)–(i) are with the optimized combinations of the voltage space vectors for the minimum rms value of the 3LVSI input current in the high-modulation indices region. With the vector combinations shown in (g)–(i), the voltage reference vector it not to be generated under these conditions.

Fig. 6.7 shows the phase angle dependencies of the rms values of the harmonic flux over each control period (6.8) at the modulation index of 1.0. Fig. 6.7 confirms that the optimized vector combinations for the minimum rms value of 3LVSI input current worsen the values of $\lambda_{rms}(T_s)$ with regard to any phase angle compared to the conventional 3-level SVPWM. However, it is demonstrated that the optimized combinations of voltage space vectors **V**$_2$–**V**$_{13}$–**V**$_{18}$, **V**$_6$–**V**$_{18}$–**V**$_{13}$, **V**$_2$–**V**$_{13}$–**V**$_6$, and **V**$_6$–**V**$_{18}$–**V**$_2$ suppress the increase of the harmonic flux at the modulation index of 1.0. For example, **V**$_2$–**V**$_{13}$–**V**$_6$ combination leads to the smallest increase of $\lambda_{rms}(T_s)$ in the phase range of 18°–30° as observed in Fig. 6.7. Note that $\lambda_{rms}(T_s)$ value has both the phase angle dependency and the modulation index dependency. Therefore, the proposed 3-level SVPWM vector patterns are determined by selecting the combination to achieve the smallest value of $\lambda_{rms}(T_s)$ from the optimized vector combinations for the minimum rms value of 3LVSI input current with respect to the phase angle and the modulation index. Note that the selection for the final combination of the applied voltage space vectors is also performed off-line and any on-line calculations of (3.3) or (6.8) are not necessary.

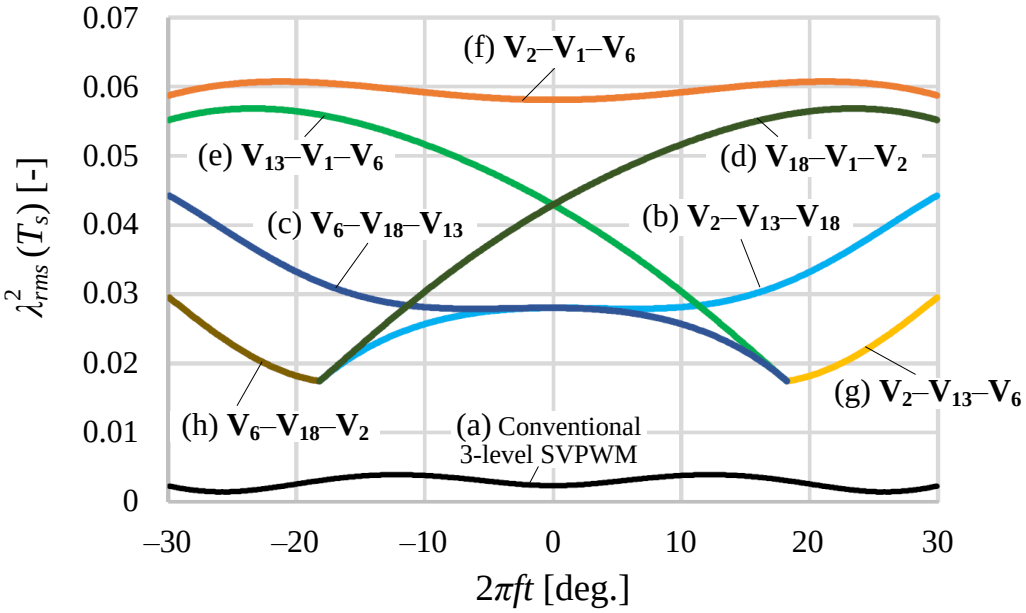
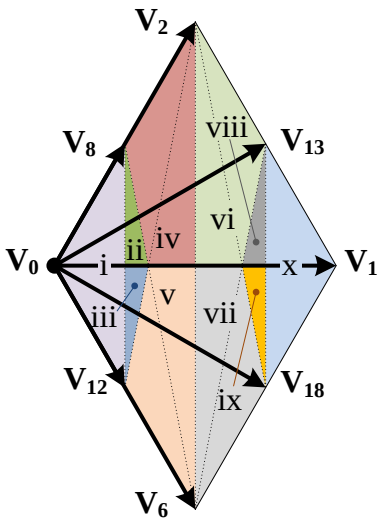


Fig. 6.7. Phase angle dependencies of rms values of harmonic flux over control period at m = 1.0.

Fig. 6.8 shows the proposed vector patterns to minimize the rms value of the 3LVSI input current when the phase currents i_u is positive, and i_v and i_w are negative with the consideration of the load current quality.



Area	Vectors
i	$\mathbf{V_8}$–$\mathbf{V_0}$–$\mathbf{V_{12}}$
ii	$\mathbf{V_6}$–$\mathbf{V_{12}}$–$\mathbf{V_8}$
iii	$\mathbf{V_2}$–$\mathbf{V_8}$–$\mathbf{V_{12}}$
iv	$\mathbf{V_2}$–$\mathbf{V_8}$–$\mathbf{V_6}$
v	$\mathbf{V_6}$–$\mathbf{V_{12}}$–$\mathbf{V_2}$
vi	$\mathbf{V_2}$–$\mathbf{V_{13}}$–$\mathbf{V_6}$
vii	$\mathbf{V_6}$–$\mathbf{V_{18}}$–$\mathbf{V_2}$
viii	$\mathbf{V_6}$–$\mathbf{V_{18}}$–$\mathbf{V_{13}}$
ix	$\mathbf{V_2}$–$\mathbf{V_{13}}$–$\mathbf{V_{18}}$
x	$\mathbf{V_{13}}$–$\mathbf{V_1}$–$\mathbf{V_{18}}$

Fig. 6.8. Proposed vector patterns to minimize rms value of 3LVSI input current when i_u is positive, and i_v and i_w are negative with consideration of load current quality.

Fig. 6.9 shows the flowchart to determine the detailed area i-x in Fig. 6.8 and applied voltage space vectors. First, the duty cycles corresponding to the applied voltage space vectors, listed in Fig. 6.8, are calculated. Next, those calculated duty cycles are ensured whether those are realistic values or not. If there is only one realistic case, it is identified as the area where the voltage reference vector $\mathbf{V}^*$ locates. If not, the phase angle (γ) of the inner voltage reference vector determines the correct area. For example, duty cycles are to be realistic values both in the parts of area ii and iii in Fig. 6.8. In this case, area ii and iii are identified whether γ exceeds 180° or not. Note that this area identification process is just one example. In practical use, the detailed area i-x is to be identified using lookup tables, avoiding the heavy on-line computation load.

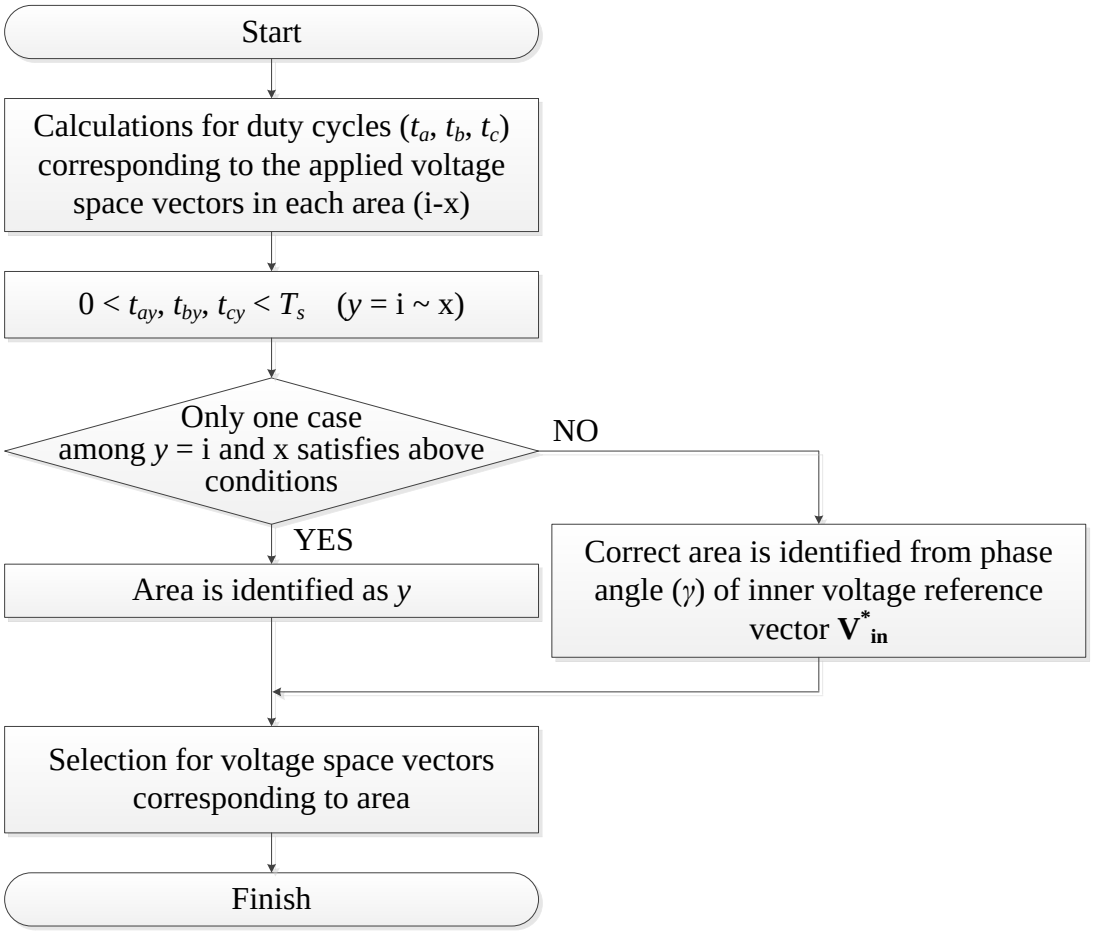


Fig. 6.9. Flowchart to determine detailed area i–x and applied voltage space vectors.

6.3.3 DC-bus Neutral Point Potential Discussion

The neutral current flowing out or into the neutral point of the dc-link causes the variation of the dc-bus neutral point potential. Its current is related to the common-mode voltage of 3LVSI and calculated from the switching functions and load currents as

$$i_n = \sum_{x=u,v,w} \left(s_{x3} \times s_{x4} \times i_x \right). \quad \text{.....(6.9)}$$

The variation of the dc-bus neutral point potential contains [6-12]:

1. the dc components due to the error of the common-mode voltage of 3LVSI or the capacitance mismatch connected in series, and
2. the fluctuations at triplen frequency of the fundamental waveform due to the common-mode fluctuations.

Both of them causes an excessive high voltage across the switching devices, load current distortion, and motor torque ripple; thus, the dc-bus neutral point potential control is necessary. Note that these problems occur both in the conventional and proposed SVPWM unless the switching state (0) with the phase voltage of zero is not used. Generally, the duty cycle of redundant vectors, of which have redundant switching states such as $\mathbf{V_7}$ (+ 0 0) and (0 – –), is rearranged in order to reduce the variation of the dc-bus neutral point potential [6-13]. However, in the high-modulation index region of the proposed SVPWM, no redundant vectors are selected; thus, the dc-bus neutral point potential control is not achievable. Note that the following two approaches have the potential to achieve the neutral potential control in the high-modulation index region of the proposed SVPWM:

1. applying only large active vectors (e.g., $\mathbf{V_1}$ (+ – –), $\mathbf{V_2}$ (+ + –), $\mathbf{V_3}$ (– + –), $\mathbf{V_4}$ (– + +), $\mathbf{V_5}$ (– – +), $\mathbf{V_6}$ (+ – +) for load current sector A), which do not depend on the dc-bus neutral point potential, with the sacrificed load current quality, or
2. partially (e.g., one-sixth phase angle period of all load current sectors) applying the conventional SVPWM, which uses the redundant vectors during every switching period, with the sacrificed reduction effect on the input current harmonics.

6.4. Adaptation to Wide Load Power Factor Range using Load Current Sector

The reduction of the rms value of the 3LVSI input current through the use of these optimized combinations of the voltage space vectors is dependent on the load power factor because the instantaneous values of the input current is dependent on not only the switching patterns but also the output phase current. Therefore, the adaption to the load power factor variation is important to reduce the 3LVSI input current harmonics over wide load power factor range, which is a typical requirement of the motor drive system.

In order to recognize the load current conditions, the load current sectors A–F, defined in table 3.2, are used as well as the dc-link capacitor current ripple reduction two-level PWM strategies.

Fig. 6.10 shows the layout of the load current sectors in the $\alpha\beta$ reference frame at the load power factor of 0.766 (40° lagging). The proposed vector patterns shown in Fig. 6.8 reduces the rms value of the 3LVSI input current only when i_u is positive and i_v and i_w are negative, i.e., the load current sector A. These load current sectors are rotated by the phase shift angle φ according to the variation of the load power factor. As a result, the load current sectors A–F will lead by the load power factor angle φ from the corresponding voltage sectors I-VI. As shown by the mesh area in Fig. 6.10, a part of load current sector A is not available with the optimized combinations of the voltage space vectors for the load current sector A because the mesh area is not covered by the proposed vector patterns. In these mesh areas, new combinations of the space vectors are ineffective in reducing the rms value of 3LVSI input current; hence, the conventional SVPWM is applied.

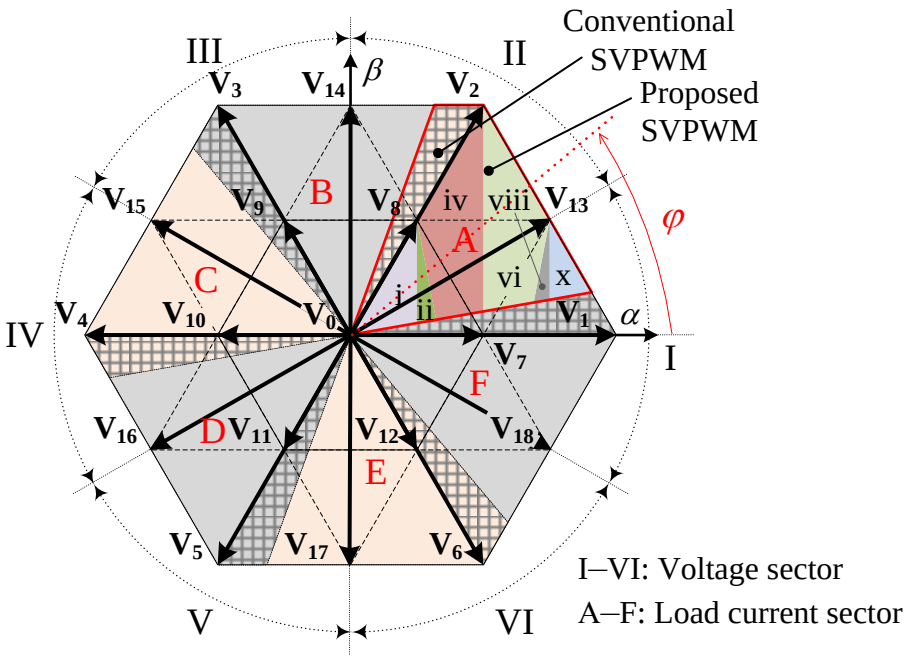


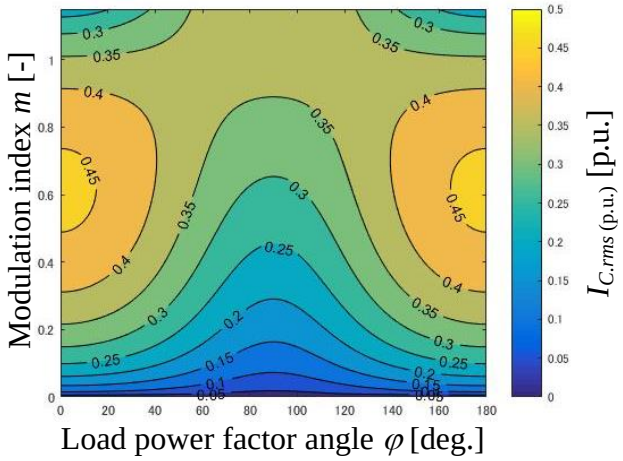
Fig. 6.10. Layout of load current sectors in $\alpha\beta$ reference frame at cos φ = 0.766 (40° lagging). The load current sector A leads by 40° from the voltage sector I.

6.5. Analytical Evaluations

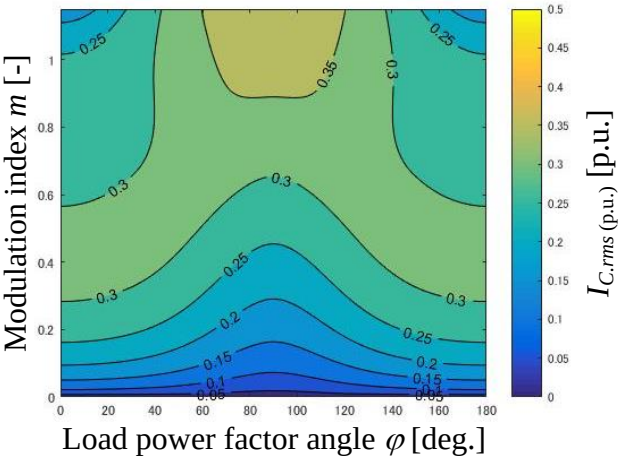
6.5.1 DC-link Capacitor RMS Current

In this chapter, the normalized dc-link capacitor rms current $I_{C.rms(\text{p.u.})}$ which is calculated as (2.13) is used for the evaluation of dc-link capacitor current harmonics reduction with the proposed three-level SVPWM.

Fig. 6.11 shows the analytical results of the dc-link capacitor current with regard to the modulation index m and the load power factor angle φ. Fig. 6.11(a) demonstrates that $I_{C.rms(\text{p.u.})}$ becomes the maximum at around $m = 0.6$ and absolute value of the load power factor $|\cos \varphi| = 1.0$ with the conventional SVPWM. On the other hand, Fig. 6.11(b) demonstrates that the proposed SVPWM reduces $I_{C.rms(\text{p.u.})}$ under almost all conditions of m and φ except for $\varphi = 90°$. In addition, a higher $|\cos \varphi|$ leads to a greater reduction effect on $I_{C.rms(\text{p.u.})}$. This trend is resulted from the relationship between φ and the application ratio of the optimized combination of the voltage space vectors. When $|\cos \varphi|$ is lower than 0.866, the conventional SVPWM is partially applied in whole phase range as observed in Fig. 6.10. The application ratio of the optimized vector patterns decreases as $|\cos \varphi|$ becomes small, and there is no $I_{C.rms(\text{p.u.})}$ difference between the conventional and proposed SVPWM when $\cos \varphi = 0$.



(a) Conventional three-level SVPWM.



(b) Proposed three-level SVPWM.

Fig. 6.11. Analytical results of dc-link capacitor rms current with regard to modulation index m and load power factor φ.

6.5.2 Load Current Quality

Since the voltage space vectors which are symmetric with regard to every 60° of phase angle are applied in the modern PWM strategy also for the three-level three-phase system, the characteristics of $\lambda_{rms}(T_s)$ (6.8) have the six-fold symmetry. Therefore, in this chapter, the rms value of the harmonic flux over fundamental period λ_{rms} which is calculated as (3.4) is used for the evaluation of the load current quality with the proposed three-level SVPWM as well as the dc-link capacitor current ripple reduction two-level PWM strategies.

Fig. 6.12 shows the rms values of the harmonic flux over fundamental period in the linear modulation range. The distance between the harmonic flux trajectories and the origin, which is the initial value of $\boldsymbol{\lambda}_{\mathbf{h}}$ at the beginning of the carrier cycle, corresponds to the magnitude of the harmonic flux. Thus, Fig. 6.12 confirms that the proposed SVPWM worsens the harmonic flux compared with those obtained with the conventional SVPWM. This is because the proposed vector patterns result in the application of the voltage space vector which is not the closest to $\mathbf{V}^*$, i.e., $\mathbf{V}_6$ and $\mathbf{V}_{13}$ in Fig. 6.5.

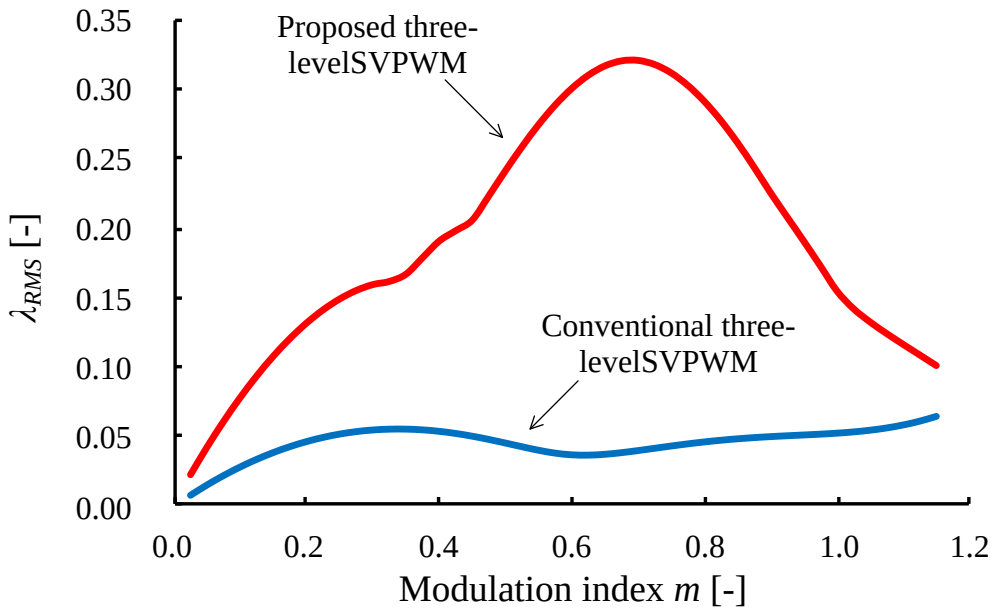


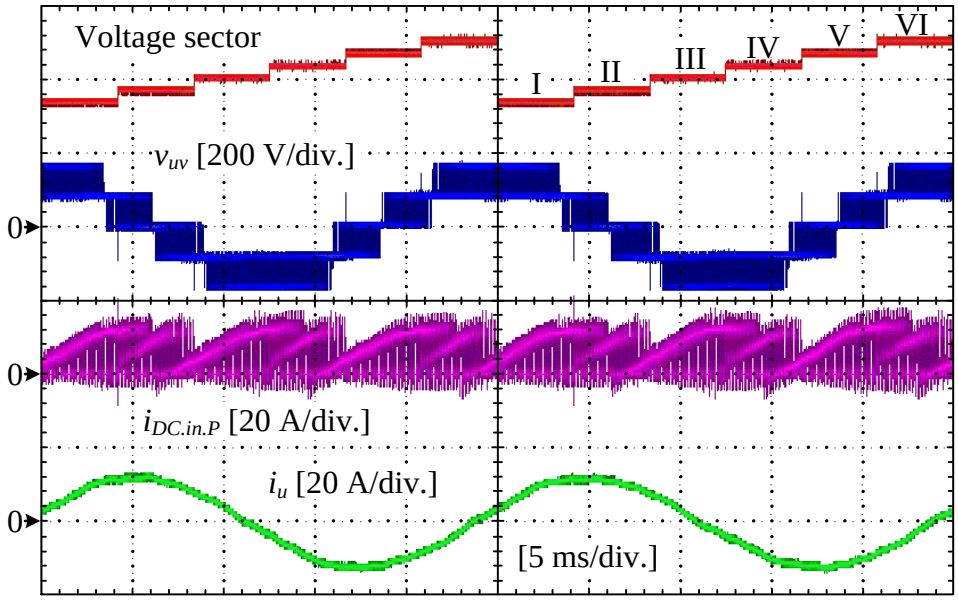
Fig. 6.12. Comparison of harmonic flux rms values with regard to modulation index. In the proposed three-level SVPWM calculations, the load power factor is set to 1.

6.6. Simulation and Experimental Results

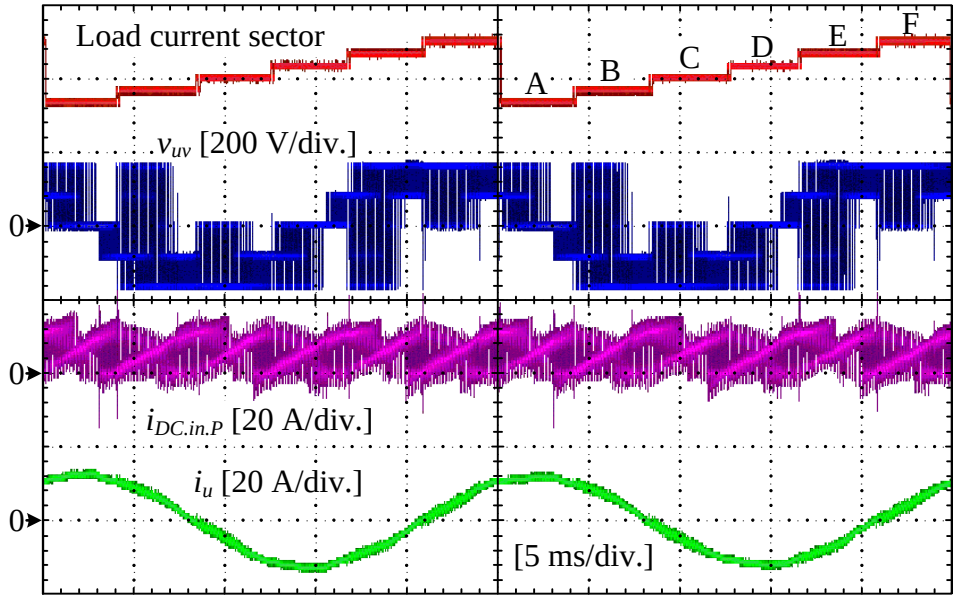
The performances of the conventional and proposed SVPWM are verified in PLECS simulation and experiment. In the experiment, 3LVSI, composed of IGBT power modules (2MBI150U2A-060, Fuji Electric Co., Ltd.), is operated at the switching frequency of 10 kHz with the dead time of 2 μs (2% of the control period). A three-phase induction motor (MVK8115A-R, Fuji Electric Co., Ltd.) with a rated power of 3.7 kW was used as the test motor and controlled by V/f control with the conventional and proposed SVPWM, which are implemented into an evaluation board (TMS320C6713, Texas Instruments). The load power factor was varied by controlling the torque reference of the load motor.

6.6.1. Input Current Harmonics

Fig. 6.13 shows the operating waveforms of 3LVSI with each modulation method at the modulation index of 0.930 and the load power factor of 0.866 (30° lagging). The width of the envelope in the input current is reduced by the proposed SVPWM. On the other hand, the transitions between $+E_{dc}$ and $-E_{dc}$ occur at worst in the line-to-line voltage with the proposed SVPWM due to the proposed selection of the voltage space vectors, whereas the voltage transition range with the conventional SVPWM is $E_{dc}/2$.



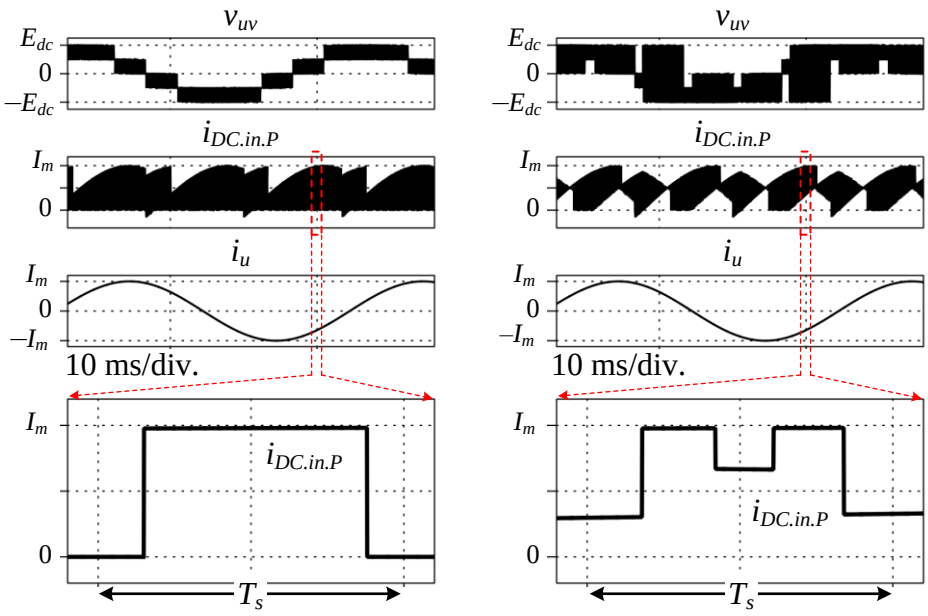
(a) Conventional SVPWM.



(b) Proposed SVPWM.

Fig. 6.13. Experimental waveforms at m = 0.930 and cos φ = 0.866 (30° lagging), i.e., high-load power factor; voltage or load current sector, output line-to-line voltage, input current, and u-phase output current.

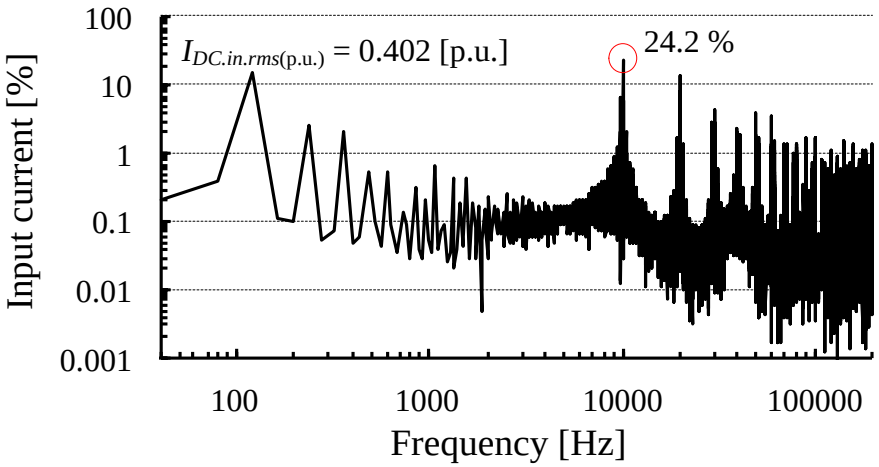
Fig. 6.14 shows the PLECS simulation results at the modulation index of 0.930 and the load power factor of 0.866 (30° lagging), same conditions of the experiments in Fig. 6.13. The zoomed-in waveforms of the input current demonstrate that the width of the step change in the input current is reduced by the proposed SVPWM.



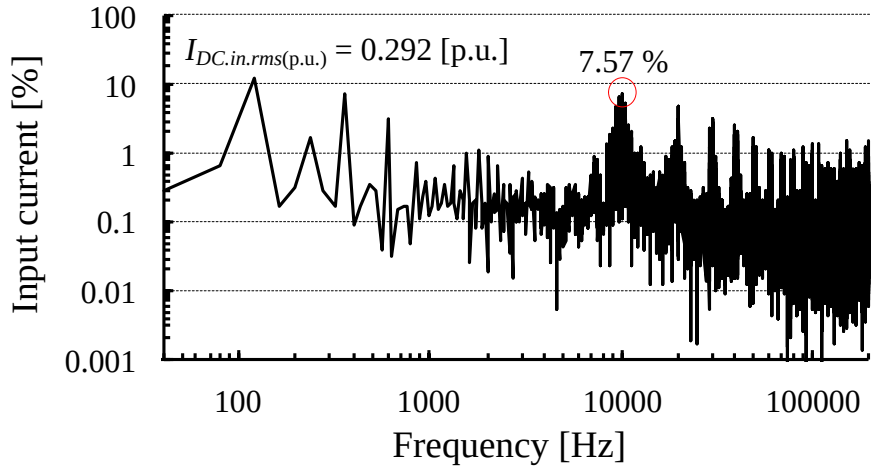
(a) Conventional SVPWM. (b) Proposed SVPWM.

Fig. 6.14. PLECS simulation results at m = 0.930 and cos φ = 0.866 (30° lagging) (under same conditions of experiments in Fig. 6.13).

Fig. 6.15 shows the harmonic components of the input current under the same conditions in Fig. 6.13. The proposed SVPWM reduces the switching frequency component by 16.6 points at most. Furthermore, the normalized input current harmonics, calculated as (3.5), is reduced by 27.4%.



(a) Conventional SVPWM.

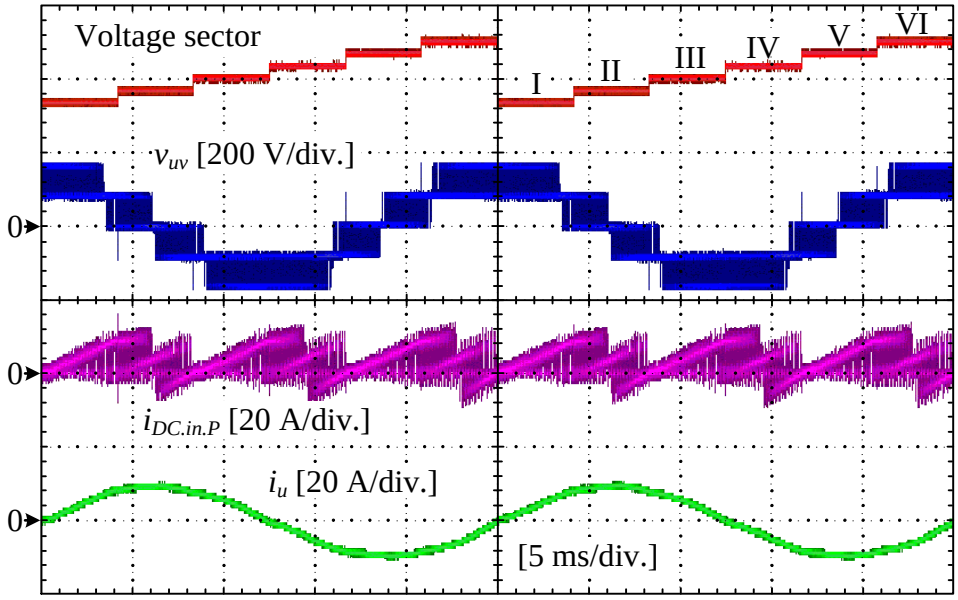


(b) Proposed SVPWM.

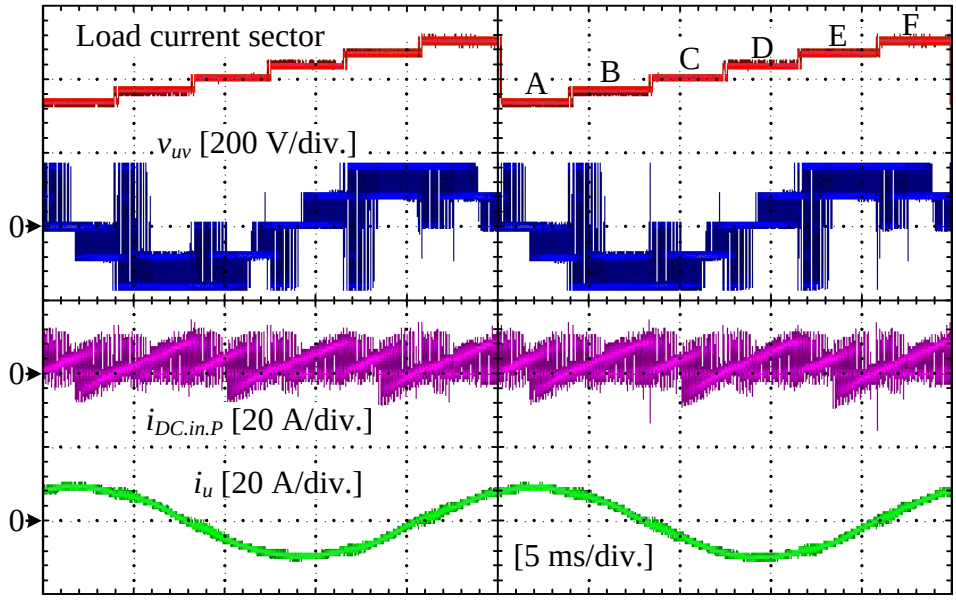
Fig. 6.15. Harmonic components of input current at m = 0.930 and cos φ = 0.866 (30° lagging), i.e., high-load power factor (under same conditions as in Fig. 6.13).

Figs. 6.16–6.17 show the 3LVSI operating waveforms and the harmonic components of the input current at the modulation index of 0.930 and the load power factor of 0.707 (45° lagging), i.e., low-load power factor condition. These results demonstrate that the proposed SVPWM is effective in reducing the input current harmonics even when the load power factor is low.

Fig. 6.18 shows the analytical and experimental results of the input current harmonics at the load power factor from 0.259 to 0.866. The proposed SVPWM reduces the input current harmonics under any conditions of the modulation index and the load power factor. Furthermore, these results confirm that the experimental results of the input current harmonics match the analytical values well. A higher load power factor enables a greater reduction effect on the input current harmonics to be obtained.

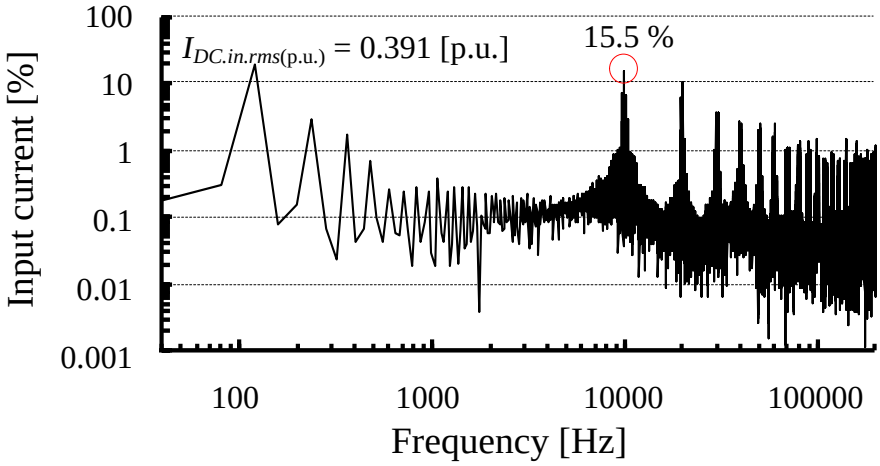


(a) Conventional SVPWM.

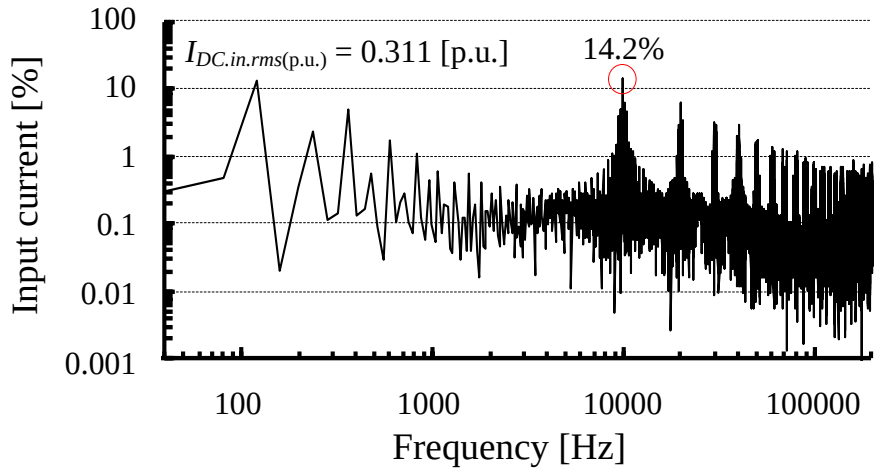


(b) Proposed SVPWM.

Fig. 6.16. Experimental waveforms at m = 0.930 and cos φ = 0.707 (45° lagging), i.e., low-load power factor; voltage or load current sector, output line-to-line voltage, input current, and u-phase output current.

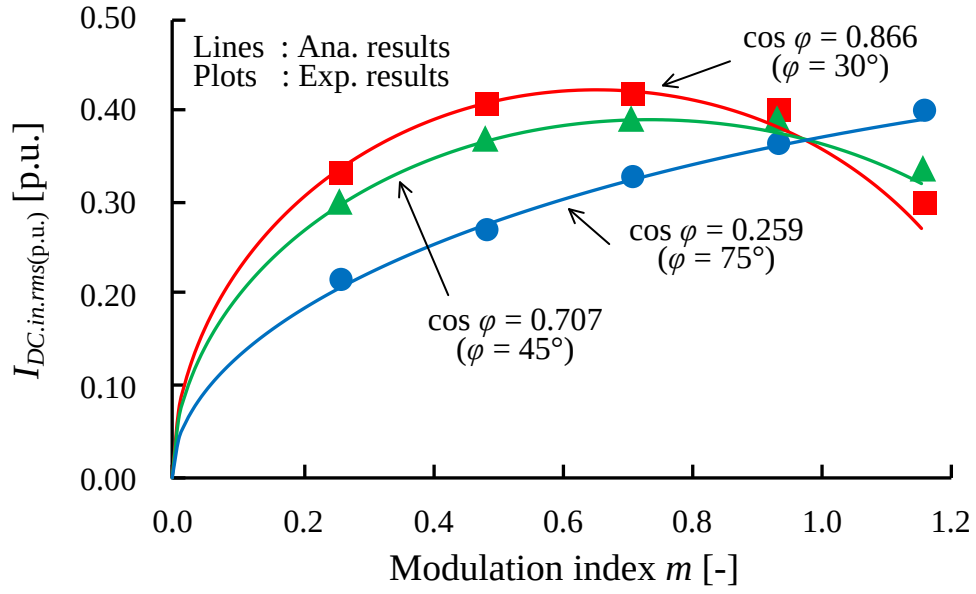


(a) Conventional SVPWM.

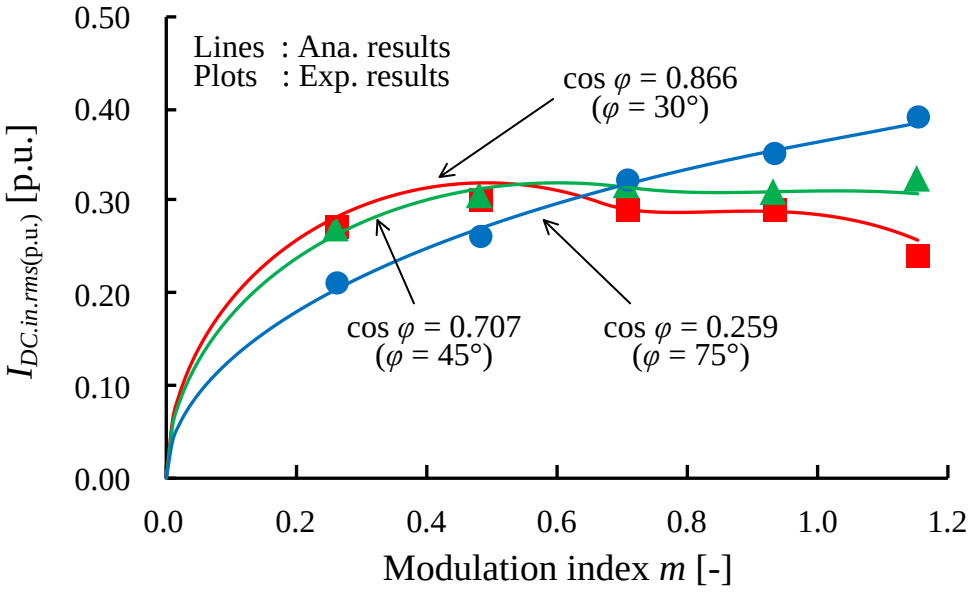


(b) Proposed SVPWM.

Fig. 6.17. Harmonic components of input current at m = 0.930 and cos φ = 0.707 (45° lagging), i.e., low-load power factor (under same conditions as in Fig. 6.16).



(a) Conventional SVPWM.



(b) Proposed SVPWM.

Fig. 6.18. Analytical and experimental results of input current harmonics.

6.6.2. Output Phase Current Harmonics

Fig. 6.19 shows the total harmonic distortion (THD) of the output *u*-phase current at the load power factor of 0.866 (30° lagging). The harmonic components up to 40th-order of the fundamental frequency are considered in this evaluation. The proposed SVPWM increases the distortion of the output phase current compared to those with the conventional SVPWM, which is also observed from harmonic flux analysis in Fig. 6.12.

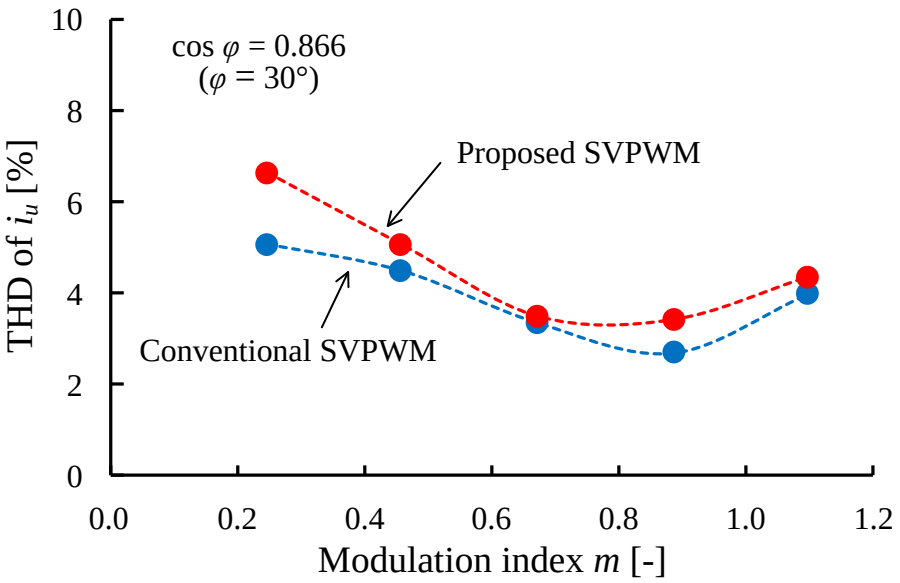


Fig. 6.19. Output *u*-phase current THD comparison between conventional and proposed SVPWM against different modulation index at cos φ = 0.866 (30° lagging).

6.6.3. Inverter Efficiency

Fig. 6.20 shows the 3LVSI efficiency, measured using Yokogawa WT 1800 power analyzer, at the load power factor of 0.866 (30° lagging). Fig. 6.20 demonstrates that the proposed SVPWM improves the efficiency. The proposed SVPWM may lead to the increased number of the voltage vector area changing timing. However, the occurrence frequency of the voltage vector area changing in the proposed SVPWM is much smaller than the switching frequency. Figs. 6.4 and 6.5 demonstrate that the proposed SVPWM leads to less number of switching transitions in each switching period compare to the conventional SVPWM. Therefore, the proposed SVPWM reduces the total number of switching transitions over the fundamental period compared to the conventional, leading to the small switching loss.

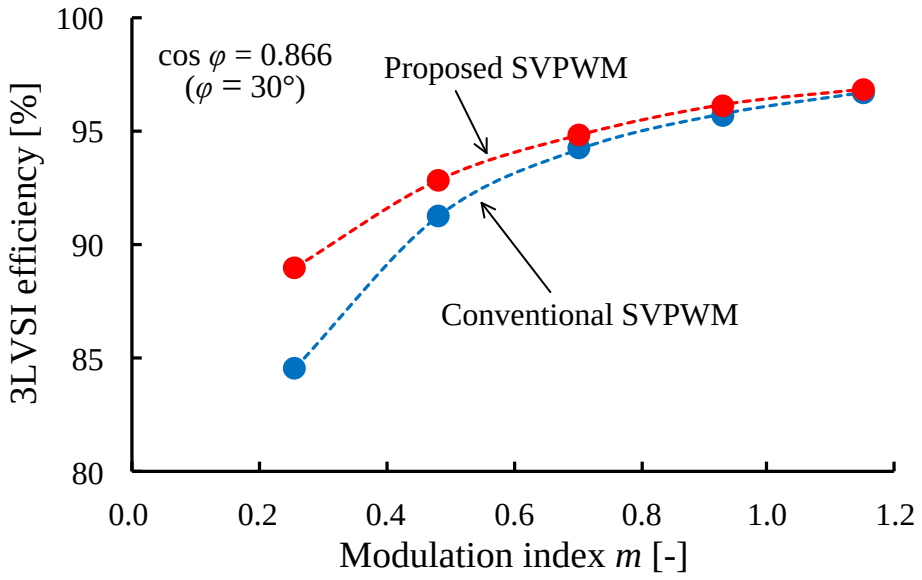


Fig. 6.20. 3LVSI efficiency comparison between conventional and proposed SVPWM against different modulation index at cos φ = 0.866 (30° lagging).

6.6.4. Common Mode Voltage

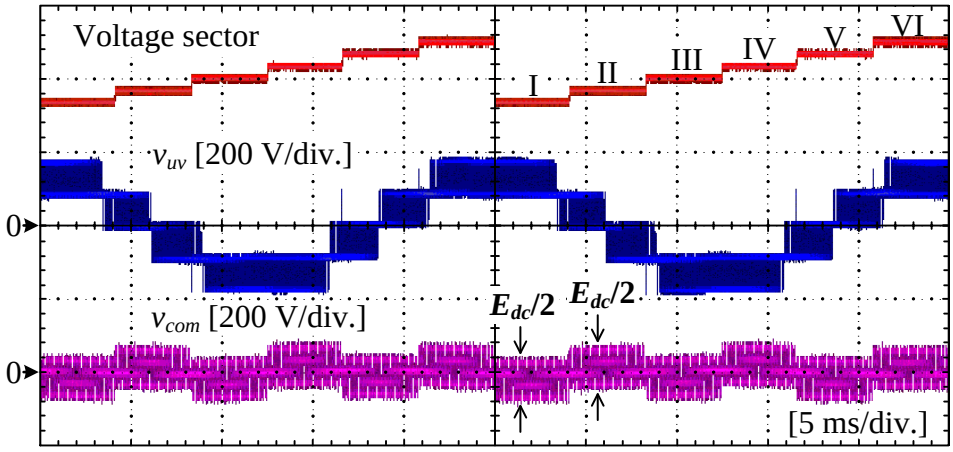
The common-mode voltage of the three-phase inverter (v_{ng} in Fig. 6.1) is defined as the potential of the star point of the motor load (*n* in Fig. 6.1) with respect to the motor-frame ground (*g* in Fig. 6.1). In practical, the potential of the center of the dc-bus (*o* in Fig. 6.1) with respect to the ground v_{og} is small and slowly varies compared to v_{no}. So, the common-mode voltage v_{com} is defined as the potential difference between *n* and *o* as [6-14]

$$v_{com} = v_{ng} = v_{no} + v_{og} \approx v_{no} = \frac{v_{uo} + v_{vo} + v_{wo}}{3}. \quad \text{.....(6.10)}$$

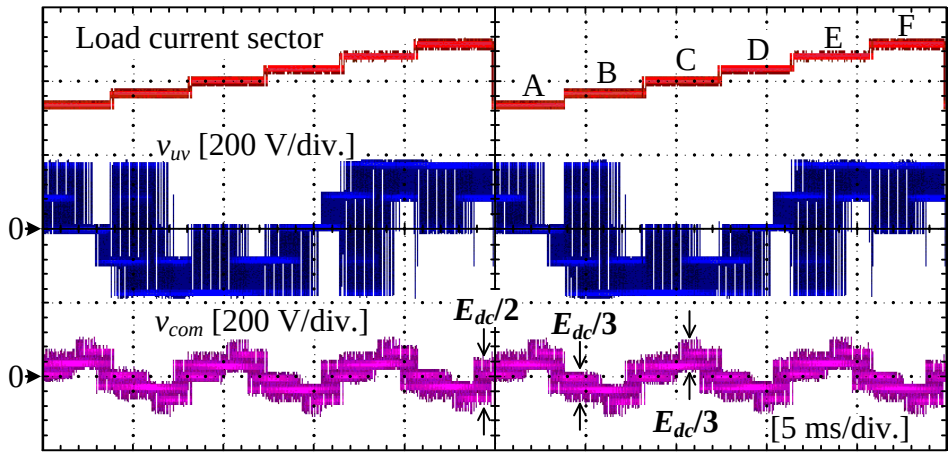
The common-mode voltage with large magnitude might result in high common-mode current (CMC, motor leakage current). This may lead to the motor bearing failures, EMI noise and so on [6-15]–[6-17]. Note that CMC (motor leakage current) flows to ground through the parasitic capacitances between the motor wirings and frame [6-16].

Fig. 6.21 shows the measured common-mode voltage with each modulation method at the modulation index of 0.930 and the load power factor of 0.866. Note that the star point of the several hundred kΩ resistances connected to 3LVSI three-phase outputs is probed to observe v_{com} as the imaginary star point of the motor load. Fig. 6.21 demonstrates that the peak to peak value of v_{com} is increased with the proposed SVPWM compared to the conventional SVPWM. However, the *dv/dt* of v_{com} is important for the electromagnetic interference (EMI) [6-18]. When the conventional SVPWM is applied, the equivalent zero vector of the two-level SVPWM in each voltage sector (e.g., $\mathbf{V}_7$ in the voltage sector I) is always applied during the switching period. The both switching states of the equivalent zero vector (e.g., (+ 0 0) and (0 – –) as $\mathbf{V}_7$) leads to the v_{com} step change of $E_{dc}/2$ over an entire period. On the other hand, the proposed vector patterns to minimize the rms value of 3LVSI input current do not contain the application of the equivalent zero vectors, leading the smaller v_{com} step change of $E_{dc}/3$.

Fig. 6.22 shows the harmonic component of the common-mode voltage under the same conditions in Fig. 6.21. Note that the common-mode voltage is normalized by E_{dc}. By reducing the step change in v_{com} with the proposed SVPWM, the switching frequency component of 10 kHz is reduced by 11.5 points, might be leading to the smaller motor leakage current peak. On the other hand, the proposed SVPWM worsens the 3rd-order v_{com} component by 7.14 points compared to the conventional SVPWM. In the proposed SVPWM, the positive switching state (+) is mainly applied in the following load current sectors (A, C, E), whereas the negative switching state (–) is mainly applied in the following load current sectors (B, D, F). This asymmetric selection of the switching states during the consecutive load current sectors results in the larger v_{com} fluctuations at triple frequency of the fundamental waveform, which is observed in Fig. 6.21(b). Furthermore, the high-frequency component such as of 150 kHz is increased by 0.0897 points due to the complicated voltage space vector selections in the proposed SVPWM. Assuming that CMC component of 150 kHz is dominant to design common-mode filter attenuation, the worsened v_{com} component of 150 kHz with the proposed SVPWM indicates that the proposed SVPWM might lead to the bulky common-mode filter compared to those with the conventional SVPWM.

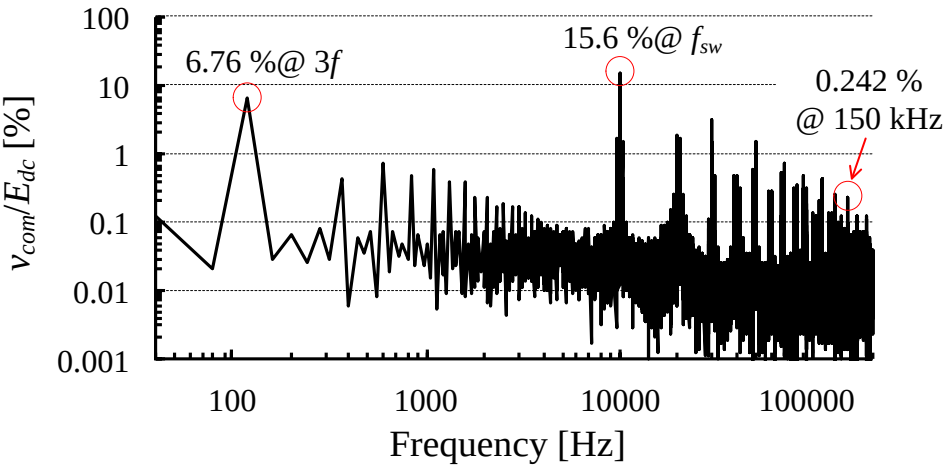


(a) Conventional SVPWM.

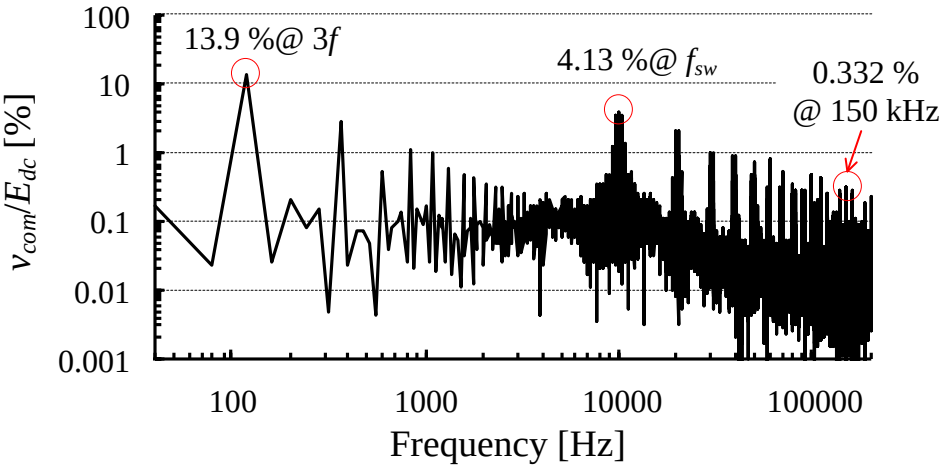


(b) Proposed SVPWM.

Fig. 6.21. Measured common-mode voltage at m = 0.930 and cos φ = 0.866 (30° lagging).



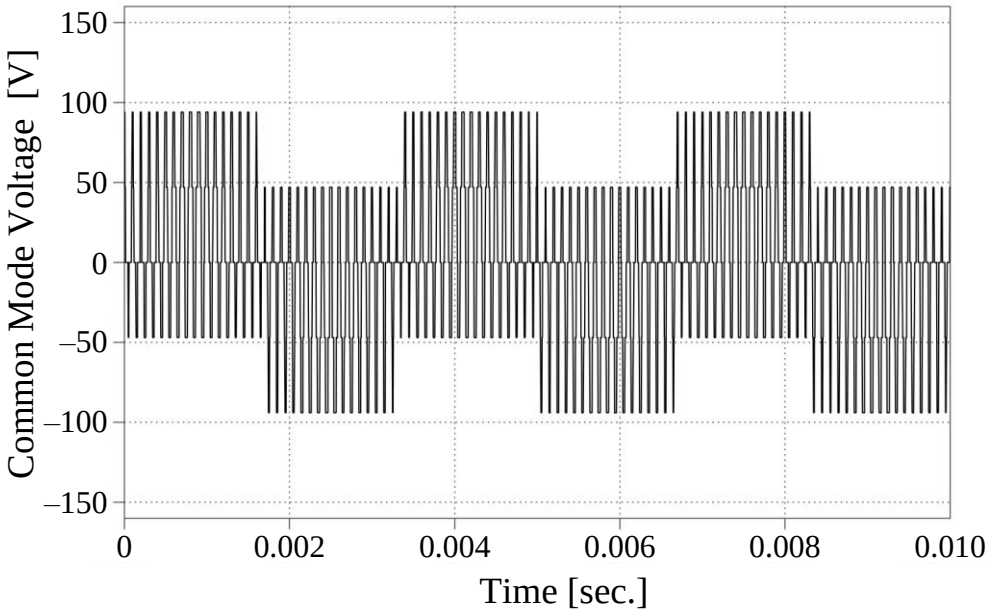
(a) Conventional SVPWM.



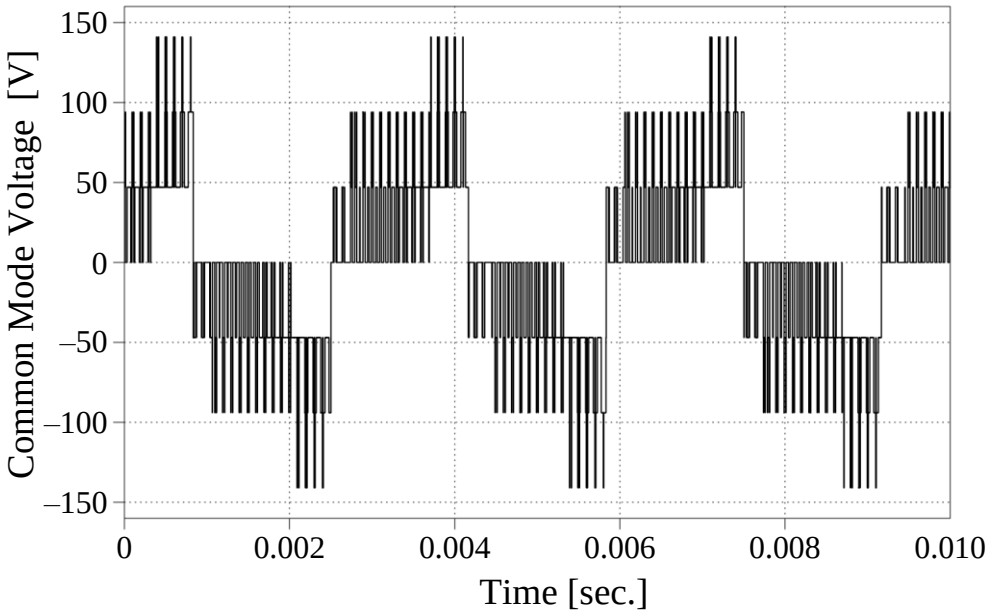
(b) Proposed SVPWM.

Fig. 6.22. Harmonic components of common-mode voltage at m = 0.930 and cos φ = 0.866 (30° lagging) (under same conditions as in Fig. 6.21). The fundamental frequency f is 40 Hz, whereas the switching frequency f_{sw} is 10 kHz.

Figs. 6.23–6.24 show the PLECS simulation results of common-mode voltage waveforms and the harmonic components at the modulation index of 0.930 and the load power factor of 0.866 under same conditions as in the experiment shown in Figs 6.21–6.22. Note that the fundamental frequency is set to 100 Hz for the simplification of the harmonic analysis, whereas the switching frequency is 10 kHz. Fig. 6.24 demonstrates the conducted EMI frequency band components of the common-mode voltage up to 30 MHz. This simulation results demonstrate that the conducted EMI frequency band components of v_{com} is also worsened with the proposed SVPWM.

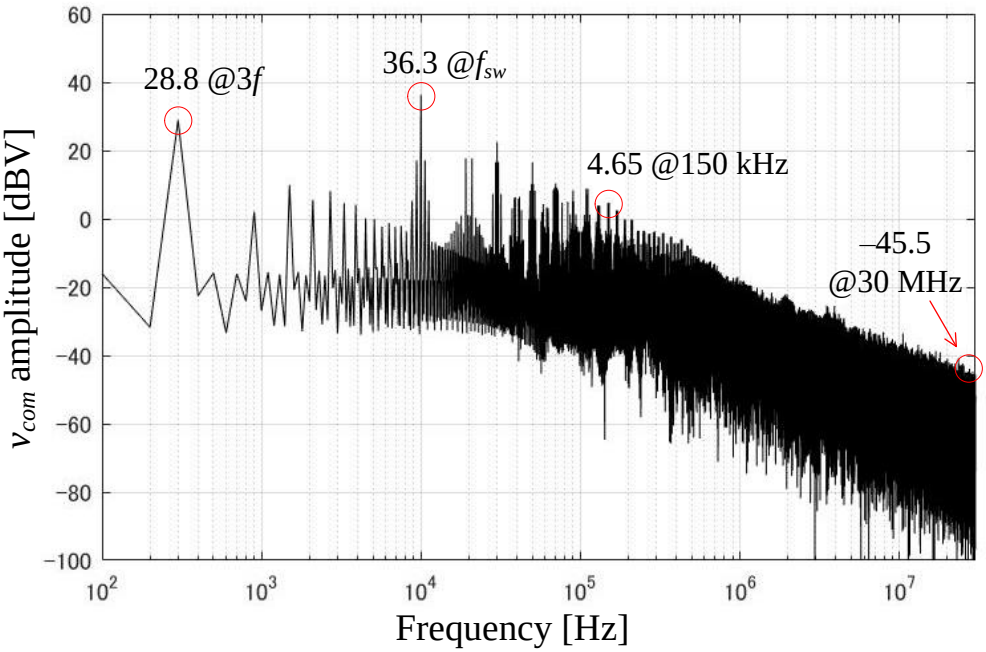


(a) Conventional SVPWM.

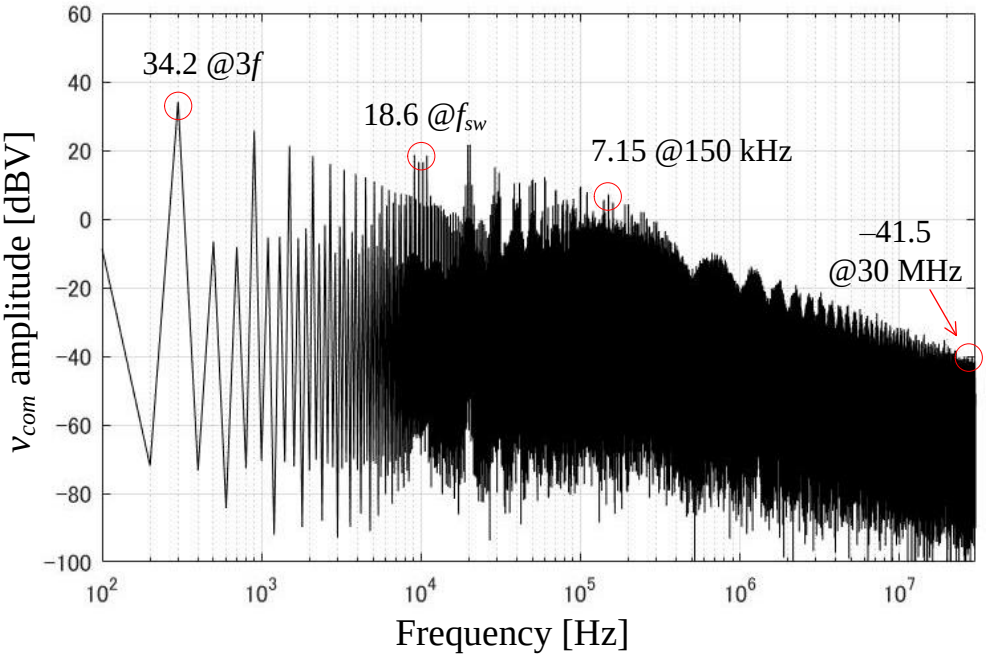


(b) Proposed SVPWM.

Fig. 6.23. PLECS simulation results of common-mode voltage at $m = 0.930$ and $\cos \varphi = 0.866$ (30° lagging) (under same conditions as in Figs. 6.21–6.22 except for fundamental frequency of 100 Hz).



(a) Conventional SVPWM.



(b) Proposed SVPWM.

Fig. 6.24. v_{com} harmonic spectrum at m = 0.930 and cos φ = 0.866 (30° lagging) (under same conditions as in Figs. 6.21–6.22 except for fundamental frequency of 100 Hz).

6.7. Electrolytic Capacitor Lifetime Estimation

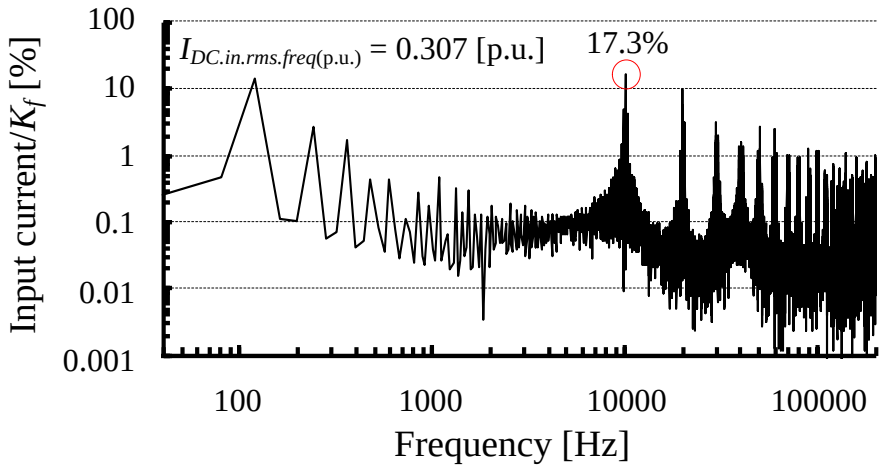
Fig. 6.25 shows the harmonic components of the input current considering the frequency dependence of the ESR of aluminum electrolytic capacitor (NX series, Nichicon Corp. [6-19]) at the modulation index of 0.930 and the load power factor of 0.866 (under the same conditions as in Fig. 6.13). The expected lifetime (L_n) of the electrolytic capacitors is calculated as the same manner introduced in the chapter 3.6. The proposed SVPWM reduced the input current harmonics $I_{DC.in.rms.freq}$(p.u.) by 25.4% when the frequency dependence of the ESR of aluminum electrolytic capacitor is considered. Assuming that the motor is mostly operated at the modulation index of 0.930 and the load power factor of 0.886, and the aluminum electrolytic capacitors in the conventional SVPWM are designed at the worst case of the rated ripple current (i.e., F_I as 1), the lifetime expectancy of the electrolytic capacitor can be given by

$$L_{n\_conv.SVPWM} = L_o \times 1 = 5000 \text{ h.} \quad \text{.....(6.11)}$$

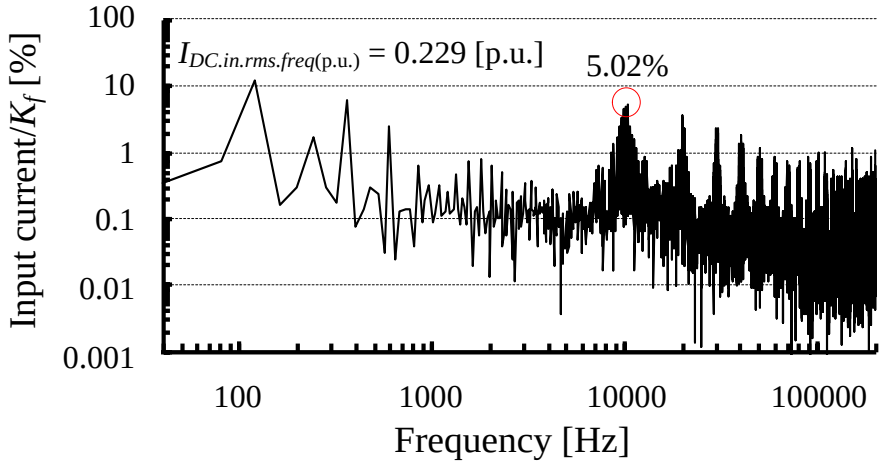
On the other hand, the application of the proposed SVPWM raises F_I to 1.36 due to a current harmonic reduction of 25.4%. So, the lifetime expectancy of the electrolytic capacitor with the proposed SVPWM can be given by

$$L_{n\_prop.SVPWM} = L_o \times 1.36 = 6800 \text{ h.} \quad \text{.....(6.12)}$$

It is concluded that the application of the proposed SVPWM might extend the lifetime of the electrolytic capacitor about 1.36 times longer at most than that of the conventional SVPWM.



(a) Conventional SVPWM.



(b) Proposed SVPWM.

Fig. 6.25. Harmonic components of input current considering frequency dependence of ESR of aluminum electrolytic capacitor at m = 0.930 and cos φ = 0.866 (30° lagging) (under same conditions as in Fig. 6.13).

6.8. Conclusion

The proposed SVPWM in this chapter optimized the combinations of the applied voltage space vector to reduce 3LVSI input current harmonics based on the load current sector as well as the proposed SVPWM for two-level VSI. This proposed SVPWM contributed to the current harmonics reduction of the dc-link capacitors in NPC-3LVSI which achieves high voltage capacity compared to two-level VSI. In comparison with the conventional SVPWM, the proposed SVPWM reduces the input current harmonics by 25.4%, which might be leading to the 1.36 times lifetime extension of the electrolytic capacitors. Furthermore, the proposed SVPWM reduced 3LVSI input current harmonics over entire range of the load power factor, which is also the typical requirement of the high voltage motor drive system. On the other hand, the dc-bus neutral point potential control is not achievable in the high-modulation index region of the proposed SVPWM because no redundant vectors are used. However, by sacrificing the load current quality or the reduction effect on the input current harmonics, the dc-bus neutral point potential control is achieved. In addition, the effect on EMI might be another drawback of the proposed SVPWM and will be future task.

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Chapter 7

Conclusion

7.1 Discussion

The dc-link capacitors play an important role in the AC motor drive system acting as an energy buffer between the input and output of the three-phase VSI. These are important components but cause reliability issue due to its heat-sensitivity.

The motivation of this thesis is to reduce the dc-link capacitor current stress over wide range of load power factor, which is the typical requirement of the AC motor drive system. Specifically, the reduction of the dc-link capacitor current stress is effective in improving the power density especially in the EV applications where the rated ripple current is key factor to design the capacitors. Chapter 2 reviews the state of arts of the current approaches to extend the dc-link capacitor reliability. The circuit configuration-dependent approaches can improve the dc-link capacitor reliability by elimination or great reduction of the dc-link capacitance. Nevertheless, those approaches raise a big problem of the low stiffness of the dc-link, which is unsuitable for the AC motor drive systems with the consideration of fault conditions. On the other hand, the modified PWM approaches reduce the dc-link capacitor current harmonics without the dc-link stiffness issue. However, the conventional PWM approaches are able to reduce the dc-link capacitor

current harmonics only in a limited load power factor range; therefore, those PWM strategies are not applicable for the AC motor drive system. Then, this thesis proposes new PWM strategies to reduce the dc-link capacitor current harmonics with the varied load power factor with the introduction of the load current sector. For balanced three-phase load, the combination of three-phase load currents' directions switches every 60° of phase angle. These 60° periods are defined as the load current sectors. The proposed PWM strategies optimize the switching patterns by using the load current sector.

Chapter 3 describes the optimization method for the PWM switching patterns to reduce the dc-link capacitor current stress with the consideration of the load power factor variation based on the space vector concept. With the introduction of the new load current sectors, which are determined by the output phase current directions, the PWM switching pattern optimization for the minimization of the dc-link capacitor current stress is possible under any load power factor conditions. The simulation and experimental results have verified the validity of the proposed SVPWM strategy, including (i) reducing the dc-link capacitor current harmonics both in the driving mode and the regenerative braking mode, and (ii) lowering the capacitor heating due to its ripple current, and (iii) improving the common-mode voltage harmonics. However, the analytical and experimental results have also demonstrated the deteriorated load current THD, which has a trade-off relationship with the dc-link current harmonics, with the proposed SVPWM. Furthermore, in order to achieve the optimized PWM switching patterns for the minimization of the dc-link capacitor current stress, the high cost digital hardware such as FPGA is necessary.

Chapter 4 describes the proposed carrier-based continuous PWM strategy to reduce the dc-link capacitor current stress. The proposed CPWM is achievable with the more practical digital hardware such as micro-computer, which is used in the EV applications, through the use of its signal-updated-timings. The PWM switching patterns to reduce the dc-link capacitor current stress are implemented by shifting the classical continuous

modulating signals in every half control period based on the load current sector. Furthermore, the proposed sinusoidal-based modulating signals, which do not contain any triplen harmonics, achieve small load current THD deterioration. The analytical, simulation and experimental results have verified the validity of the proposed CPWM in terms of both the dc-link capacitor current stress reduction and the small load current harmonics deterioration. However, the proposed sinusoidal-based modulating signals limits the maximum voltage transfer ratio up to 0.866. Furthermore, the absence of the gate pulse symmetry about the center of the control period due to the proposed shifted modulating signals leads to the increased common-mode voltage harmonics.

Chapter 5 describes the proposed carrier-based discontinuous PWM strategy to reduce the dc-link capacitor current stress. The proposed DPWM is also achievable only with the general-purpose micro-computer as well as the proposed CPWM. Furthermore, the injection of the proper zero-sequence signal based on the load current sector in the three-phase modulating signals provides both the extended maximum voltage transfer ratio and the adaptation to the load power factor variation. The analytical, simulation and experimental results have verified the validity of the proposed DPWM in terms of the dc-link capacitor current stress reduction. However, the absence of the gate pulse symmetry about the center of the control period in the proposed DPWM deteriorates the common-mode voltage harmonics as well as the proposed CPWM.

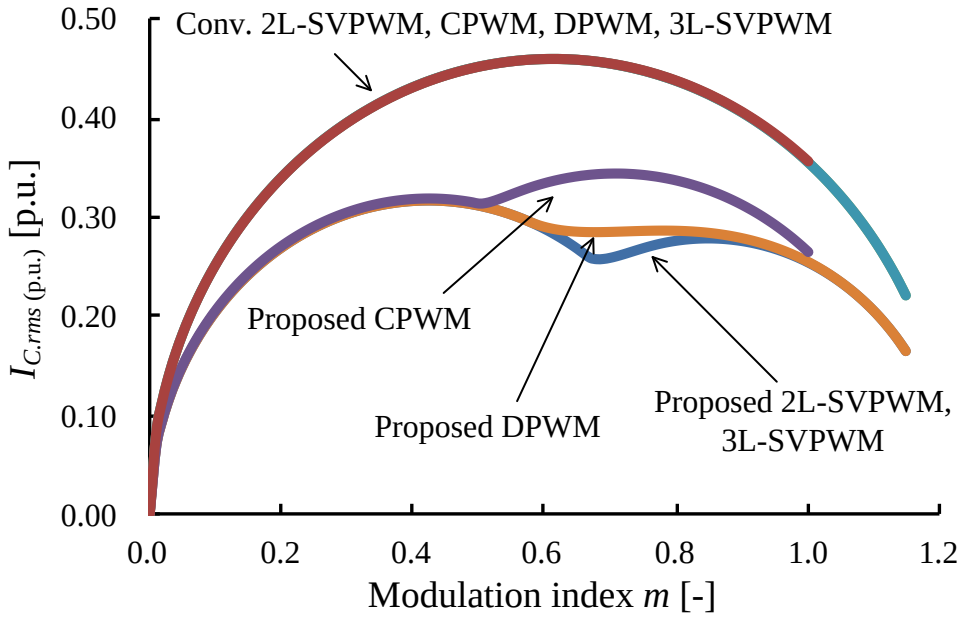
Chapter 6 demonstrates the application of the proposed optimization method for the PWM switching patterns to reduce the dc-link capacitor current stress based on the load current sector to the three-level VSI. Due to the more available voltage space vectors of 3LVSI than those of 2LVSI, there is a number of the optimized combinations of the voltage space vectors for the minimization of the dc-link capacitor current stress. Therefore, it is possible to take into account for the load current quality to decide the proposed PWM switching patterns. The analytical, simulation and

experimental results have verified the validity of the proposed three-level SVPWM in terms of the dc-link capacitor current stress reduction. Furthermore, the electrolytic capacitor lifetime calculation confirms that the proposed three-level SVPWM extend the lifetime with the proposed three-level SVPWM.

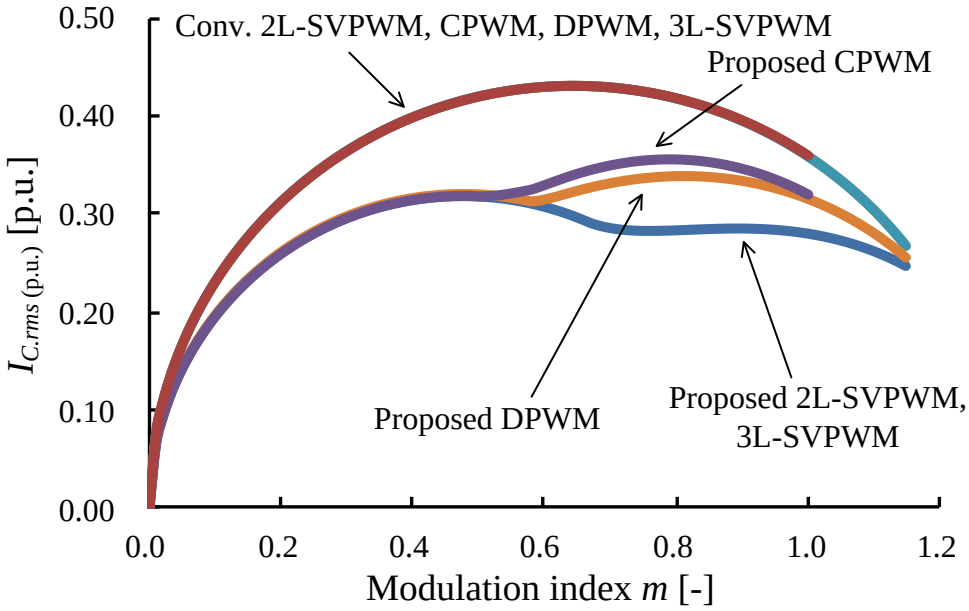
7.2 Comparison of Proposed PWM Strategies

This chapter compares the three proposed PWM strategies for 2LVSI and the proposed SVPWM for 3LVSI to reduce the dc-link capacitor current stress with the corresponding conventional PWM strategies, respectively. This comparison is based on the analytical results which are demonstrated in chapter 3.5, chapter 4.3, chapter 5.3, and chapter 6.5. For the comparison between the PWM strategies for 2LVSI, the dc-link film capacitor heating test results which are demonstrated in chapter 3.6.4, chapter 4.4.4, and chapter 5.4.4 are also referred due to the same simulation and experimental conditions. The simulation and experimental results in chapter 6.6 are referred for the comparison between the conventional and proposed SVPWM for 3LVSI.

Fig. 7.1 shows the comparisons of the dc-link capacitor rms current, which is calculated as (2.13), under the high-load power factor conditions. Both figures confirm that there are no $I_{C.rms(\text{p.u.})}$ differences between the conventional 2L-SVPWM, CPWM, DPWM, and 3L-SVPWM due to those same applying durations of the active vectors and the zero vectors. Fig. 7.1(a) demonstrates that the capacitor current reduction 2L-SVPWM and 3L-SVPWM leads to the best reduction effect in the modulation index region from 0.6 to 0.8 under the unity load power factor condition, which is a typical operating condition of the grid-tied VSI. Within the carrier-based PWM approaches, the capacitor current reduction DPWM leads to the better reduction effect than those of the CPWM approach. This is because the fact that certain one phase discontinuous modulating signal is always clamped, making it possible to set the switching pattern which leads to the smaller $i_{DC.in}$ ripple longer than CPWM approach. Fig. 7.1(b) demonstrates the dc-link capacitor heating experimental condition of cos φ = 0.891 with an induction motor load. The trend in the reduction effect of $I_{C.rms(\text{p.u.})}$ between the three proposed PWM strategies is clearly shown also in this condition.



(a) cos φ = 1.0.



(b) cos φ = 0.891 (27° lagging).

Fig. 7.1. $I_{C.rms(p.u.)}$ comparisons between conventional and proposed PWM strategies against different modulation index at high-load power factor conditions.

Fig. 7.2 shows the comparison of the harmonic flux rms values, which is calculated as (3.4) and used as the evaluation function of the load current quality, at the unity load power factor condition. Fig. 7.2 confirms that the all proposed PWM strategie worsen λ_{rms} compared to those obtained with each conventional PWM strategies. The reason is because the proposed PWM strategies result in the application of the voltage space vector which is not the closest to the reference voltage vector $\mathbf{V}^*$. Within the proposed PWM strategies, the proposed 2L-SVPWM leads to the worst λ_{rms}, and the proposed CPWM leads to the minimal deterioration. This trend in the worsened λ_{rms} with the proposed PWM strategies is in a trade-off relationship with the trend in the improved $I_{C.rms(\text{p.u.})}$ which is shown in Fig. 7.1.

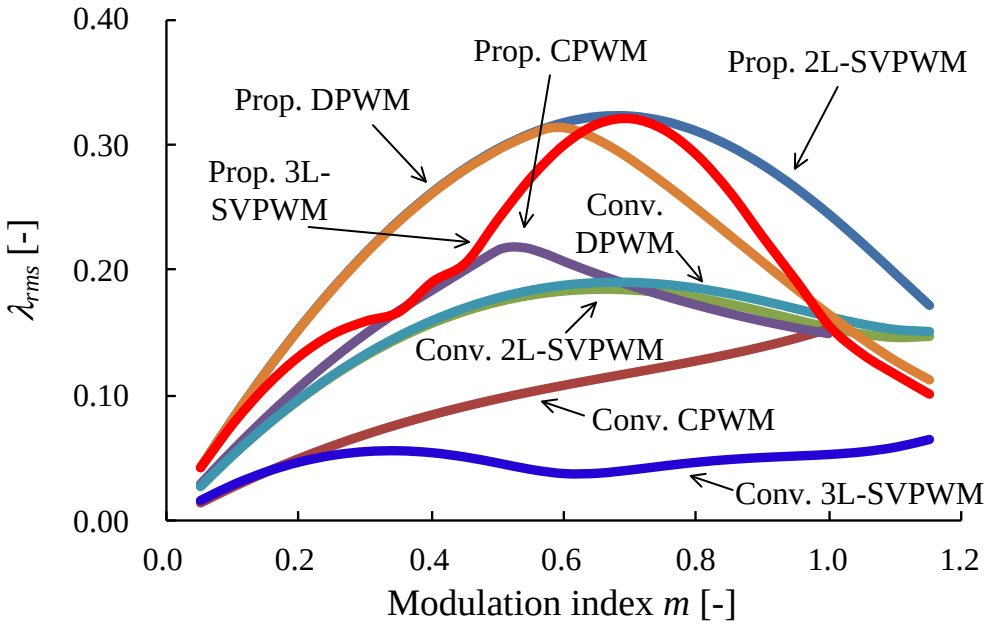


Fig. 7.2. Load current quality comparisons between conventional and proposed PWM strategies against different modulation index at unity load power factor conditions. In this comparison, the harmonic flux rms value λ_{rms} is used as the evaluation function.

Table 7.1 lists the comparison of the conventional and proposed PWM strategies for 2LVSI based on the dc-link film capacitor heating test results. In terms of the dc-link capacitor current stress and its heating, the proposed SVPWM leads to the greatest reduction effect, whereas the proposed CPWM leads to the smallest reduction effect, of which trend is also confirmed by the analytical results shown in Fig. 7.1. However, the load current THD trend confirms the trade-off between the improved dc-link capacitor current stress and the deteriorated load current quality. The proposed CPWM leads to the smallest load current deterioration while achieving the dc-link capacitor current stress reduction. In terms of the inverter efficiency, the facts that one leg is always clamped during each control period with the proposed SVPWM and DPWM leads to the higher efficiency than those with the proposed CPWM. In terms of the common-mode voltage v_{com} harmonics (conducted EMI frequency band), the proposed SVPWM which uses the near switching state voltage vectors with the gate pulse symmetry about the center of the control period achieves the common-mode voltage harmonics reduction as well. The proposed CPWM and DPWM also use the near switching states; however, the absence of the gate pulse symmetry through the use of only micro-computer increase the conducted EMI frequency band components.

Finally, it is concluded that it is possible to select the appropriate one from the proposed three PWM strategies depending on the required application. If there is no digital hardware restriction and the load motor current distortion is not problem, the SVPWM approach is the most beneficial. Otherwise, the carrier-based CPWM and DPWM are better choices, whereas there is the trade-off between the maximum voltage transfer ratio and the load current quality.

TABLE 7.1.
COMPARISON OF CONVENTIONAL AND PROPOSED PWM STRATEGIES FOR 2LVSI BASED ON DC-LINK FILM CAPACITOR HEATING TEST RESULTS.

Comparison Aspects	SVPWM (Chapter 3)		Carrier-based CPWM (Chapter 4)		Carrier-based DPWM (Chapter 5)	
	Conv.	Prop.	Conv.	Prop.	Conv.	Prop.
DC-link capacitor loss	0.780 W	0.357 W	0.777 W	0.531 W	0.807 W	0.395 W
DC-link cap. heating diff.	11℃ (18.9%)		4.4℃ (8.92%)		8.0℃ (17.5%)	
Load current THD	3.67%	5.07%	2.87%	4.03%	2.89%	4.61%
Inverter efficiency	96.11%	96.39%	95.27%	95.17%	96.30%	96.22%
v_{com} (conducted EMI band)	Medium	Low	Low	High	Low	High
Max. volt. transfer ratio	1.0		0.866		1.0	
Digital hardware demand	DSP + FPGA		Micro-computer		Micro-computer	

Table 7.2 lists the comparison of the conventional and proposed SVPWM strategies for 3LVSI. There is also trade-off between the dc-link capacitor current stress and the deteriorated load current quality as well as the proposed PWM strategies for 2LVSI. In terms of the inverter efficiency, the proposed SVPWM leads to the higher efficiency due to its less number of switching transitions in switching period. However, the conducted EMI frequency band components of the common-mode voltage is worsened with the proposed SVPWM due to the complicated voltage space vector selections. Even though the proposed 3L-SVPWM has several drawbacks, this PWM strategy is potentially applicable to the high-voltage AC motor drive systems for the dc-link capacitor current stress reduction.

TABLE 7.2.
COMPARISON OF CONVENTIONAL AND PROPOSED SVPWM STRATEGIES FOR 3LVSI.

Comparison Aspects	3L-SVPWM (Chapter 6)	
	Conv.	Prop.
DC-link capacitor current stress	High	Low
Load current quality	High	Low
Inverter efficiency	Low	High
v_{com} (conducted EMI band)	Low	High
Max. volt. transfer ratio	1.0	
Digital hardware demand	DSP + FPGA	

7.3 Future Works

This thesis has demonstrated that the proposed PWM strategies are capable of achieving the dc-link capacitor current stress reduction for the AC motor drive system of which the load power factor variation is wide. However, the proposed PWM strategies are still required further research to achieve high-reliability and high-power density AC motor drive system.

7.3.1 AC Motor Loss Consideration

The proposed PWM strategies reduce the dc-link capacitor current stress at the sacrifice of the load current quality. This deteriorated load current quality might cause the AC load motor losses, resulting in the motor heating. High temperatures inside the motor may result in insulation failure in winding or magnetic behavior transition between ferromagnetic-phase and paramagnetic-phase. Due to above reasons, a future work is to analyze the AC motor loss and heating with the proposed PWM strategies in order to consider the reliability of the whole AC motor drive system.

7.3.2 Common Mode Filter Consideration

The proposed CPWM and DPWM achieves the dc-link capacitor current stress reduction only with the micro-computer through the use of its signal-updated-timings. On the other hand, this unique generation method of the modulating signals result in the absence of the gate pulse symmetry about the center of the control period. The simulation results in Figs. 4.25 and 5.22 demonstrate that the conducted EMI frequency band components of the common mode voltage are worsened with the proposed CPWM and DPWM, might be requiring the stronger attenuation of the common mode filter. In order to achieve the higher power density of the whole AC motor drive system, it is also necessary to consider the common mode filter volume requirement when the proposed PWM strategies are applied.

List of Achievements

Publication Journals

[1] Koroku Nishizawa, Jun-ichi Itoh, Akihiro Odaka, Akio Toba, and Hidetoshi Umida, “Current Harmonic Reduction Based on Space Vector PWM for DC-Link Capacitors in Three-Phase VSIs Operating Over a Wide Range of Power Factor,” in *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4853–4867, May. 2019.

[2] Koroku Nishizawa, Jun-ichi Itoh, Akihiro Odaka, Akio Toba, Hidetoshi Umida, and Satoru Fujita, “Current Stress Reduction for DC-Link Capacitors of Three-Phase VSI with Carrier-Based Continuous PWM,” in *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 6061–6072, Nov/Dec. 2019.

[3] Koroku Nishizawa, Jun-ichi Itoh, Akihiro Odaka, Akio Toba, and Hidetoshi Umida, “Microcomputer-based Discontinuous PWM for DC-link Current Harmonic Reduction in Three-phase VSIs,” in *IEEJ Journal of Industry Applications*, vol. 8, no. 6, pp. 904–914, Nov. 2019.

[4] Koroku Nishizawa, Jun-ichi Itoh, Akihiro Odaka, Akio Toba, and Hidetoshi Umida, “Input Current Harmonic Reduction based on Space Vector PWM for Three-level Inverter Operating over a Wide Range Power Factor,” in *IEEJ Journal of Industry Applications*, vol. 9, no. 3, 11 pages (In press).

International Conference Proceedings (Peer-reviewed)

[1] Koroku Nishizawa, Jun-ichi Itoh, Akihiro Odaka, Akio Toba, and Hidetoshi Umida, "Reduction of Input Current Harmonics based on Space Vector Modulation for Three-phase VSI with varied Power Factor," *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, pp. 1–8, EC-0318, 2016.

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[3] Koroku Nishizawa, Jun-ichi Itoh, Akihiro Odaka, Akio Toba, and Hidetoshi Umida, "Reduction of DC-link current harmonics for Three-phase VSI over Wide Power Factor Range using Single-Carrier-Comparison Discontinuous PWM," *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Warsaw, pp. 1–10, 0297, 2017.

[4] Koroku Nishizawa, Jun-ichi Itoh, Satoru Fujita, Akihiro Odaka, Akio Toba, and Hidetoshi Umida, "Reduction of DC-link Current Harmonics over Wide Power-Factor Range for Three-Phase VSI using Single-Carrier-Comparison Continuous PWM," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, pp. 6772–6779, 2018.

[5] Koroku Nishizawa, Jun-ichi Itoh, Satoru Fujita, Akihiro Odaka, Akio Toba, and Hidetoshi Umida, "Thermal Stress Reduction for DC-link Capacitors of Three-phase VSI with Multiple PWM Switching Patterns," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, pp. 1584–1591, 2019.

National Conference Proceedings

[1] Koroku Nishizawa, Koji Orikawa, Jun-ichi Itoh, Akihiro Odaka, Akio Toba, and Hidetoshi Umida, “Space Vector Modulation to Reduce Input Current Harmonics of two-level VSI Corresponding to the Power Factor Change,” *2015 Semiconductor Power Conversion Joint Conference*, Sapporo, SPC-15-133/MD-15-104, pp. 7–12, 2015.

[2] Koroku Nishizawa, Koji Orikawa, Jun-ichi Itoh, Akihiro Odaka, Akio Toba, and Hidetoshi Umida, “Experimental Verification of a Space Vector Modulation to Reduce Input Current Harmonics of Two-level VSI Corresponding to the Power Factor Change,” *2016 Annual Meeting Record IEEJ*, Sendai, no. 4-086, pp. 144–145, 2016.

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[5] Koroku Nishizawa, Jun-ichi Itoh, Akihiro Odaka, Akio Toba, and Hidetoshi Umida, “Input Current Harmonics Reduction for Three-phase VSI over Wide Load Power Factor Range using Carrier-Comparison PWM based Discontinuous PWM,” *2017 IEEJ Industry Application Society Conference (JIASC2017)*, Hakodate, no. 1-109, pp. 491–494, 2017.

[6] Koroku Nishizawa, Jun-ichi Itoh, Satoru Fujita, Akio Toba, and Hidetoshi Umida, “Estimation method of Average Current Value for Discontinuous PWM to Reduce Input Current Harmonics of Three-phase VSI over Wide Power Factor Range,” *2018 Annual Meeting Record IEEJ*, Fukuoka, no. 4-029, pp. 45–46, 2018.

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